Design Considerations of Distributed and Centralized Switched-Capacitor Converters for Power Supply On-Chip

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***Abstract*— On-chip power supply distribution faces the challenges of high and fast-changing load current, limited metal layers and decoupling capacitors, efficiency, and thermal issues. This paper mainly discusses system-level design considerations of both distributed and centralized fully integrated voltage regulators. In particular, a ring-shaped switched-capacitor dc–dc converter that has a unity-gain frequency a few times higher than its switching frequency is introduced with comprehensive considerations, and optimizing the number of time-interleaving phases (power cells) is detailed. Design issues such as on-chip power-rail routing parasitics, input capacitor and input ripple, and phase mismatch between power cells are addressed. Furthermore, a couple of possible extensions of the converter-ring architecture are proposed, which include power management of the active-matrix light-emitting diode array in a microdisplay system, cascading multiple nMOS-LDO regulators for granular power, and on-chip power converter grid with flipped-chip packaging.**

***Index Terms*— Active-matrix light-emitting diode (AMLED), amplifier, charge pump, converter ring, dc–dc converter, digital control, dynamic voltage scaling (DVS), fully integrated voltage regulator (FIVR), hybrid converter, low-dropout regulator (LDO), multilevel, multiphase, resonant converter, switched-capacitor (SC) power converter, voltage-controlled oscillator (VCO).**

I. Introduction

THE goal of an on-chip power distribution system is to deliver the requested current across the whole chip to the load circuits while maintaining the voltage level necessary for proper operation of the loads. Therefore, efficient, low-noise, and compact power supply on chip is favorable for fully integrated system-on-a-chip (SoC) solutions [1]–[6]. However, an on-chip power supply suffers from severe *IR* voltage drop because of the thinner routing metal layers compared to printed circuit board (PCB) traces and faces much faster load transient current because it is closer to the load and because of limited on-chip decoupling capacitors. Nevertheless, there are several benefits of integrating voltage regulators on-chip as point-of-load supplies. First, by using advanced technologies, faster transient response can be achieved using smaller passive components with reduced parasitics. Second, by taking the proximity into consideration, more intelligent power management techniques can be realized by a closer interaction with supply and load co-design, using dynamic voltage scaling (DVS) or adaptive voltage scaling. Third, the conducting input current through PCB and bond wires can be reduced by integrating an on-chip step-down power converter, because ideally $I_{\mathrm{IN}} = (V_{\mathrm{OUT}}/V_{\mathrm{IN}}) \times I_{\mathrm{OUT}}$ and $V_{\mathrm{OUT}}/V_{\mathrm{IN}}$ is smaller than one. In addition, the $L_P \times \mathrm{d}i/\mathrm{d}t$ supply variations, due to the in-rush current $\mathrm{d}i/\mathrm{d}t$ and the parasitic inductor L_P of the bond wires and power buses, are now the variations on the input rather than on the output of the regulator, and are relatively more tolerable.

Fig. 1 shows different floor-plans of on-chip power delivery, with dc–dc converter(s) delivering power from one side, two sides, four sides, and from all around the chip. Obviously, the worst case is with only one-side dc–dc converter(s) [Fig. 1(a)] and the converter-to-load parasitic resistor and inductor are R_P and L_P. With opposite-side converters [Fig. 1(b)], the parasitics are reduced to $R_P/2$ and $L_P/2$, and with both sets of converters delivering power together, the effective parasitics are $R_P/4$ and $L_P/4$, and the efficiency could thus be improved. Parasitics could further be reduced by having converters on all four sides [Fig. 1(c)]. Note that each individual converter needs a separate controller that consumes extra power and area. However, if the interleaving technique is employed, individual converters could be designed as sub-converters and they may even be laid out as a ring-shaped converter [5] that uses only one controller with a small area [Fig. 1(d)]. The power cells (or subconverters) of the converter-ring are distributed around the chip and high quality power is accessible at any point of the chip edges.

In the recent years, granular power management has been a popular solution for energy efficient SoCs. The idea of granular power is to divide one lumped supply module into many fine-grained supply voltage domains, such that different loading blocks can operate at different voltage levels or be power-gated according to individual operation needs. Fig. 2 shows the separated on-chip voltage domains being powered up by different low-dropout (LDO) regulators with or without cascading an on-chip dc–dc converter, as the prestage. The LDO regulator is the one easy and compact

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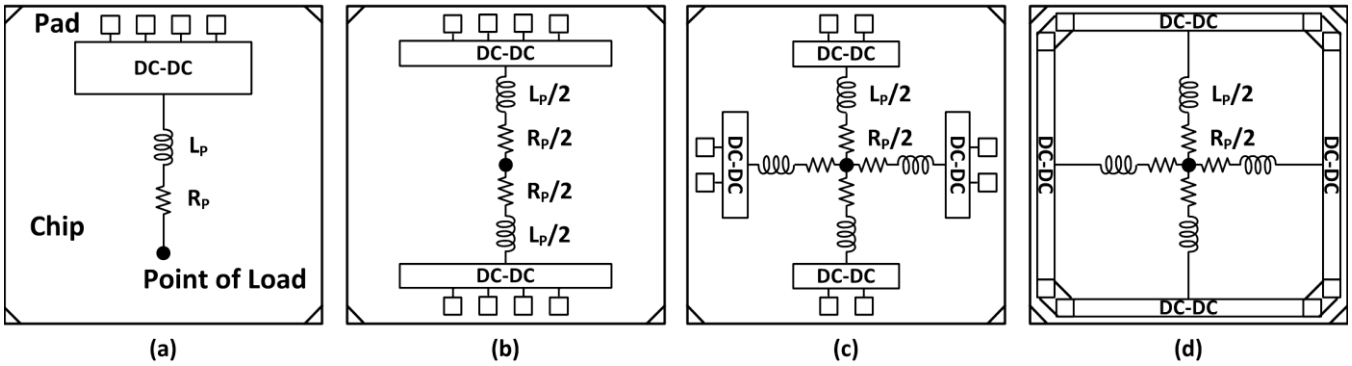

Fig. 1. Parasitics of the supply routing that globally supplied by dc–dc converter(s) from (a) one side, (b) two sides, (c) four sides, and (d) all directions.

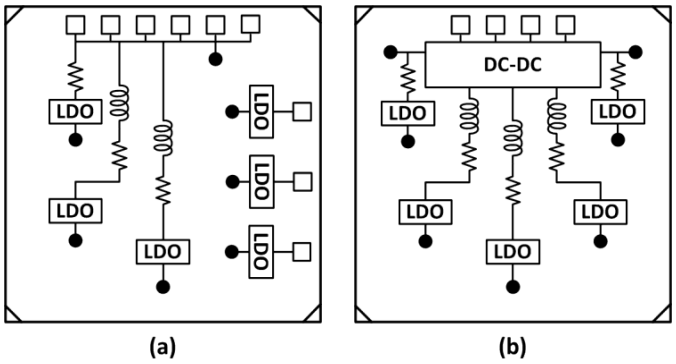

Fig. 2. Granular power supplied by (a) LDO regulators only and (b) dc–dc converter and cascaded LDO regulators.

way to implement DVS and power gating, but the power efficiency is low when the difference between V_{IN} and V_{OUT} is large. Even so, for driving a digital load in the idle mode, lowering the output voltage of the LDO regulator would still be beneficial if dynamic voltage and frequency scaling are incorporated [7]–[9], because while the LDO regulator efficiency drops linearly with V_{OUT}, the power consumption of the digital load drops quadratically with V_{OUT}. Certainly, if the LDO regulator is replaced by the dc–dc converter in realizing DVS then energy saving would be more pronounced [10]–[13]. However, a fully integrated power converter requires significantly larger chip area for the passives, and therefore, high energy density passive components are highly desirable.

The next question is whether distributed or centralized on-chip voltage regulators, or cascaded regulators should be used? We will address this question with considerations on multiple aspects. This paper is organized as follows. Section II gives a review on the fully integrated voltage regulator solutions for power supply on-chip. Section III presents the design considerations of the proposed ring-shaped switched-capacitor (SC) power converter. Section IV discusses issues of chip implementation and possible extensions of the converter-ring structure. Section V summaries the circuit techniques of the SC converter, and finally, conclusions are drawn in Section VI.

II. Fully Integrated Voltage Regulators

It is safe to claim that LDO regulators are the most convenient implementation of fully integrated voltage regulators (FIVRs). Alternative implementations are shown in Fig. 3, which include inductor-based SC and hybrid dc–dc converters.

The inductor-based converter can achieve a theoretical efficiency of 100%, but the actual efficiency highly depends on the quality of the inductor(s). Magnetic core that significantly increases the quality factor has been integrated on-chip with additional postsilicon steps and increased cost [14], [15]. Alternatively, low-cost inductors can be made from bond wires and PCB traces with moderate quality factors [16]–[20]. A down side of using inductors is that they do not shrink as much as capacitors do as the technology advances. Besides the issues of inductor integration, considerably large on-chip input decoupling capacitor needs to be deployed for the buck converters to reduce the bond wire-induced input voltage ripple, especially for very-high-frequency switching converters. To reduce the input voltage ripple, it was proposed in [19] to connect a relatively small capacitor between the input and output nodes of a buck converter.

The SC dc–dc converter does not need any inductors. It takes the advantages of using on-chip capacitors and becomes the simplest FIVR implementation among the candidates, as shown in Fig. 3. However, due to the charge redistribution loss, the SC converter can only attain good efficiency when its V_{OUT} is barely lower than the predefined ideal output voltages $M \times V_{\mathrm{IN}}$, where M is the voltage conversion ratio and the achievable M depends on the converter topology [21]–[23]. Nevertheless, the input voltage ripple of an SC converter could be much lower than that of the buck converter counterpart, because the flying capacitors that connect to V_{IN} are automatically reused as input filtering capacitors. In addition, a fully integrated SC converter can be implemented with a large number of phases with very little power and area overheads by simply slicing a large piece of capacitors and switches into multiple small portions and using a ring oscillator to generate the interleaving clock phases [24]–[26]. In such way, both the input current ripples and output voltage ripples can be much reduced compared to the single-phase or dual-phase cases. In general, SC converters are popular for medium-power to low-power applications [27]–[33], because the required capacitance scaled linearly with its handling power (which is in the opposite way for the required inductance of the inductor-based converters).

Recently, hybrid converters are becoming popular research topics, because they have a large potential to provide a higher

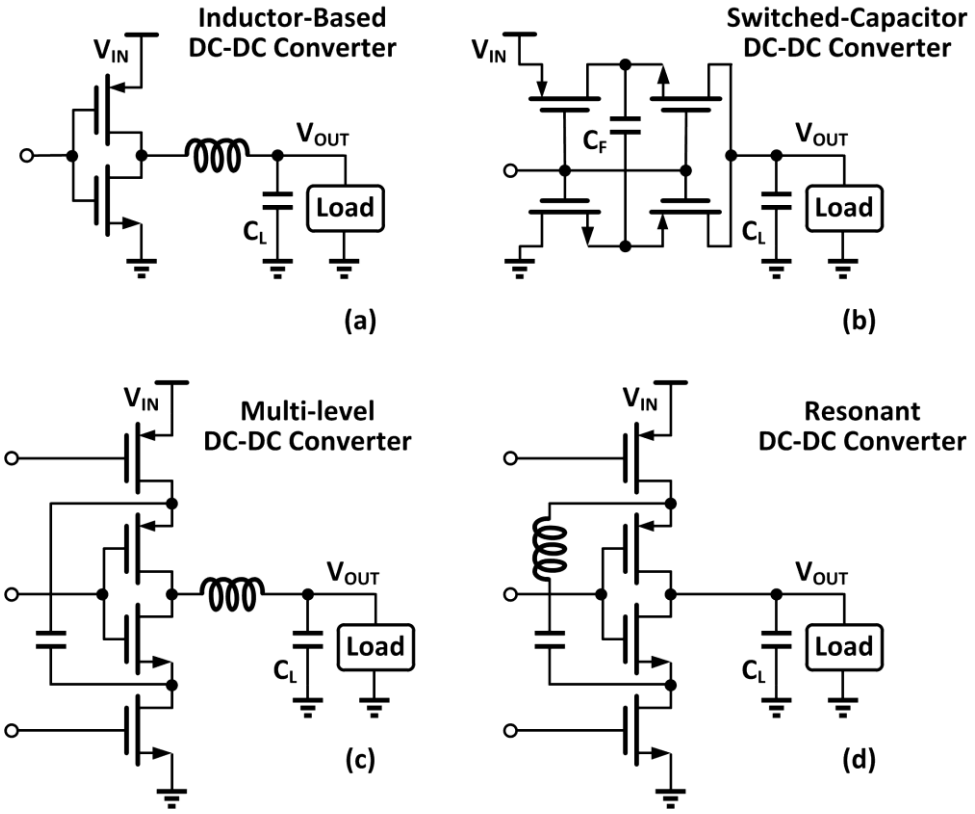

Fig. 3. Step-down. (a) Inductor-based dc–dc converter. (b) SC dc–dc converter. (c) Multilevel dc–dc converter. (d) Resonant dc–dc converter.

product of power density and conversion efficiency [34]–[42]. As shown in Fig. 3(c), multilevel converters employ flying capacitor(s) to generate N voltage levels for one of the inductor terminals while the other terminal is fixed at V_{OUT}. Therefore, the voltage across the inductor is reduced and consequently the inductor current ripple is reduced by a factor of $N-1$, if the same switching frequency is used [34]–[36]. With the same output voltage ripple requirement as the conventional buck converter, a multilevel converter could use much smaller passive components and enables higher loop bandwidth. Thus, with the advantages of both high loop bandwidth and high power efficiency, multilevel converters found a very suitable application in envelope tracking for the RF power amplifier supply modulation [37], [38], [43]. As shown in Fig. 3(d), resonant SC converter can also be considered as a hybrid converter. The resonant converter switches at the resonant frequency of the *LC* resonant tank to obtain a sinusoidal conducting current, which has a smaller root-mean-square (rms) conducting current with the same average output current, and thus increases the efficiency by reducing the conduction loss of the power switches [39]–[41]. However, the resonant converter suffers from slow transient response and has restricted topologies as each flying capacitor needs one inductor to avoid hard switching.

To summarize, the LDO regulator can achieve the highest power density because it has only one linear transistor and has no energy storage component, while the other solutions are process dependent. For higher absolute power, inductor-based and hybrid dc–dc converters that use inductor(s) are excellent candidates. On the contrary, for low power, good flexibility and fast transient response, SC converters, and LDO regulators should be better choices.

III. Multiphase Ring-Shaped SC Converter

Multiphase interleaving is a commonly used technique in fully integrated SC converter. As shown in Fig. 4, to take full advantage of the multiphase interleaving technique, a ring-shaped SC converter with unity-gain frequency (UGF) higher than its switching frequency was implemented [26]. The designed converter ring consists of many time-interleaved power cells and only one controller. The size of the controller layout is exactly the same as that of one power cell. The input and Gnd pins of the converter ring are placed at every corner of the chip, without affecting the pads of the load. Similar to a standard pad ring, the converter ring surrounds the load in the square, with minimum changes (if not no change) to the existing layout of the load. One of the advantages of the power cell approach is the simplicity in design: we only need to design one power cell and one control block. Whether the power ring has 101 or 1001 power cells, it is just a copy-and-paste task. Therefore, the top-level integration of cascading the controller and the power cells is like Lego building.

A. Power Line Routing Parasitics

There are three types of *IR* drops: V_{IN} *IR* drop, V_{OUT} *IR* drop, and Gnd *IR* drop. For the distributed converter-ring architecture, the V_{OUT} and Gnd *IR* drops are lower than

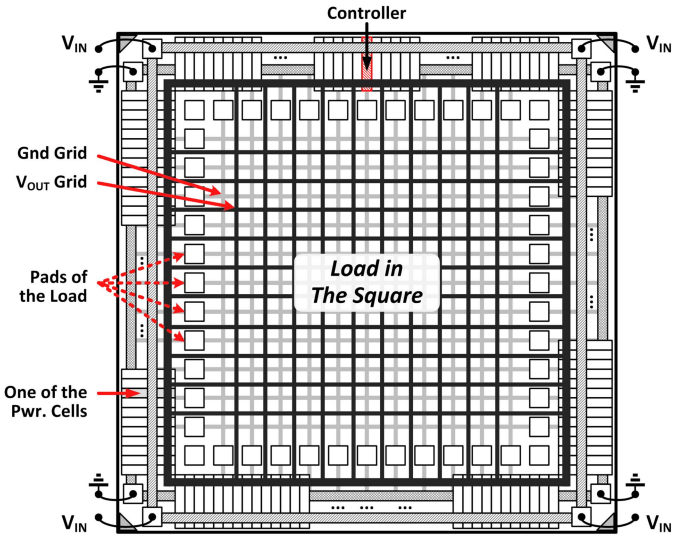

Fig. 4. Ring-shaped multiphase SC dc–dc converter with on-chip V_{OUT} and Gnd grids.

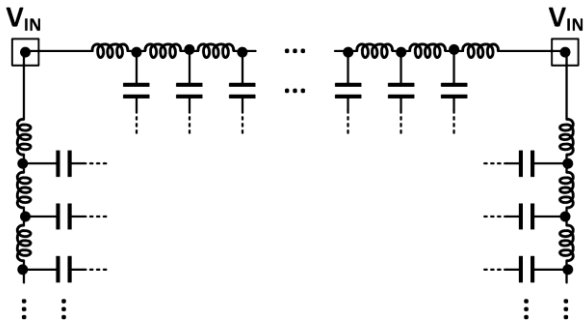

Fig. 5. *LC* network consists of input routing and flying capacitors.

those of the conventional centralized architecture, as illustrated in Fig. 1. In addition, the V_{OUT} and Gnd grids can be designed according to the locations of the loads to minimize the *IR* drops and di/dt variations. Nevertheless, the V_{IN} *IR* drop may increase due to the longer routing parasitics between the input pads and the distributed power cells. Since this is a step-down converter, the input current is roughly M/η times (η is the power conversion efficiency) lower than the output current, which means that the V_{IN} *IR* drop will be lower than the V_{OUT} *IR* drop for the same parasitic resistance. As far as the load is concerned, it matters more for the quality of V_{OUT} and Gnd than that of V_{IN}, and the proposed architecture is favorable in this aspect.

As shown in Fig. 5, although there are larger parasitic inductances due to longer distribution routing at the input node, they will not generate significant ringing and overshoots/undershoots during switching, because the flying capacitors in the SC converter are distributed along the long route. Therefore, the long input routings are split into sections of *LC* networks, which are mainly capacitive due to the large amount of flying capacitors.

B. Multiphase Operation

Let V_{MIN} be the minimum supply voltage that the load can function correctly, a voltage margin of ΔV above V_{MIN} should be reserved for robustness. Obviously, the reserved margin ΔV should also include the output voltage ripple, and reducing the output voltage ripple allows reducing the reserved margin, which means improving the efficiency. An SC converter with interleaving multiphase operation is one of the popular methods of reducing output ripple.

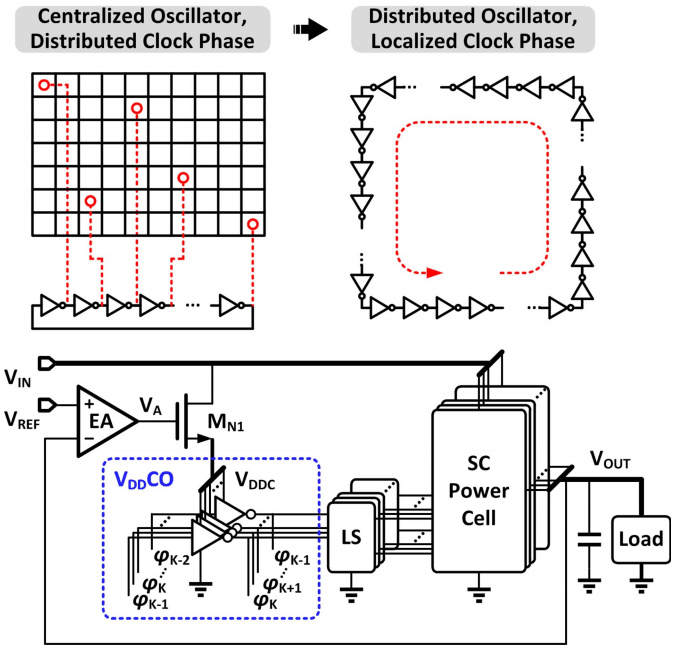

Fig. 6. Schematic of the converter-ring design with distributed oscillator.

In conventional designs, the interleaving clock phases are centrally generated by a ring oscillator or by frequency dividers and are then distributed to each power cell using the H-tree structure or other complicated structures [1], [28], [44]–[47]. When the phase number is very large, say 101, there could be substantial mismatches among different phases that will offset the ripple canceling effect. Therefore, to minimize phase mismatches, the inverters of the ring oscillator should be distributed over every power cell of the SC converter [26], as shown in Fig. 6. All clock phases are localized and the clock phase of each power cell is enabled by the clock phase of its previous power cell. Therefore, phase mismatches are well under controlled, and more phases can be easily employed. Also, this structure is good for digitally scaling up/down the converter strength [24].

The current-starving voltage-controlled oscillator (VCO) used in conventional SC converters cannot change its output frequency fast enough, because there are high-impedance nodes in the ring oscillator. By changing the supply voltage V_{DDC} of the ring oscillator, the oscillation frequency can be effectively and linearly controlled [26]. The error amplifier (EA) compares V_{OUT} with V_{REF} and drives the source follower (M_{N1}) with small output impedance that in turns drives the ring oscillator with fast transient response. As such, pulse-frequency modulation (PFM) can be realized by using the V_{DD}-controlled oscillator (V_{DD}CO).

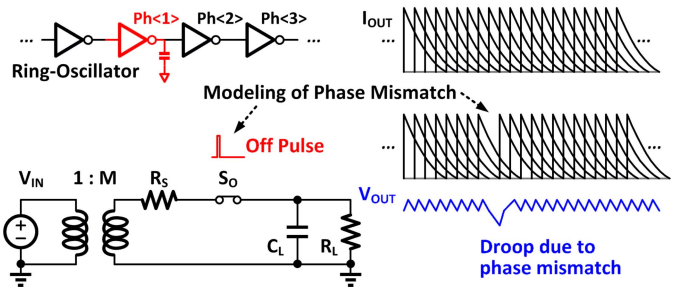

Fig. 7. Modeling of phase mismatch.

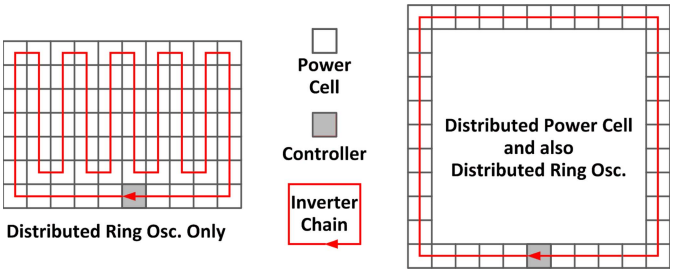

Fig. 8. Architectures for minimum phase mismatch.

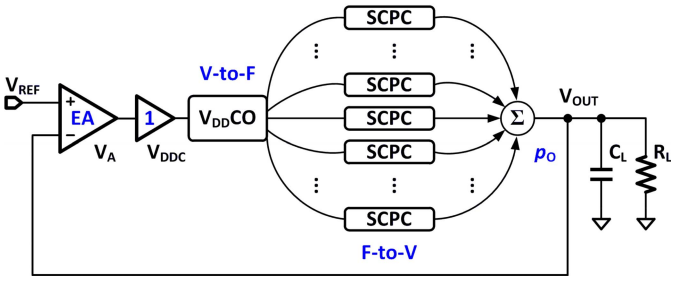

Fig. 9. Small-signal analysis of the multiphase SC converter.

C. Mismatch Between Power Cells

As shown in Fig. 7, the power cells are switched in cascade, controlled by the ring oscillator. Suppose there is a phase mismatch for Ph⟨1⟩ due to a larger routing parasitic capacitor, which could happen to the power cells at the corners of the chip. The phase mismatch could be modeled as if the converter is completely disconnected from the load, because although it only occurs at one of the power cells, all the power cells are actually delayed by the same phase mismatch. Similar to a long queue of people waiting for fast-food ordering, if one people order slowly, all the people behind get delayed.

Phase mismatches could also occur due to process, voltage, and temperature (PVT) variations. Here, two cases should be distinguished, as shown in Fig. 8. They are: the distributed ring oscillator case and the distributed power cell case. In the distributed ring oscillator case, the inverters are distributed into each power cell, but the power cells can be placed together or distributed. In this paper, our scheme can be considered as both distributed power cell and distributed ring oscillator.

When the power cells are distributed, the process and temperature gradients across the chip and the mismatches in $V_{\rm IN}$ *IR* drop of each power cell may result in phase mismatches and consequently larger voltage ripple. Nevertheless, when the power cells are distributed, the switching frequency contains the information of the averaged process and temperature variations of the whole chip. In other words, the process and temperature gradients are embedded into the output frequency of the ring oscillator and the distributed scheme might be more immune to process variations in terms of power density and efficiency. In addition, with reduced equivalent parasitic inductors and resistors for the $V_{\rm OUT}$ node, smaller output voltage ripples can still be expected. If the load is really sensitive to the noise, a possible solution is to employ a separate ground pin in its pad ring for noise absorption/shielding.

D. Extending the UGF of SC Converter

Small-signal analysis of the multiphase SC converter is shown in Fig. 9. One key feature of this paper is that the UGF of the proposed multiphase converter is a few times higher than its switching frequency $F_{\rm S}$. This feature is achieved because of the following.

1) The multiphase SC converter can be considered as a pseudocontinuous-time voltage regulator.
2) The dominant pole is set at the $V_{\rm OUT}$ node.
3) A high-speed EA is employed.
4) The oscillator frequency is tuned through its supply to change F_S of all phases instantly and simultaneously.

SC circuits can be modeled as discrete-time resistors and they provide first-order filtering in the power stage. However, multiphase operation empowers the SC converters with more attractive features, for examples, smaller input and output ripples and faster transient responses, because it allows the converter to response within a small fraction of the switching period, and to act more like a continuous-time voltage regulator. On the other hand, the *LC* tank of a buck converter operating in continuous-conduction mode is a second-order filter, which can provide better filtering but slows down the transient response, because the inductor current needs to be changed before $V_{\rm OUT}$ can be regulated during load/line transients.

For the control loop design, there are several benefits of designing the dominant pole at the output node, as discussed in [48]. If the output pole p_O is a nondominant pole, the loop needs to have an internal dominant pole of which the frequency is a couple of decades lower than p_O, which will limit the UGF. To set p_O as the dominant pole, the converter can drive large capacitive load without affecting the loop stability. More capacitive load only makes the loop more stable.

For an SC converter with no interleaving, ac signals that are higher than $F_S/2$ cannot be recovered according to the Nyquist Sampling Theorem. Nevertheless, it is verified that the time-interleaving multiphase SC power cells (SCPCs) together act as a pseudocontinuous-time stage [26], which means that ac signals higher than F_S can also pass through the discrete-time multiphase power stage. In the proposed $V_{\rm DD}$CO-based PFM scheme, after the voltage information $V_{\rm DDC}$ is converted to frequency information by the $V_{\rm DD}$CO, it is converted back to voltage information by the multiphase SCPC stage. Therefore,

with a high-speed EA design, a UGF that is a few times higher than F_S can be realized.

Although the buck converter can achieve bandwidth extension through multiphase interleaving [49], it does not enjoy the pseudocontinuous-time condition as the SC converter. For the buck converter, the pulse width modulation (PWM) duty-ratio generator is a sampling block [50]. Although, PFM control schemes such as hysteretic control, constant-ON/OFF time control can be applied in buck converter, in fact, the constant-on-time control should be considered as both PWM and PFM control. Because when the load is fixed, the duty ratio and thus the on-time are fixed, as so does the switching frequency. During a large load transient, the duty-ratio should be optimally 100% for light-to-heavy load transition and 0% for heavy-to-light load transition. As such, the sampling effect of the PWM control still applies to the constant-on-time controller, and thus limits the bandwidth extension [51], [52]. Therefore, PFM control with fixed duty ratio, which can be considered as the pseudocontinuous-time operation, can only be applied to the SC converters [26].

E. Design Procedures for SC DC–DC Converter

Let us now turn to the design procedures of the multiphase SC converter. Assume that the chip area available for the SC converter is fixed, there are still five factors to be considered in finding the optimized solution: phase number, switching frequency, output power, output voltage ripple, and efficiency. First, the product of power density and efficiency is basically decided by the process employed and more advanced or post-CMOS processes gives a larger product. The output power level is decided by the application (the load). A flatter efficiency curve versus output power can be achieved with circuit techniques such as capacitance or conductance modulations [27], [53], and a flatter efficiency curve versus output voltage can be achieved with more conversion ratios [54], [55], but when the process and the output power level are set, the peak efficiency is basically set.

The question then becomes how to achieve the required maximum output power with minimum output ripple. To increase the maximum output power, the switching frequency has to be increased. In this converter-ring design, there are two ways to increase the switching frequency. The first is to reduce the number of inverters in the chain, which means less phase number and larger voltage ripple. The second is to increase the strength of each inverter to reduce the duration of each phase, which increases the VCO power consumption (lowers the efficiency) but keeps the voltage ripple unchanged.

Since the ring oscillator is distributed throughout the whole SC converter, the parasitic capacitors on the ring oscillator cannot be ignored and will affect the maximum achievable frequency. To estimate the parasitic capacitance, the following method is used. As shown in Fig. 10, the capacitance between two delay cells consist of the output capacitance C_{OUT} of the prestage $\varphi_{\mathrm{N}-1}$, the input capacitance of the level shifter C_{LS}, the input capacitance C_{IN} of the poststage φ_N, and the parasitic capacitance on the routing wire C_{WIRE}.

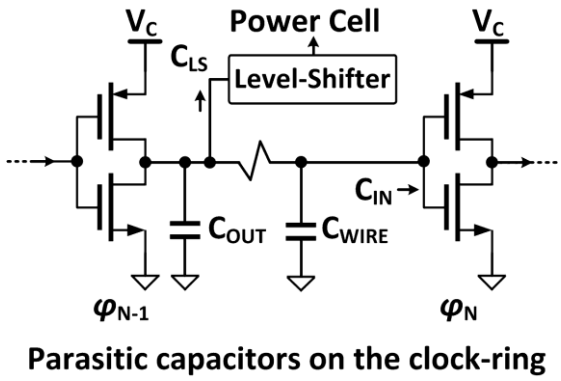

Fig. 10. Parasitic capacitors on the clock ring.

The design of the ring oscillator starts with the total length of the converter ring that is determined by the area of the load. Given a total length L_{TOT} and a phase number N, the total capacitance on one phase of the ring oscillator C_{PHASE} is given by

$$C_{\mathrm{PHASE}} = \frac{L_{\mathrm{TOT}}}{N}a + mC_{\mathrm{LOGIC}} \tag{1}$$

$$C_{\mathrm{LOGIC}} = C_{\mathrm{OUT}} + C_{\mathrm{IN}} + C_{\mathrm{LS}} \tag{2}$$

where a is the parasitic capacitance density on the routing wire and m is the finger multiplier (strength) of the unit inverters. A practical value of a could be chosen as 0.1 fF/μm^2 for rough estimation. The delay of one interleaving phase can then be roughly obtained by

$$t_{\mathrm{d}} \approx \frac{R_{\mathrm{ON}}C_{\mathrm{PHASE}}}{m} \tag{3}$$

where R_{ON} is the turn-ON resistance of one unit inverter cell. Therefore, the output frequency of the ring oscillator, which is the F_S of the converter ring, is given by

$$F_S \approx \frac{1}{Nt_d} = \frac{1}{\frac{R_{\mathrm{ON}}L_{\mathrm{TOT}}}{m}a + NR_{\mathrm{ON}}C_{\mathrm{LOGIC}}}. \tag{4}$$

As the targeted frequency is decided by the maximum output power and efficiency, by using (4) the phase number N and the inverter size m could be decided. Obviously, the length of the clock path sets the maximum achievable frequency. Fig. 11 shows the postlayout simulation results of the maximum achievable frequency versus different phase numbers with different inverter sizes. Adding inverters or delay cells will increase the total capacitance on the clock path and thus will decrease the frequency. When the frequency with a given phase number could not fulfill the output power requirement, the inverter size should be increased to meet the specification.

Thus, the design procedure of the converter ring is suggested as follows: 1) determine the maximum switching frequency with given chip area and maximum output power and 2) determine the phase number with acceptable ripple voltage and quiescent current.

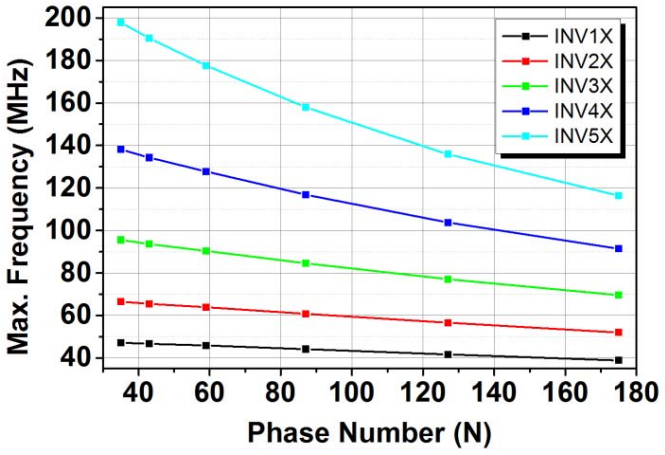

Fig. 11. Postlayout simulation results of the V_{DD}CO with parasitics on the ring.

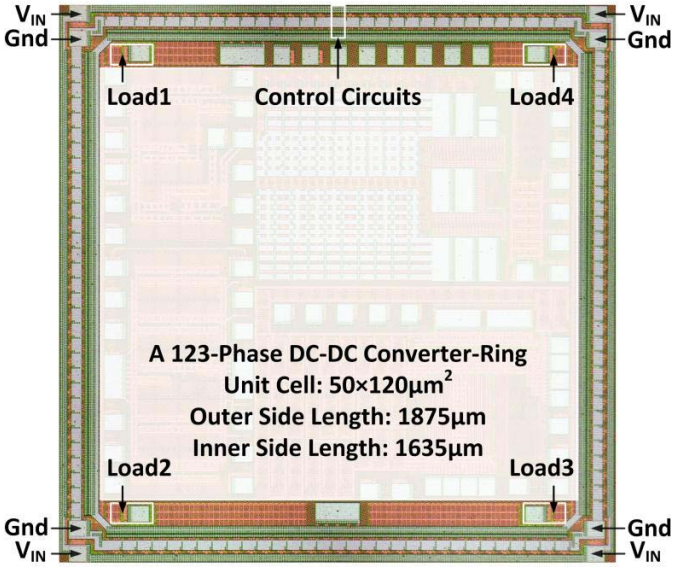

Fig. 12. Chip micrograph of the dc–dc converter ring.

IV. Converter Ring Implementations and Extensions

The first version of the converter-ring design [5] was implemented in a 65-nm CMOS process for microprocessor applications, as shown in Fig. 12. It has 30 power cells and one controller on the top edge and 31 power cells on the other three edges, forming a ring around the whole chip. Fig. 13 shows the measured load transient response, reference tracking, and output voltage ripple waveforms of the first converter-ring design. One on-chip load of 25 mA was placed at each corner of the chip to emulate the load transient events. With $V_{IN} = 2$ V, $V_{OUT} = 1.1$ V, $M = 2/3$ and for load transients between 10 and 110 mA, the output voltage variations are within 58 mV because of the designed high UGF. To accommodate the DVS function, reference tracking speed of 2.5 V/μs is demonstrated. The measured output ripples range from 2.2 to 30 mV, which are dominated by the phase mismatch at the chip corners. Also, the output ripple is a complicated function of load current and V_{OUT}/V_{IN} conditions [26].

Our second converter-ring design is used to power up an active-matrix light-emitting diode (AMLED) microdisplay system. The loading current is quite uniform across the whole chip and is a more suitable application for the proposed ring-shaped converter. A chip micrograph of the fully integrated converter ring driving the AMLED microdisplay is shown in Fig. 14. In such case, the supply ripples and *IR* drops can be well planned, while power can be evenly distributed to each pixel.

To further extend the idea of the ring-shaped converter, fine-grained voltage domains can be realized by cascading a step-down SC converter with low-dropout (for example, down to dropout voltage of 50-mV) regulators that use nMOS transistors as the power transistor, as shown in Fig. 15. Using nMOS as the power transistor has the benefits of intrinsic fast transient response and good power supply ripple rejection (PSRR). A simple EA design can be used [56] because the nMOS power stage is essentially a source follower. PSRR can be improved by adding a small capacitor (in pF level) to the gate of the power nMOS. For the EA of the nMOS-LDO regulator, only a small quiescent current (say 10 μA) needs to be drawn from the V_{IN} node, while the main current delivered to the load is drawn from the step-down converter output V_{DCDC} for high efficiency [56]. This FIVR solution with merged dc–dc converter and nMOS-LDO regulators could be a good tradeoff for efficiency, supply noise, and granularity.

If flipped-chip package or through silicon via technologies are selected for the targeted SoC design, an on-chip power converter grid could then be possibly conceived as shown in Fig. 16. With the V_{IN} and Gnd bumps or vias being distributed around the loads, the multiphase power cells can be distributed along the converter grid for better power delivery.

V. Discussion on SC DC–DC Converters

The proposed fast-response control loop design methodology presented in Section III can also be applied to typical multiphase SC converters of which the power cells are gregarious as shown in the left architecture of Fig. 8. The centralized architectures do have certain advantages, because they allow more complex and adaptive schemes to be integrated into the controller [53]–[61]. For example, switch resistance modulation or adaptive switch sizing could reduce the output ripple by controlling the peak current during charge transfer [53], [55], [57]–[59]. Another example is a dual-output SC converter that is realized by sharing the design margins of two SC converters for area reduction and efficiency optimization [61]. Since the power cells of the SC converter can be easily divided or combined, the SC converter is more compatible with digital control when compared to the inductor-based dc–dc converter [27], [56], [59], [61]. Nevertheless, instead of trying to reduce the output ripple with interleaving phases, an opposite way is to switch all the power cells simultaneously and to adapt the operation frequency of the digital load according to the supply ripple [62]. High system-level efficiency can then be achieved by removing the

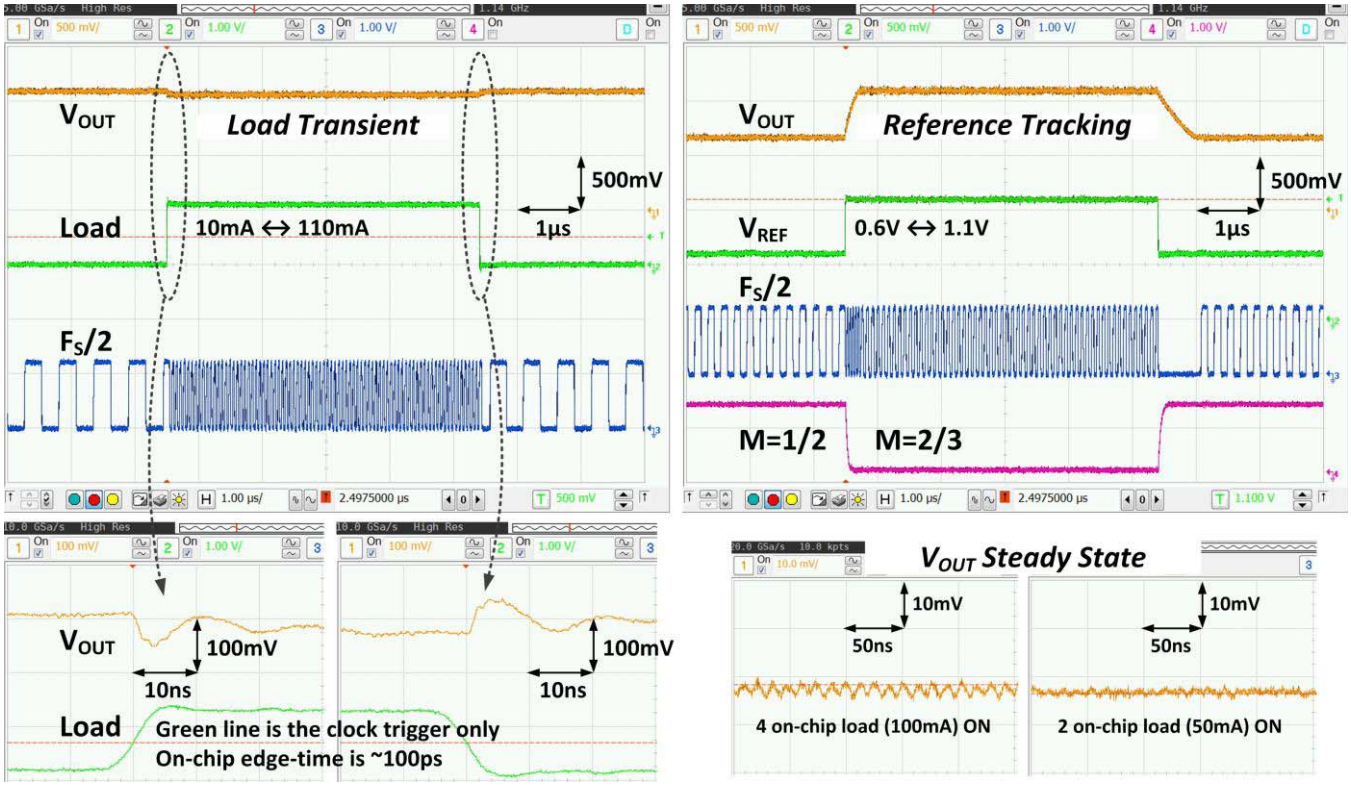

Fig. 13. Measured load transient response, reference tracking, and output voltage ripple waveforms of the converter ring.

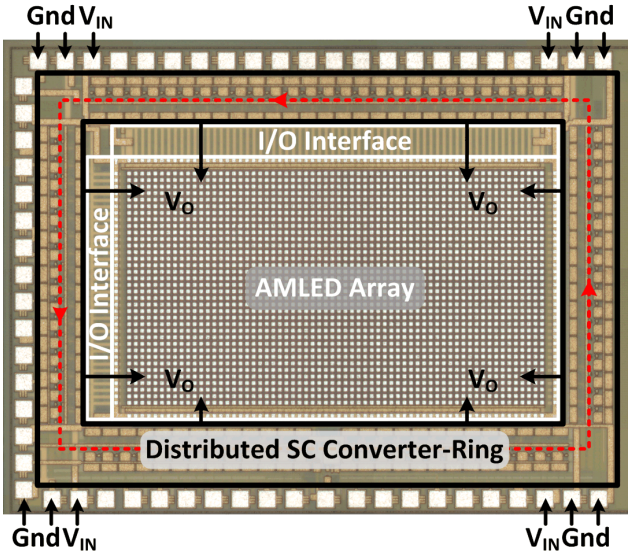

Fig. 14. Chip micrograph of proposed capacitive LED driver.

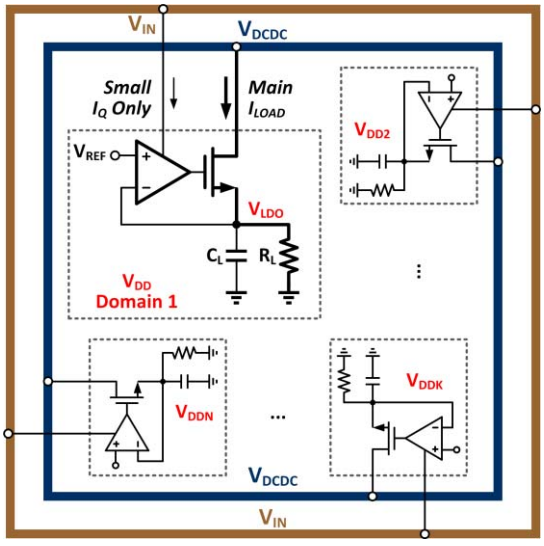

Fig. 15. Incorporate the converter-ring structure with cascaded nMOS-LDO regulator.

charge redistribution losses and by adapting the clock of the digital load, which requires a low-frequency ripple to allow for sufficient time for adaptation. Currently, this method could only be applied to drive fully digital loads, the behavior of which is adjustable to the supply ripple. For analog and noise-sensitive devices, low supply ripple is always desirable.

For low-cost designs using standard CMOS processes, the bottom-plate parasitic of MOS capacitors used as flying capacitors would significantly degrade the output power and efficiency. Therefore, for the SC converters in low-cost CMOS technologies, parasitic capacitors have to be taken good care of, by using topological and circuit-level techniques [47], [54], [63]–[65]. The parasitic junction capacitor can be reduced by limiting the charging/discharging current with a large blocking resistor [47], or by applying a large reverse bias voltage to the p-n junction [54], or by both [65].

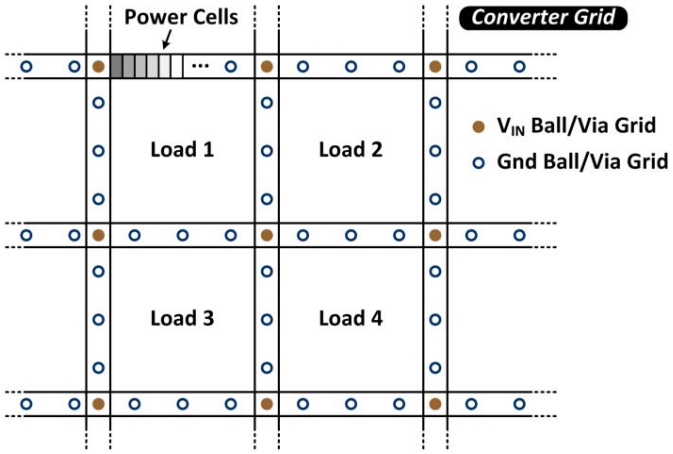

Fig. 16. Conceptual diagram of the on-chip power converter grid.

As the parasitic loss is proportional to the switching frequency, these improvements help the SC converter to operate at higher frequencies, therefore, increase the product of power density and efficiency and decrease the output ripple as well.

VI. Conclusion

This paper discusses and compares commonly used voltage regulators in power supply on-chip, which includes LDO regulators, SC converters, inductor-based converters, and hybrid converters. Several design considerations and suggestions on selecting the conversion topologies are provided. The design methodology of the multiphase SC converter could be quite similar to that of the linear regulator, because the multiphase SC power stage could response within a fraction of the switching period and can be considered as a first-order pseudocontinuous-time power stage. The dominant pole of the SC converter control loop could be set at the output node and thus the UGF can be designed to be a few times higher than its switching frequency. Moreover, a layout-oriented converter-ring design that powers up the loads from all directions is analyzed in detail with suggested design procedures to reach a near-optimum design solution. In addition, we found that the AMLED driver-array is a very suitable application for the proposed converter-ring structure, as it has a uniform load current across the whole chip.

There are pros and cons for the distributed and the centralized FIVRs. A multiphase SC converter with distributed power cells can provide better power delivery to the load, but may suffer from larger PVT variations among the power cells and consequently may result in larger output ripples. A centralized FIVR design could have more sophisticated control schemes, while the distributed fine-grained supply domains help individual blocks to enjoy a dedicated point-of-load supply.

References

[1] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[2] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[3] G. Villar-Piqué, H. J. Bergveld, and E. Alarcón, "Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4156–4167, Sep. 2013.

[4] M. Steyaert, F. Tavernier, H. Meyvaert, A. Sarafianos, and N. Butzen, "When hardware is free, power is expensive! Is integrated power management the solution?" in *Proc. 41st Eur. Solid-State Circuits Conf.*, Sep. 2015, pp. 26–34.

[5] Y. Lu *et al.*, "A 123-phase DC-DC converter-ring with fast-DVS for microprocessors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[6] R. Karadi, G. V. Piqué, and H. J. Bergveld, "Switched-capacitor power-converter topology overview and performance comparison," in *Wideband Continuous-Time* $\Sigma\Delta$ *ADCs, Automotive Electronics, and Power Management*. Cham, Switzerland: Springer, 2017, pp. 239–261.

[7] Y. Lu, "Digitally assisted low dropout regulator design for low duty cycle IoT applications," in *Proc. IEEE Asia–Pacific Conf. Circuits Syst. (APCCAS)*, Oct. 2016, pp. 33–36.

[8] S. T. Kim *et al.*, "Enabling wide autonomous DVFS in a 22 nm graphics execution core using a digitally controlled fully integrated voltage regulator," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 18–30, Jan. 2016.

[9] W.-J. Tsou *et al.*, "Digital low-dropout regulator with anti PVT-variation technique for dynamic voltage scaling and adaptive voltage scaling multicore processor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 338–339.

[10] G. Patounakis, Y. W. Li, and K. L. Shepard, "A fully integrated on-chip DC-DC conversion and power management system," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 443–451, Mar. 2004.

[11] Y. K. Ramadass and A. P. Chandrakasan, "Minimum energy tracking loop with embedded DC–DC converter enabling ultra-low-voltage operation down to 250 mV in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 256–265, Jan. 2008.

[12] M. Alioto, E. Consoli, and J. M. Rabaey, "'EChO' reconfigurable power management unit for energy reduction in sleep-active transitions," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1921–1932, Aug. 2013.

[13] H. Li *et al.*, "Energy-efficient power delivery system paradigms for many-core processors," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 36, no. 3, pp. 449–462, Mar. 2017.

[14] C. R. Sullivan, D. V. Harburg, J. Qiu, C. G. Levey, and D. Yao, "Integrating magnetics for on-chip power: A perspective," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4342–4353, Sep. 2013.

[15] H. K. Krishnamurthy *et al.*, "A digitally controlled fully integrated voltage regulator with on-die solenoid inductor with planar magnetic core in 14 nm tri-gate CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 336–337.

[16] M. Wens, K. Cornelissens, and M. Steyaert, "A fully-integrated 0.18 μm CMOS DC-DC step-up converter, using a bondwire spiral inductor," in *Proc. 33rd Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2007, pp. 268–271.

[17] G. Villar and E. Alarcon, "Monolithic integration of a 3-level DCM-operated low-floating-capacitor buck converter for DC-DC step-down donversion in standard CMOS," in *Proc. IEEE Power Electron. Specialists Conf. (PESC)*, Jun. 2008, pp. 4229–4235.

[18] C. Huang and P. K. T. Mok, "An 84.7% efficiency 100-MHz package bondwire-based fully integrated buck converter with precise DCM operation and enhanced light-load efficiency," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2595–2607, Nov. 2013.

[19] C. Huang and P. K. T. Mok, "A 100 MHz 82.4% efficiency package-bondwire based four-phase fully-integrated buck converter with flying capacitor for area reduction," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2977–2988, Dec. 2013.

[20] M. K. Song, M. F. Dehghanpour, J. Sankman, and D. Ma, "A VHF-level fully integrated multi-phase switching converter using bond-wire inductors, on-chip decoupling capacitors and DLL phase synchronization," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 1422–1425.

[21] G. Palumbo, D. Pappalardo, and M. Gaibotti, "Charge-pump circuits: Power-consumption optimization," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 11, pp. 1535–1542, Nov. 2002.

[22] W.-H. Ki, F. Su, and C.-Y. Tsui, "Charge redistribution loss consideration in optimal charge pump design," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 2. May 2005, p. 1895 1898.

[23] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[24] D. Somasekhar *et al.*, "Multi-phase 1 GHz voltage doubler charge pump in 32 nm logic process," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 751–758, Apr. 2010.

[25] G. V. Piqué, "A 41-phase switched-capacitor power converter with 3.8 mV output ripple and 81% efficiency in baseline 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 98–100.

[26] Y. Lu, J. Jiang, and W.-H. Ki, "A multiphase switched-capacitor DC–DC converter ring with fast transient response and small ripple," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 579–591, Feb. 2017.

[27] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A fully-integrated switched-capacitor step-down DC-DC converter with digital capacitance modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec. 2010.

[28] T. M. Van Breussegem and M. S. J. Steyaert, "Monolithic capacitive DC-DC converter with single boundary–multiphase control and voltage domain stacking in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1715–1727, Jul. 2011.

[29] Y. Lu, W.-H. Ki, and C. P. Yue, "Input-adaptive dual-output power management unit for energy harvesting devices," in *Proc. IEEE 55th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2012, pp. 1080–1083.

[30] W.-H. Ki *et al.*, "Analysis and design strategy of on-chip charge pumps for micro-power energy harvesting applications," in *VLSI-SoC: Advanced Research for Systems on Chip*. Berlin, Germany: Springer, 2012, pp. 158–186.

[31] S. Bang, D. Blaauw, and D. Sylvester, "A successive-approximation switched-capacitor DC–DC converter with resolution of $V_{\mathrm{IN}}/2^N$ for a wide range of input and output voltages," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 543–556, Feb. 2016.

[32] W. Jung *et al.*, "An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2800–2811, Dec. 2014.

[33] L. G. Salem and P. P. Mercier, "A recursive switched-capacitor DC-DC converter achieving 2^N-1 ratios with high efficiency over a wide output voltage range," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2773–2787, Dec. 2014.

[34] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.

[35] X. Liu, C. Huang, and P. K. T. Mok, "A 50 MHz 5 V 3 W 90% efficiency 3-level buck converter with real-time calibration and wide output range for fast-DVS in 65 nm CMOS," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2016, pp. 1–2.

[36] X. Liu, P. K. T. Mok, J. Jiang, and W.-H. Ki, "Analysis and design considerations of integrated 3-level buck converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 5, pp. 671–682, May 2016.

[37] X. Liu, H. Zhang, M. Zhao, X. Chen, P. K. T. Mok, and H. C. Luong, "A 2.4 V 23.9 dBm 35.7%-PAE −32.1 dBc-ACLR LTE-20 MHz envelope-shaping-and-tracking system with a multiloop-controlled AC-coupling supply modulator and a mode-switching PA," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 38–39.

[38] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[39] K. Kesarwani and J. T. Stauth, "Resonant and multi-mode operation of flying capacitor multi-level DC-DC converters," in *Proc. IEEE 16th Workshop Control Modeling Power Electron. (COMPEL)*, Jul. 2015, pp. 1–8.

[40] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "A resonant switched-capacitor IC and embedded system for sub-module photovoltaic power management," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3043–3054, Dec. 2012.

[41] K. Kesarwani, R. Sangwan, and J. T. Stauth, "A 2-phase resonant switched-capacitor converter delivering 4.3 W at 0.6 W/mm^2 with 85% efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 86–87.

[42] Y. Pascal and G. Pillonnet, "Efficiency comparison of inductor-, capacitor-, and resonant-based converters fully integrated in CMOS technology," *IEEE Trans. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 3, pp. 421–429, Sep. 2015.

[43] Q. Jin, X. Ruan, X. Ren, Y. Wang, Y. Leng, and C. K. Tse, "Series–parallel-form switch-linear hybrid envelope-tracking power supply to achieve high efficiency," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 244–252, Jan. 2017.

[44] R. Jain *et al.*, "A 0.45–1 V fully-integrated distributed switched capacitor DC-DC converter with high density MIM capacitor in 22 nm tri-Gate CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, Apr. 2014.

[45] T. M. Andersen *et al.*, "A sub-ns response on-chip switched-capacitor DC-DC voltage regulator delivering 3.7 W/mm^2 at 90% efficiency using deep-trench capacitors in 32 nm SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 90–91.

[46] T. M. Andersen *et al.*, "A feedforward controlled on-chip switched-capacitor voltage regulator delivering 10 W in 32 nm SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 362–363.

[47] H.-P. Le, J. Crossley, S. R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19 W/mm^2 at 73% efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 372–373.

[48] Y. Lu, Y. Wang, Q. Pan, W.-H. Ki, and C. P. Yue, "A fully-integrated low-dropout regulator with full-spectrum power supply rejection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 707–716, Mar. 2015.

[49] X. Zhou, P.-L. Wong, P. Xu, F. C. Lee, and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, Nov. 2000.

[50] A. R. Brown and R. D. Middlebrook, "Sampled-data modeling of switching regulators," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 1981, pp. 349–369.

[51] Y. Qiu, K. Yao, Y. Meng, M. Xu, F. C. Lee, and M. Ye, "Control-loop bandwidth limitations for multiphase interleaving buck converters," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, vol. 2. Feb. 2004, pp. 1322–1328.

[52] S. Xiao, W. Qiu, G. Miller, T. X. Wu, and I. Batarseh, "Adaptive modulation control for multiple-phase voltage regulators," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 495–499, Jan. 2008.

[53] R. Jain, S. T. Kim, V. Vaidya, K. Ravichandran, J. W. Tschanz, and V. De, "Conductance modulation techniques in switched-capacitor DC-DC converter for maximum-efficiency tracking and ripple mitigation in 22 nm tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1809–1819, Aug. 2015.

[54] J. Jiang, Y. Lu, C. Huang, W.-H. Ki, and P. K. T. Mok, "A 2-/3-phase fully integrated switched-capacitor DC-DC converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 366–367.

[55] J. Jiang, W.-H. Ki, and Y. Lu, "Digital 2-/3-phase switched-capacitor converter with ripple reduction and efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1836–1848, Jul. 2017.

[56] Y. Lu, W.-H. Ki, and C. P. Yue, "An NMOS-LDO regulated switched-capacitor DC–DC converter with fast-response adaptive-phase digital control," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1294–1303, Feb. 2016.

[57] H. Lee and P. K. T. Mok, "An SC voltage doubler with pseudo-continuous output regulation using a three-stage switchable opamp," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1216–1229, Jun. 2007.

[58] F. Su, W.-H. Ki, and C.-Y. Tsui, "Regulated switched-capacitor doubler with interleaving control for continuous output regulation," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1112–1120, Apr. 2009.

[59] S. S. Kudva and R. Harjani, "Fully integrated capacitive DC–DC converter with all-digital ripple mitigation technique," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1910–1920, Aug. 2013.

[60] C. Zheng, I. Chowdhury, and D. Ma, "Low-noise switched-capacitor power converter with adaptive on-chip surge suppression and preemptive timing control," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5174–5182, Nov. 2013.

[61] J. Jiang, Y. Lu, W.-H. Ki, S.-P. U, and R. P. Martins, "A dual-symmetrical-output switched-capacitor converter with dynamic power cells and minimized cross regulation for application processors in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 344–345.

[62] B. Zimmer *et al.*, "A RISC-V vector processor with simultaneous-switching switched-capacitor DC–DC converters in 28 nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 930–942, Apr. 2016.

[63] H. Meyvaert, T. Van Breussegem, and M. Steyaert, "A 1.65 W fully integrated 90 nm bulk CMOS capacitive DC-DC converter with intrinsic charge recycling," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4327–4334, Sep. 2013.

[64] N. Butzen and M. Steyaert, "A 94.6%-efficiency fully integrated switched-capacitor DC-DC converter in baseline 40 nm CMOS using scalable parasitic charge redistribution," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 220–221.

[65] N. Butzen and M. Steyaert, "A 1.1 W/mm^2-power-density 82%-efficiency fully integrated 3:1 switched-capacitor DC-DC converter in baseline 28 nm CMOS using stage outphasing and multiphase soft-charging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 178–179.

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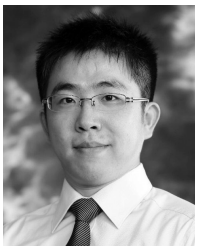

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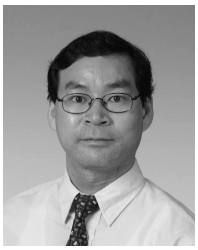

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