A Highly-Scalable Analog Equalizer Using a Tunable and Current-Reusable Active Inductor for 10-Gb/s I/O Links

Yong Chen, Pui-In Mak, and Yan Wang

***Abstract*— A 0.0015-mm^2 1.28-mW single-branch analog equalizer is demonstrated in 65-nm CMOS for 10-Gb/s input/output links. Instead of using passive inductors that are untunable and unscalable with technologies, gain compensation here is optimized via a tunable and current-reusable active inductor (AI). This AI incorporates a positive-feedback impedance converter with only two MOSFETs and one MOS varactor. Together with the use of: 1) negative Miller capacitors to optimize the pole-zero composition and 2) tunable resistive source degeneration to adjust the low-frequency losses, the analog equalizer recovers an eye-opening rate of minimally 30% up to 10 Gb/s over a pair of 60-cm FR4 microtrip traces. The data Pk-to-Pk jitter is <24 ps, and the RMS jitter is <4 ps, over a number of pseudorandom bit sequence patterns (2^7–1, 2^{15}–1, and 2^{31}–1).**

***Index Terms*— Active inductor, analog equalizer, CMOS, eye-opening rate, jitter, negative Miller capacitor, positive-feedback.**

I. Introduction

High-speed input/output (I/O) links over low-cost FR4 printed circuit boards (PCBs) [1] suffer from frequency-dependent channel loss due to the skin effect and dielectric loss. A response-tunable amplifier, matching the inverse response of the channel-loss profile, can serve as the equalizer to optimize the eye opening. Most analog equalizers, such as [2], were based on a pseudodifferential common-source amplifier with resistive-capacitive source degeneration, and passive inductors at the outputs for gain-peaking and bandwidth enhancement. The former technique can easily incorporate tunable elements (e.g., MOS resistor and varactor) to control the low-frequency losses. For the high-frequency response, however, the latter is hard to be tuned, and is increasingly costly in nanoscale CMOS for its area impact, particularly in multistage designs.

Although passive equalizers [3] seem more power efficient, the single-pole single-zero response is limited to slow roll-off compensation. Moreover, the pole-zero tuning can mainly rely on switched-capacitor banks that are bulky in size and cannot offer continuous tuning for optimal performance.

This brief describes a 65-nm CMOS analog equalizer with continuously tunable low-/high-frequency responses achieved by merging resistive source degeneration and active inductor (AI) techniques in one branch. The presented AI enables wide and continuous tuning of high-frequency complex poles by a voltage signal, simplifying the system-level adaptation while minimizing the die area and parasitics. The equalizer also measures more favorable figure of merit (FOM), area and power efficiencies than the state of the art. The principles of positive-feedback impedance converter (PFIC) for realizing an AI is described in Section II. The proposed analog equalizer embedded such an AI is described in Section III, followed by the experimental results in Section IV.

Manuscript received August 17, 2013; revised April 12, 2014; accepted April 16, 2014. Date of publication May 9, 2014; date of current version April 22, 2015. This work was supported in part by the National 973 Program of China, in part by the National 863 Program of China, in part by the University of Macau under Grant MYRG114 (Y1-L4)-FST13-MPI, and in part by the Macau Science and Technology Development Fund.

Y. Chen and Y. Wang are with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China (e-mail: chenyong@ieee.org; wangy46@tsinghua.edu.cn).

P.-I. Mak is with the State-Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau, China (e-mail: pimak@umac.mo).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2014.2318733

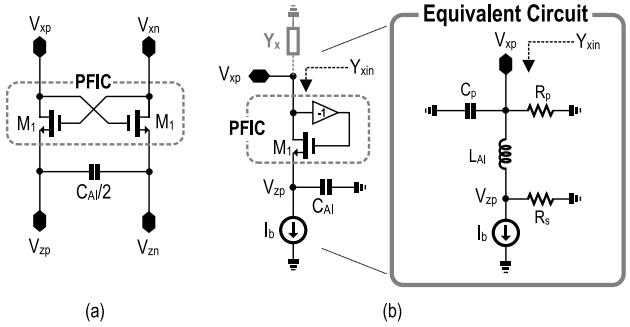

Fig. 1. (a) Differential PFIC-based AI that can be merged with another circuitry to work under the same bias current. (b) Half-circuit equivalent showing the transformed admittance ($Y_{\rm xin}$) from $V_{\rm xp}$ looks into the PFIC, where $V_{\rm zp}$ is terminated with a current source $I_{\rm b}$.

II. PFIC-Based AI

Conventional AIs were mainly relied on active or passive negative-feedback circuits [4], [5] and can involve extra power [6]. Thus, their area and power efficiencies are generally low, because a high self-resonant frequency demands a sufficient bias current to overcome the parasitic effects induced by the AI. Recently, it has been revealed that a differential AI could be more effectively emulated via a PFIC, especially for analog circuits, such as filters [7]. This brief studies, for the first time, the versatility of PFIC-based AI in the 10-GHz range, using a mainstream 65-nm CMOS process.

One possible topology of PFIC-based AI is shown in Fig. 1(a). A pair of MOSFETs (M_1) with cross-diode connection can transfer the capacitive effect of $C_{\rm AI}/2$ at $V_{\rm zp,n}$, into an inductive one at $V_{\rm xp,n}$. This AI topology enjoys a number of merits: 1) easy and wide inductance tunability if $C_{\rm AI}$ is a MOS varactor, which has a high Q-factor in nanoscale CMOS; 2) high self- resonant frequency because of no inner parasitic poles; and 3) power efficient because it can be merged into the main circuit to reuse the bias current and avoid extra V–I and I–V conversions.

To understand the admittance transfer characteristics of the AI, its half-circuit equivalent model is studied, as shown in Fig. 1(b). With $V_{\rm zp}$ terminated by an ideal current source $I_{\rm b}$, the input admittance ($Y_{\rm xin}$) at $V_{\rm xp}$ can be derived

$$Y_{\rm xin} \cong \frac{1}{R_{\rm p}} + sC_{\rm p} + \frac{1}{s}L_{\rm AI} + R_{\rm s}. \quad (1)$$

TABLE I
L_{AI} AND f_{SR} WITH RESPECT TO THE SIZE OF C_{AI}

C_{AI} (fF)	50	100	200	400	600
L_{AI} (nH)	29	33.5	47.5	77.5	106
f_{SR} (GHz)	11.3	8.75	6.6	4.73	4

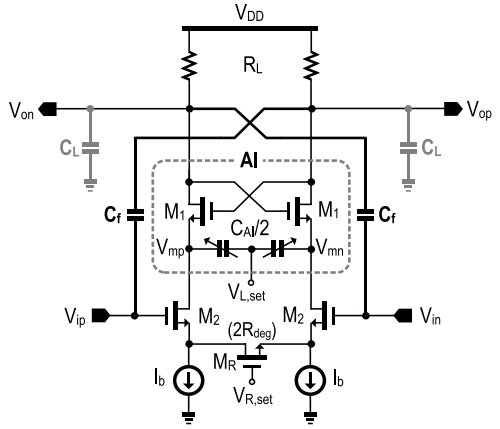

Fig. 2. Proposed analog equalizer with a tunable current-reusable AI.

Assuming $C_{AI} \gg C_{gs1}$ and $g_{m1} \gg g_{o1}$, the parameters in (1) can be expressed as

$$\begin{aligned} R_p &= -\frac{(C_{AI}+C_{gs1})^2}{(C_{AI}+2C_{gs1})(C_{AI}g_{m1}-C_{AI}g_{o1}-2C_{gs1}g_{o1})} \\ &\cong -\frac{1}{g_{m1}} - g_{o1} \\ C_p &= \frac{C_{AI}C_{gs1}}{C_{AI}+C_{gs1}} + 4C_{gd1} \\ L_{AI} &= \frac{(C_{AI}+C_{gs1})^3}{(C_{AI}+2C_{gs1})(C_{AI}g_{m1}-C_{AI}g_{o1}-2C_{gs1}g_{o1})(g_{m1}+g_{o1})} \\ &\cong \frac{C_{AI}}{g_{m1}^2} \\ R_s &= \frac{(C_{AI}+C_{gs1})^2}{(C_{AI}+2C_{gs1})(C_{AI}g_{m1}-C_{AI}g_{o1}-2C_{gs1}g_{o1})} \\ &\cong \frac{1}{g_{m1}-g_{o1}}. \end{aligned} \tag{2}$$

The symbols g_{m1}, g_{o1}, C_{gs1}, and C_{gd1} denote the transconductance, output conductance, and gate-source and gain-drain capacitances of M_1, respectively. To ensure stability, the positive resistance ($1/Y_x$) at $V_{xp,n}$ must be larger than $-1/(g_{m1}-g_{o1})$. The simulated L_{AI} and its self-resonant frequency (f_{SR}) with respect to the size of C_{AI} are summarized in Table I. Hence, with a MOS varactor to realize a tunable C_{AI} in the range of 50 to 100 fF, gain peaking at the 10-GHz range is feasible in the 65-nm CMOS technology node, with M_1 (10/0.06 μm) biased at 400 μA.

III. SINGLE-BRANCH ANALOG EQUALIZER WITH AN AI

Fig. 2 shows the schematic of the proposed single-branch analog equalizer. Its basis is a pseudodifferential common-source amplifier (M_2) with resistive load (R_L). The output gain boost is based on the described AI (M_1 and $C_{AI}/2$), which befits the use of a nMOS input stage, creating an inductive effect to the outputs ($V_{op,n}$) to drive the capacitive load (C_L). The impedance at $V_{mp,n}$ can be sized to accommodate the parasitic capacitance of C_{AI}, while R_L can be sized to ensure the stability at $V_{op,n}$. The AI, with a MOS varactor for $C_{AI}/2$, also allows easy-tuning of inductance via a voltage control signal ($V_{L,set}$), which is much more convenient and area efficient than the use of capacitor banks [3]. Moreover, the intensity of the gain boost can be tuned to facilitate circuit adaptation in the system level, being insensitive to the channel-loss variations. Since M_1 is stacked atop M_2, current reuse is attained with acceptable voltage-headroom consumption, while improving the reverse isolation. This act also avoids any high-impedance inner node that otherwise degrades the signal bandwidth.

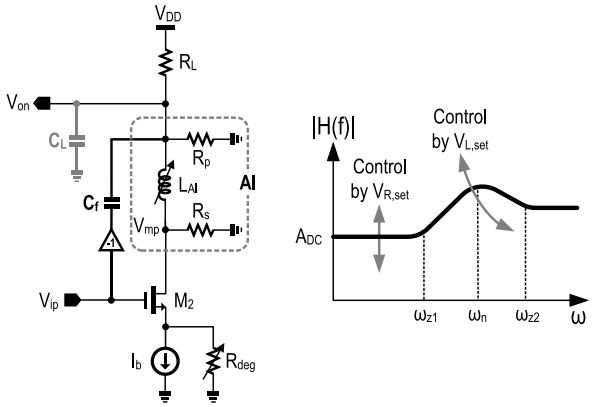

Fig. 3. Single-ended equivalent circuit of the analog equalizer.

To compensate the voltage headroom consumed by the AI, the V_{DD} was elevated from 1.2 to 1.5 V like other high-voltage-enabled circuits [8]. The operating voltages (V_{GS}, V_{GS}, and V_{DS}) of each device was monitored by the node-voltage trajectory diagrams extracted from transient simulations, ensuring there is no risk on device reliability at all time. Together with the negative Miller capacitors (C_f) and the tunable source degeneration resistor (M_R), the poles and zeros can be adjusted (or adapted) to tune the frequency response with respect to the channel-loss profile.

To effectively analyze the transfer function, only the gate-source capacitance of the MOSFET is considered. The circuit parameters (L_{AI}, R_p, and R_s) in its equivalent circuit (Fig. 3) are substituted from Fig. 1(b). The derived transfer function is written as

$$H(s) = A_{dc}\frac{s^2b_2 + sb_1 + 1}{s^2a_2 + sa_1 + 1} \tag{3}$$

where

$$\begin{aligned} A_{dc} &= \frac{g_{m2}R_s}{(1+g_{m2}R_{deg})\left(\frac{R_s}{R_L}+\frac{R_s}{R_p}+1\right)} \\ &\cong \frac{g_{m2}R_s}{1+g_{m2}R_{deg}} \\ b_2 &\cong \frac{C_{AI}C_f(1+g_{m2}R_{deg})}{g_{m1}g_{m2}} \\ b_1 &= \frac{C_f(1+g_{m2}R_{deg})}{g_{m2}} \\ a_2 &\cong \frac{C_{AI}(C_L+C_f)}{g_{m1}/R_L} \\ a_1 &\cong \frac{C_{AI}\left(\frac{1}{R_L}-g_{m1}\right)+(C_L+C_f)g_{m1}}{g_{m1}/R_L}. \end{aligned} \tag{4}$$

The dc gain (A_{dc}) is tunable by $V_{R,set}$, and the locations of the poles and zeros can be adjusted via $V_{R,set}$ and $V_{L,set}$. C_f is to optimize the pole-zero location computationally as it affects all coefficients and is realized as a MOSCAP to reduce its area and parasitic impacts. From the coefficients b_2 and b_1 in (4), it is easy to calculate the two zeros (ω_{z1} and ω_{z2}) using

$$\omega_{z1,z2} = \frac{-b_1 \pm \sqrt{b_1^2 - 4b_2}}{2b_2}. \tag{5}$$

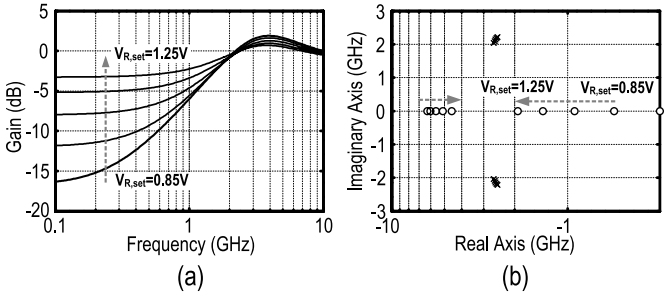

Fig. 4. Simulated (a) gain response and (b) pole-zero plot with $V_{R,\text{set}}$ swept from 0.85 to 1.25 V.

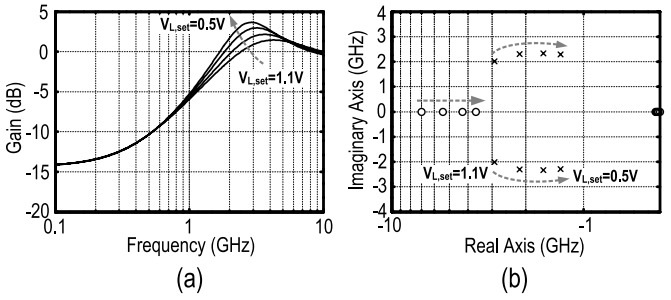

Fig. 5. Simulated (a) gain response and (b) pole-zero plot with $V_{L,\text{set}}$ swept from 0.5 to 1.1 V.

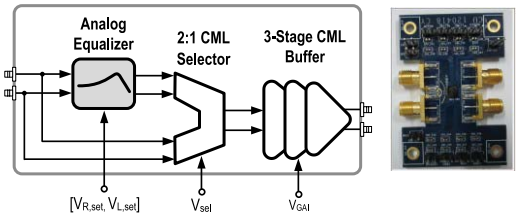

Fig. 6. Experimental setup for measuring the analog equalizer.

They should be sized as real zeros with different magnitudes, and can be widely tunable via R_{deg}. These conditions require

$$\frac{C_f}{C_{\text{AI}}} > \frac{4g_{\text{m2}}}{g_{\text{m1}}\left(1+g_{\text{m2}}R_{\text{deg}}\right)}. \tag{6}$$

For the two poles, they should be in complex conjugate and widely tunable via $V_{L,\text{set}}$. According to the coefficients a_2 and a_1 in (4), the complex-pole frequency (ω_n) and Q are given by

$$\omega_n = \sqrt{\frac{g_{\text{m1}}/R_L}{C_{\text{AI}}(C_L+C_f)}}, \quad Q = \frac{\sqrt{\frac{C_{\text{AI}}(C_L+C_f)}{g_{\text{m1}}/R_L}}}{(C_L+C_f)R_L - C_{\text{AI}}\left(R_L - \frac{1}{g_{\text{m1}}}\right)}. \tag{7}$$

Clearly, both ω_n and Q are function of the tunable element $1/\sqrt{C_{\text{AI}}}$. An optimal Q for the high-frequency response can minimize the phase distortion in the eye diagram [11]. From simulations, the tunability of the low-frequency losses (~18 dB) via $V_{R,\text{set}}$ (0.85 to 1.25 V) is shown in Fig. 4(a). For the loci of the poles and zeros, they are plotted in Fig. 4(b) showing the variability trends. ω_n is insensitive to $V_{R,\text{set}}$ as expected, but still have 1 to 2 dB gain variation at high frequency. Thus, $V_{L,\text{set}}$ offers the freedom to finely adjust the high-frequency response without affecting the low-frequency one, such that the overall equalization can be optimized. Here, 2 to 3 dB continuous gain tunability offered by $V_{L,\text{set}}$ is adequate. The gain responses and

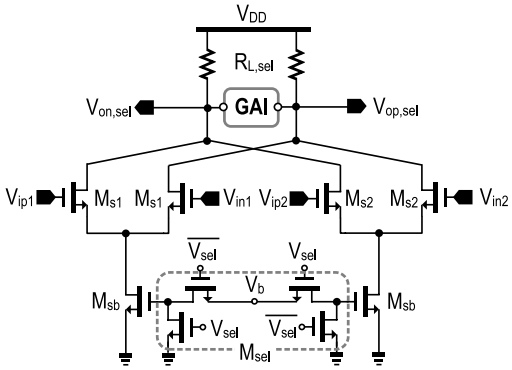

Fig. 7. 2:1 CML selector with an embedded GAI.

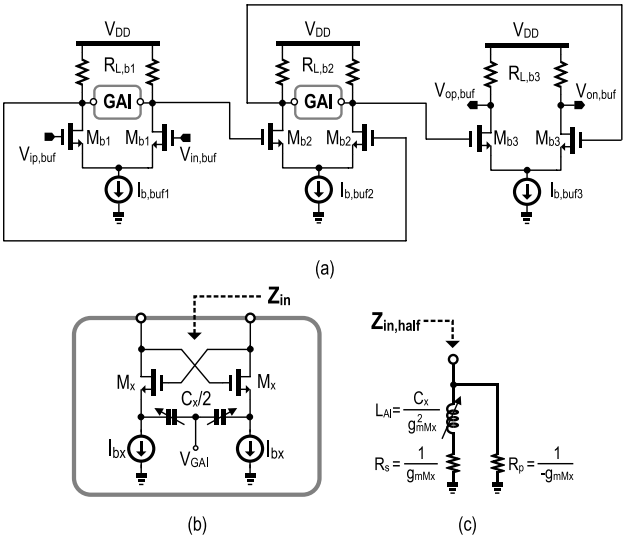

Fig. 8. (a) Three-stage CML buffer with embedded two GAIs in the first and second stages. (b) Schematic of the GAI. (c) Half-circuit equivalent.

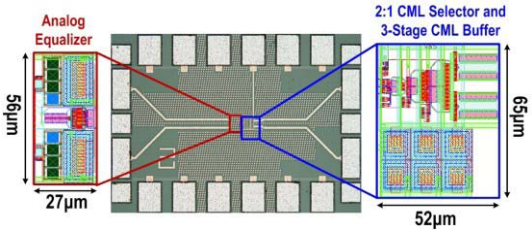

Fig. 9. Die micrograph and zoomed views of the core layouts.

loci of the poles and zeros with respect to $V_{L,\text{set}}$ (0.5 to 1.1 V) are plotted in Fig. 5(a) and (b), respectively, where $V_{R,\text{set}}$ is set as 0.9 V. The low-frequency zeros are almost unaffected by $V_{L,\text{set}}$. In the system level, a proper $V_{R,\text{set}}$ should be set first before adapting $V_{L,\text{set}}$ to optimize the performance.

IV. Experimental Setup and Measurement Results

To aid testing at the 10-Gb/s range, a 2:1 current-mode-logic (CML) selector and a three-stage CML buffer were integrated with the analog equalizer, as shown in Fig. 6. Both were designed not contributing the equalization, but just boosting the output swing for high-speed testability on PCB. Confirmed by postlayout simulations, the buffer's output essentially shows the data jitter and eye opening of the core equalizer. The data-input with different pseudorandom bit sequence (PRBS) patterns and dc bias voltages are provided by the

TABLE II
DEVICE SIZES OF THE REALIZED ANALOG EQUALIZER

M_1	10/0.06 (μm)	C_f	0.16 pF
M_2	30/0.06 (μm)	C_{AI}	2/1 (μm) x 10
M_R	0.8/0.06 (μm)	R_L	511 Ω
I_b	0.426 mA		

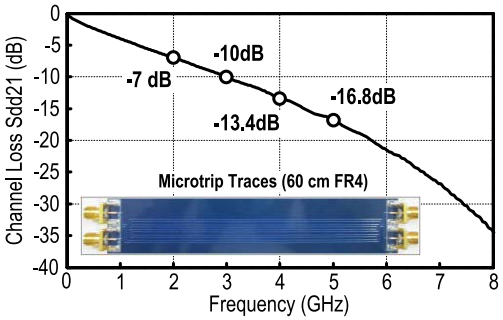

Fig. 10. Channel loss profile (Sdd21) of a pair of 60-cm microstrip traces.

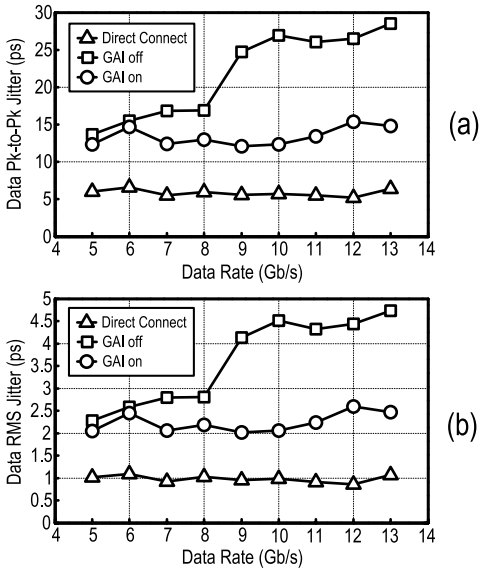

Fig. 11. Measured performances of the 2:1 CML selector plus three-stage CML buffer with the GAI ON/OFF. Direct connect means just equipment to equipment. (a) Data Pk-to-Pk jitter. (b) RMS jitter.

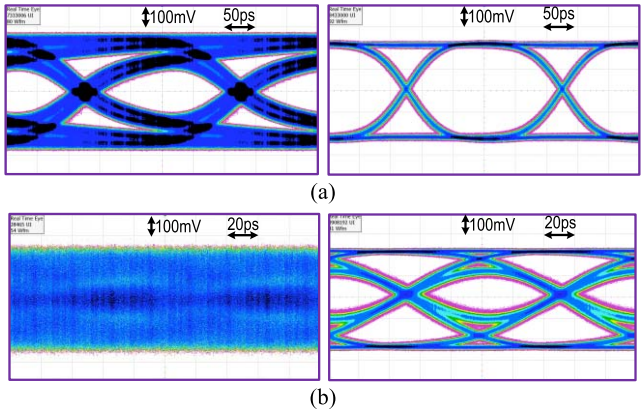

Fig. 12. Measured eye diagrams (left) before and (right) after equalization at (a) 4 Gb/s and (b) 10 Gb/s under an input signal with PRBS of 2^{31}–1.

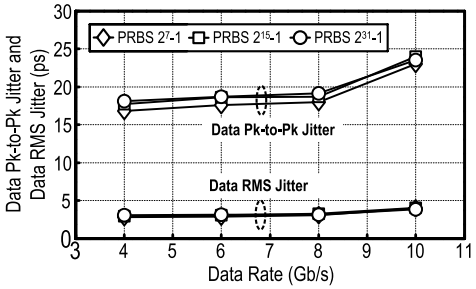

Fig. 13. Measured data Pk-to-Pk jitter and RMS jitter versus data rate under different PRBS.

$$\text{Eye Opening Rate} = \frac{\text{Eye Opening Height (mV)}}{\text{Eye } V_{\text{pk}-\text{to}-\text{pk}} \text{ (mV)}}$$

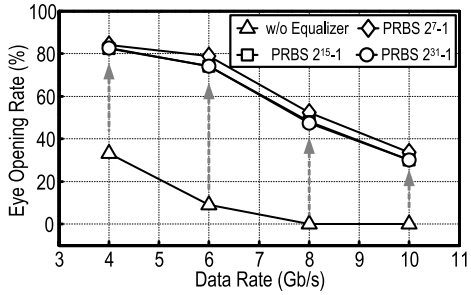

Fig. 14. Measured data eye-opening rate before and after equalization under different PRBS.

J-BERT N4903B. The jitter and output eye diagrams were captured via the DSA91304A oscilloscope.

The schematics of the 2:1 CML selector and three-stage CML buffer are shown in Figs. 7 and 8(a), respectively. Both were embedded with grounded AIs (GAIs) [Fig. 8(b)], under the same principle of the PFIC as described in Section II. However, to maximize the voltage swing and allow ON/OFF control, all GAI are not current reuse. The GAI is equivalent to a passive network [Fig. 8(c)] with a negative resistor in parallel with a tunable lossy inductance useful for bandwidth extension.

The analog equalizer and its test circuitries were fabricated in 65-nm CMOS. The die micrograph is shown in Fig. 9, where the analog equalizer occupies an active area of just 0.0015 mm^2. The device sizes are summarized in Table II. Thanks to the single-branch structure of the proposed equalizer having no high-impedance inner node, and the improved parasitics of the technology, a small I_b of 0.426 mA is already adequate for 10-Gb/s equalization. Thus, as long as the output swing is adequate to properly drive the back-end circuitry, such as the D-flip flop for DFE, the proposed equalizer can be more power and area efficient, while easing the tuning of high-frequency complex poles for optimal equalization.

The parasitic inductance due to the I/O is reduced to ∼600 pH by a parallel use of two bondwires, whereas the corresponding I/O bond pad adds ∼120-fF parasitic capacitance. The chip is mounted onto a FR4 PCB for chip-on-board tests with a pair of experimental 60-cm microstrip traces (width: 8 mils, spacing: 30 mils), which were sized with a differential characteristic impedance of 100 Ω. The measured channel-loss profile, including the effect of the SMA connectors, is plotted in Fig. 10. The key reference point is at 5 GHz, where the channel loss is −16.8 dB.

The 2:1 CML selector and three-stage CML buffer with the GAI ON/OFF are measured first. For an input PRBS of 2^7–1, the 2:1 CML

TABLE III
CHIP SUMMARY AND BENCHMARK WITH THE PRIOR ART

	JSSC'07 [11]	A-SSCC'07 [12]	EL'09 [9]	TCAS-II'09 [10]	ISCAS'11 [13]	This Work
CMOS Technology	0.13 µm	0.18 µm	0.13 µm	0.13 µm	45 nm	65 nm
Voltage Supply (V)	1.2	1.8	1.2	1.2	1.1	1.5
Power (mW)	25	34.2	6	14	8	**1.28**
Channel Loss (dB)	21.0 @ 5 GHz	16.7 @ 5 GHz	14.0 @ 5 GHz	20.0 @ 5 GHz	28.0 @ 6 GHz	16.8 @ 5 GHz
Inductor Type *	Passive	Passive	Active	no	no	Active
Active Area (mm^2)	0.162	1.1008	0.0065	0.129	0.009	**0.0015**
Data Rate (Gb/s)	10	10	10	10	12	10
Data Pk-to-Pk Jitter (ps)	24.0 *	50	/	40.0	29.0	23.0
Data RMS Jitter (ps)	/	/	4.0	/	/	3.94
FOM #	4.5	2.0	8.4	7.1	37.7	**54.0**

* Extracted value from plot. # the channel loss is based on 5 GHz, except [13] that is based on 6 GHz

selector and three-stage CML buffer totally induce a data Pk-to-Pk jitter <15 ps [Fig. 11(a)], and a RMS jitter <2.6 ps [Fig. 11(b)], up to 13-Gb/s input data. These results confirm the capability of them in characterizing the proposed analog equalizer up to 10 Gb/s.

The analog equalizer has an in-band attenuation of −8.3 dB (simulation) but it is uncritical to the equalization performances [3], such as the jitter and eye opening. Yet, in the system level, the output signal swing should be cooptimized with the sensitivity of its back-end circuitry, being the major concern of this equalizer when comparing with the existing approaches. The eye diagram before and after equalization at 4 Gb/s [Fig. 12(a)] and 10 Gb/s [Fig. 12(b)] were recorded under an input data PRBS of 2^{31}–1. Both the input and output signal swings are ∼400 mV_{pp} (i.e., around 150 mV_{pp} at the output of the equalizer), which is large enough to measure the data against the environmental and equipment noises. The data Pk-to-Pk jitter (16–24 ps) and RMS jitter (3–4 ps) under 4–10 Gb/s, for a number of PRBS patterns (2^7–1, 2^{15}–1, and 2^{31}–1), are plotted in Fig. 13. The eye-opening rate is minimally 30% up to a 10-Gb/s data rate (Fig. 14).

The chip summary and performance benchmark with [9]–[13] are given in Table III. The FOM [13] is given by (Data Rate × Channel Loss)/Power. This brief is favorable for its improved FOM, power and area efficiencies.

V. CONCLUSION

A 10-Gb/s single-branch analog equalizer has been reported. It features a tunable and current-reusable AI based on PFIC, measuring high area (0.0015 mm^2) and power (1.28 mW) efficiencies in 65-nm CMOS. The easy tunability of the AI and resistive-source degeneration allows the intensity of the low-frequency loss and high-frequency gain to be optimized. These beneficial features render this brief a superior analog equalizer candidate for cost and power reduction of wireline systems in expensive nanoscale CMOS.

ACKNOWLEDGMENT

The authors would like to thank S. Yang for assistance and Agilent Open Lab for measurement support.

REFERENCES

[1] A. Palaniappan and S. Palermo, "A design methodology for power efficiency optimization of high-speed equalized-electrical I/O architectures," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 8, pp. 1421–1431, Aug. 2013.

[2] J. Lee, "A 20-Gb/s adaptive equalizer in 0.13-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2058–2066, Sep. 2006.

[3] M. Hossain and A. C. Carusone, "7.4 Gb/s 6.8 mW source synchronous receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1337–1348, Jun. 2011.

[4] M. Maeng *et al.*, "0.18-μm CMOS equalization techniques for 10-Gb/s fiber optical communication links," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 11, pp. 3509–3519, Nov. 2005.

[5] J. Chen, F. Saibi, J. Lin, and K. Azadet, "Electrical backplane equalization using programmable analog zeros and folded active inductors," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 7, pp. 1459–1466, Jul. 2007.

[6] H. Lee *et al.*, "A 16 Gb/s/link, 64 Gb/s bidirectional asymmetric memory interface," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1235–1247, Apr. 2009.

[7] A. Pirola, A. Liscidini, and R. Castello, "Current-mode, WCDMA channel filter with in-band noise shaping," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1770–1780, Sep. 2010.

[8] P.-I. Mak and R. P. Martins, "High-/mixed-voltage RF and analog CMOS circuits come of age," *IEEE Circuits Syst. Mag.*, vol. 10, no. 4, pp. 27–39, Dec. 2010.

[9] D. Lee, J. Han, G. Han, and S. M. Park, "10 Gbit/s 0.0065 mm^2 6 mW analogue adaptive equaliser utilising negative capacitance," *Electron. Lett.*, vol. 45, no. 17, pp. 863–865, Aug. 2009.

[10] J.-H. Lu, K.-H. Chen, and S.-I. Liu, "A 10-Gb/s inductorless CMOS analog equaliser with an interleaved active feedback topology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 2, pp. 97–101, Feb. 2009.

[11] S. Gondi and B. Razavi, "Equalization and clock and data recovery techniques for 10-Gb/s CMOS serial-link receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1999–2011, Sep. 2007.

[12] J.-H. Lu, C.-L. Luo, and S.-I. Liu, "A passive filter for 10-Gb/s 0.18-μm CMOS technology," in *Proc. IEEE A-SSCC*, Nov. 2007, pp. 404–407.

[13] M. Ganzerli, L. Larcher, S. Erba, and D. Sanzogni, "An inductor-less 13.5-Gbps 8-mW analog equalizer for multi-channel multi-frequency operation," in *Proc. IEEE ISCAS*, May 2011, pp. 189–192.