A 4-b 7-μW Phase Domain ADC With Time Domain Reference Generation for Low-Power FSK/PSK Demodulation

Xuewei Lei, Chi-Hang Chan, *Member, IEEE*, Yan Zhu, *Senior Member, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

***Abstract*— This paper presents a 4-b phase-domain analog-to-digital converter (ADC) that utilizes the time-domain reference generation scheme for low-power operation. Rather than prior arts that rely on power-hungry resistive/current combiners or the IQ-assisted binary-search algorithm with large power T&H circuits for the reference generation, this design benefits from the fully dynamic power characteristic of the time-domain operation, thus leading to an energy-efficient phase ADC design. By introducing several on-chip calibration techniques, the design achieves good robustness with the proposed time-domain operation. The prototype is fabricated in the standard 65-nm CMOS technology, achieving an ENOB of 3.42 bits at 1 MS/s with near Nyquist input, while dissipating 7 μW from a 1-V supply. It leads to a 1.36-pJ/conversion-step Walden Figure of Merit at Nyquist input (FoM@Nyquist).**

***Index Terms*— Bluetooth low energy (BLE), frequency-shift keying (FSK), low power, phase ADC.**

I. Introduction

WEARABLE and portable devices are going to take part and become the major participant in Internet of Things (IoT) systems. In order to extend the battery life and meet the IoT standard, the ultra-low power consumption becomes a key feature. Bluetooth Low Energy (BLE) is a promising solution for the information linking in IoT applications as it consumes a relatively low power compared with other technologies [1]–[3]. The adopted modulation scheme in the BLE system is Gaussian Frequency-Shift Keying (GFSK), which is widely used in low-cost and short-range applications due to its spectral efficiency and constant envelope property [4], [5].

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In Frequency-Shift Keying (FSK) demodulation, the phase signal is extracted from the baseband in-phase signal I and the quadrature signal Q. Conventionally, I and Q signals are quantized by two amplitude analog-to-digital converters (IQ ADCs), and the subsequent demodulation is processed in the digital domain [6]–[9]. According to [10], the IQ ADC needs extra 0.49 bit to accommodate a non-constant vector magnitude of the phase input; otherwise, an automatic gain control (AGC) is needed to trim the magnitude of the vector. An alternative to get around the above issue is to quantize the signal in phase domain directly. A phase ADC converts the phase information into digital codes regardless of the input amplitude that obtains an inherent immunity to the magnitude variation, therefore significantly relaxed the requirement of AGC. Another benefit is that the additional digital overhead for demodulation can be avoided as the quantization is based on the signal's phase, eventually saving the area and power consumption.

With the standard modulation index h $=$ 0.5 of BLE, the phase of symbol "1" is 90°, and the phase of symbol "0" is $-90°$ [5]. Considered the conventional BLE symbol rate of 1 MHz with the baseband frequency of 250 kHz, a 2-bit phase ADC with phase LSB $=$ 90° (250 k/1 M $\times$ 360°) is sufficient to detect the symbol. In practice, the signals at the transmitter and the receiver side have a frequency deviation of $\pm$150 kHz, resulting in a frequency variation from 100 to 400 kHz in the receiver [4]. Meanwhile, the phase difference of each symbol in the system varies from 36° to 144°. Therefore, to tolerate this frequency variation, a 4-bit phase domain ADC with a quantization step of 22.5° operating at 1 MS/s is required.

To achieve the above specifications, several phase ADC architectures were investigated in the literature. In [4] and [9], two full-flash architectures are reported, where they both detect zero-crossings in the rotated versions of the initial phase to determine the input phase condition. However, such architectures demand linear resistive/current combiners that consume static current to generate phase shifted sinusoids for zero-crossing detections, thus consuming a large power dissipation [4], [9]. Another phase ADC explores a binary-search IQ-assisted algorithm [11], [12] that omits the linear combiner and reduces the number of comparisons from 2^{N-1} in Flash to N $+$ 1 for an N-bit phase ADC [11]. Nevertheless, both

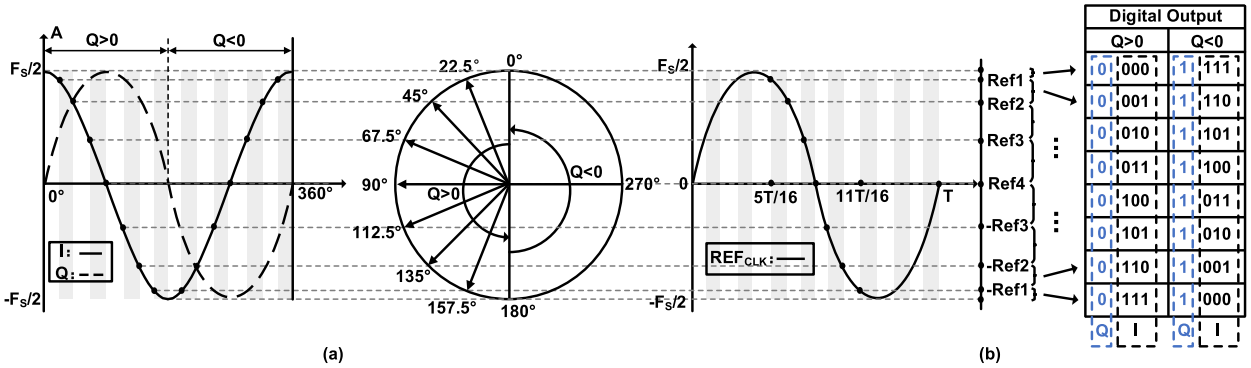

Fig. 1. (a) Phase intervals definition, (b) time to voltage definition and the corresponding digital outputs.

voltages of the I and the Q signals are necessarily tracked and then held by an active track-and-hold (T&H) circuit as well as a charge-redistribution DAC [12]. Since the I and the Q signals may behave as reference voltages of the DAC during the conversion [12], a power-hungry T&H circuit [11], [12] is essential in order to achieve a sufficient conversion accuracy.

In this paper, a phase ADC based on the time domain operation is presented. Unlike previous works, its references are realized based on the time manner, thus avoiding the power-hungry linear combiners or active T&H circuits. Benefiting from the time domain operation, the ADC only consumes dynamic power; therefore, it obtains a better energy efficiency and becomes more scaling friendly. The prototype is fabricated in the 65-nm CMOS technology. It also achieves an Effective Number of Bits (ENOB) of 3.42 bits at near Nyquist input and consumes 7 μW power from a 1 V supply when running at 1 MS/s, resulting in an FoM of 1.36 pJ/conversion-step.

The rest of the paper is organized as follows. In Section II, the proposed principles, the ADC architecture and the envelope variations are described, followed by a detailed description of the circuits in Section III. Measurement results are presented in Section IV. Finally, Section V gives the conclusion.

II. ADC Architecture and Envelope Variation

A. ADC Architecture and Operation

In Phase-Shift-Keying (PSK) and FSK, the phase information φ is represented by two quadrature signals I and Q, which equal to cosφ and sinφ, respectively [4]. To convert the phase information of this pair of quadrature signals into digital with a 4-bit phase quantizer, the full-scale phase (0°-360°) is equally divided into 16 intervals, as illustrated in Fig. 1(a) where $Q>0/Q<0$ corresponds to the signal range of $0° < \varphi <180°/180° < \varphi <360°$. The I signal is splitted into 8 voltage regions. If the values of I and Q of an unknown phase φ are given, by mapping the value of I to those 8 regions and identifying the polarity of Q, φ can be easily resolved.

Conventionally, to obtain the voltage references for such 8 regions, a combiner which is similar to the current steering is required, thus leading to an inevitable quiescent current. Instead, we proposed a time-domain reference generation technique that consumes only dynamic power. In the receiver end, a reference clock signal (REF_{CLK}) is necessary to identify

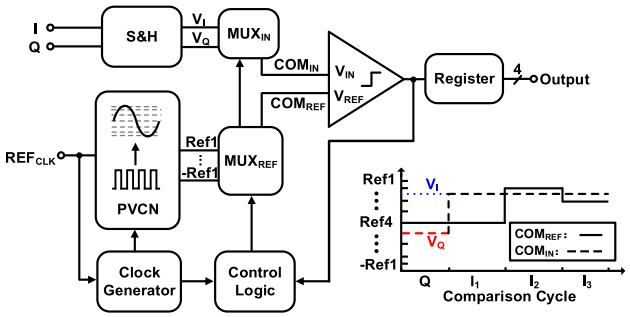

Fig. 2. ADC architecture and conversion diagram.

the baseband signals. With a period T and a normalized amplitude with I and Q signals, REF_{CLK} is divided into 16 identical time intervals (T/16). The corresponding 7 references (with 8 regions) can be obtained at the crossing points between the 16 interval instants and the REF_{CLK} (Fig. 1(b)), where Ref1, Ref2, …, −Ref1 are corresponding to 5T/16, 6T/16, …, 11T/16 time interval crossing points, respectively. Such 7 references can be easily sampled and stored in a capacitive network (Fig. 2), consuming a very low dynamic power. With these 7 intervals and a Phase-to-Voltage Capacitive Network (PVCN), the complex and power hungry resistive/current combiners [4], [9] or monotonic nonlinear unary DAC [12] in prior phase ADC designs can be avoided.

Fig. 2 shows the proposed ADC architecture. It consists of a passive S&H circuit for the input sampling, a PVCN for the reference generation, a comparator, a clock generator, a control logic, a register and two MUXes (MUX_{IN} and MUX_{REF}). The PVCN, which is designed according to the time domain concept introduced in the previous section, generates all the 7 references by co-working with the clock generator. The MUX_{IN} selects I or Q signal sampled by the S&H circuit for comparison while MUX_{REF} selects one of the reference levels to compare. The operation is similar to a Successive-Approximation Register (SAR) ADC that provides a binary-searched feedback according to the decision of the comparator in the phase domain. REF_{CLK} is the sinusoid signal that is used to generate the 7 reference levels and simultaneously severs as the master clock for our ADC.

The I and Q signals are first sampled by the S&H circuit in the sampling phase that is followed by the reference generation

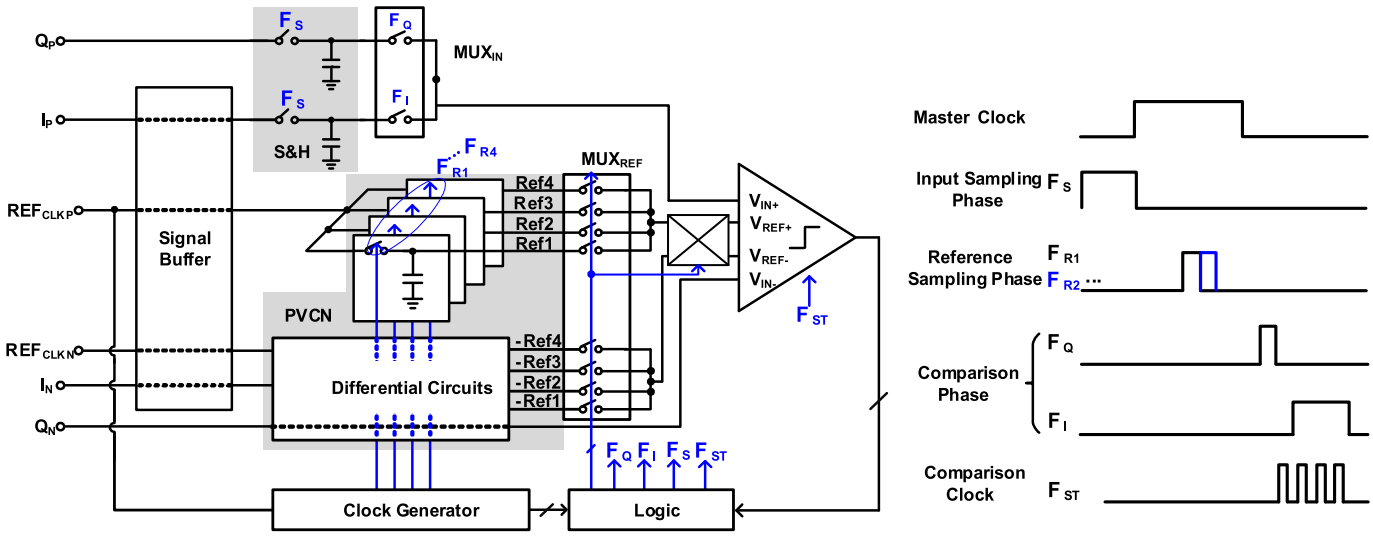

Fig. 3. ADC implementation and timing diagram.

phase. In the comparison phase, the MUX_{IN} selects the Q signal while MUX_{REF} selects Ref4 for the MSB determination that signs the polarity of Q. Afterwards, the V_I signal is selected and compared with $\pm$Ref1-3 in the successive approximation manner. As the example shown in Fig. 2, the comparison starts from Ref4, and the decision of the comparator controls MUX_{REF} to choose the next reference level (Ref2 in this case) for MSB/2. The procedure repeats 3 times to quantize a 4-bit phase resolution.

B. ADC Implementation

The specific implementation of the phase ADC is depicted in Fig. 3. For simplicity, only the positive side of the circuit is shown, as the negative counterpart is identical. A signal buffer circuit is added to serves as a voltage buffer for both I and REF_{CLK} signals. However, if voltage buffers are inherently available, such signal buffer can be omitted.

To generate the reference levels, the PVCN, which consists of a simple switch-capacitor network controlled by $F_{R1\sim4}$ (in Fig. 4), samples 4 times of the REF_{CLK} in 4 equivalent time intervals. $F_{R1\sim4}$ are four non-overlapped clocks having a fixed delay of 1/4T, 5/16T, 3/8T and 7/16T with the master clock respectively and pulse widths of T/16. When the reference generation phase ends, the voltage references are stored in the PVCN. Once the input and references are ready, the quantization is triggered by F_{ST} (the clock of the dynamic comparator).

In the last two comparison cycles of V_I, where V_I needs to compare with negative references ($-$Ref1 to $-$Ref3), the positive references and the negative references are swapped from the comparator's V_{REF+} to V_{REF-} side. For example, if the decision of the first comparison of I which is comparing with Ref4 is "0", implying that it is smaller than Ref_4, V_I will compare to $-Ref_2$ in the next comparison cycle. As shown in Fig. 3, sampled reference -Ref2 is at V_{REF-} side, but $-$Ref2 is required to connect to V_{REF+} to make the comparison. Therefore, $-$Ref2 is swapped from

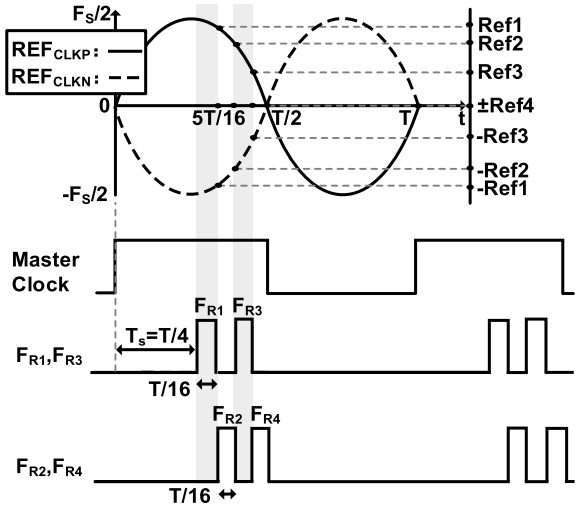

Fig. 4. Reference sampling timing diagram.

V_{REF-} to V_{REF+}, and meanwhile Ref2 is swapped from V_{REF+} to V_{REF-}. The cases of $-$Ref1 and $-$Ref3 are similar.

C. Envelope Variation

As described in the introduction section, the phase ADC has a certain ability to reject the magnitude variation of the input signals. To show the influence of the magnitude variations on our phase ADC, a simulation in which the envelope of the signals (I, Q and REF_{CLK}) are varying with time in a sinusoid fashion (Fig. 5) is conducted. The varying period of the envelope is T_E, and the period of the input signals (I and Q) is T_{IN}. A_C is the constant envelope amplitude, and A_V is the largest variation of the envelope from the constant amount. To further quantify the variation, a variation factor F_V which equals to the value of A_V/A_C is defined. Fig. 6 shows the ENOB variation versus the F_V variation under different values of T_{IN}/T_E.

In receiver systems, AGCs are always required since the envelope variations can be significant. The ADC used in

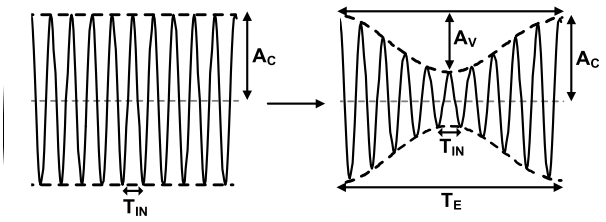

Fig. 5. Example of envelope variation diagram.

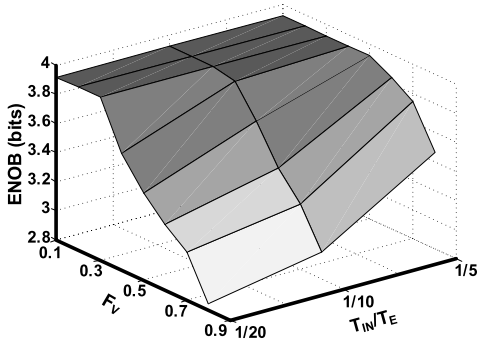

Fig. 6. ENOB versus F_V and T_{IN}/T_E.

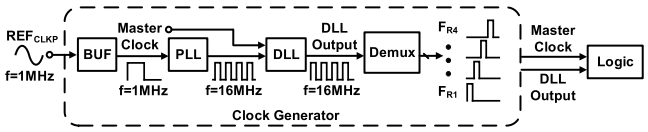

Fig. 7. Overall clock generator block diagram.

receiver systems for variable gain control should provide amplitude information of the received signals; thus, an amplitude ADC is necessary to detect the envelope information. In other words, an amplitude ADC and a phase ADC are both required . However, the resolution of the amplitude ADC and the performance of the gain control can be much more relaxed because of the robustness of phase ADC to the envelope variation. As an example, the PGA in [4] only implements a coarse gain step of 6 dB because of the large tolerance of envelope variation of the phase ADC.

III. Circuit Implementation

A. Clock Generator

The clock generator illustrated in Fig. 7 consists of a buffer, a Phase-Locked Loop (PLL) block, a Delay-Lock Loop (DLL) block and a De-multiplexer (Demux). The REF_{CLKP} first passes through the buffer to generate the master 1 MHz clock. Feeding the master clock to the PLL, a 16 MHz clock is obtained, and the 16 MHz clock passes through the DLL block to align with the master clock. The Demux separates the 16 MHz DLL output to four 1 MHz reference sampling clocks as $F_{R1\text{-}4}$. The master clock and the DLL output are also fed to the logic circuit for further control signals generation.

1) PLL: The PLL block is a feedback system that includes a voltage-controlled oscillator (VCO), a frequency divider, a phase detector and a low pass filter within its loop. Its purpose is to ensure that the VCO generates a 16 MHz output under a 1 MHz input reference clock. Fig. 8 shows the PLL block diagram. The output of the VCO is fed to the phase detector after the buffer and the frequency divider. The frequency divider divides the frequency of VCO by 16, and the phase detector detects the frequency difference between the master clock and the output signal of the frequency divider, where their frequency difference is translated into the pulse width of V_E. V_E is then transformed to V_C by the low pass filter (LPF) to generate the control voltage for adjusting the output frequency of the VCO.

When the feedback loop stabilizes, the PLL output frequency remains oscillating around 16 MHz due to the variation of V_C. This variation of the PLL output frequency potentially causes sampling mismatches of 7 reference levels, ultimately leading to conversion errors. Based on the simulation result, when the voltage variation of the reference voltages exceeds ± 37 mV (most critical case), the signal-to-noise-and-distortion ratio (SNDR) of the phase ADC drops 3 dB. As shown in Fig. 9, this voltage variation ΔV can be referred to the pulse width variation ΔT and further to the PLL's period variation T_F' which can be calculated as:

$$T_F^{'} = \frac{arcsin\left[sin\left(\frac{8\pi}{16}\right) - \Delta V\right] - \frac{8\pi}{16}}{2\pi} \times T + T_F, \qquad (1)$$

where T is the period of REF_{CLK}. Based on (1) with $T = 1\mu s$, $\Delta V = \pm 37$ mV and $T_F = 62.5$ ns, the T_F' is ± 6 ns, and the equivalent PLL frequency drift should be within 14.6 MHz $-$ 17.7 MHz in order to have less than 3 dB SNDR degradation. The frequency variation is further translated into the requirement of the K_{VCO} which defines the frequency variation when V_C varies by 1 V. In our design, even when sizing $M_{C1\text{-}3}$ to minimum width and length, a K_{VCO} of 0.5 MHz/V is achieved which can tolerate a 0.5 V variation of V_C in one cycle. The VCO is implemented by three (minimum number of inverters for VCOs to oscillate) inverter-based delay stages and all the transistors are in minimum sizes.

2) DLL: The DLL block is implemented to ensure that the 16 MHz reference sampling clock aligns with the master one so that accurate references can be obtained. The block diagram is illustrated in Fig. 10(a) together with a charge pump and a delay block circuit schematic. It contains a delay block, a frequency divider, a phase detector and a charge pump. After passing the delay blocks, the DLL output is divided by 16. Then its phase is compared with the master 1 MHz clock in the phase detector, where their phase difference is transferred to the pulse width of the output signals UP and DOWN. The charge pump generates V_{CP} and V_{CN} from UP and DOWN to control the delay of the delay cells. The phase of the DLL output can be adjusted to synchronize with the master clock.

The phase synchronization accuracy is determined by the delay time variation of the DLL circuit Δt as illustrated in Fig. 10(b). Based on the analysis in the previous PLL section, such delay time variation should be within ± 6 ns. To ensure this ± 6 ns variation requirement of Δt after the DLL stabilizes, the V_{CN} has to be designed with 150 mV variation to cover 0-62.5 ns delay variation while at the same time preventing M_9 and M_{10} from entering the

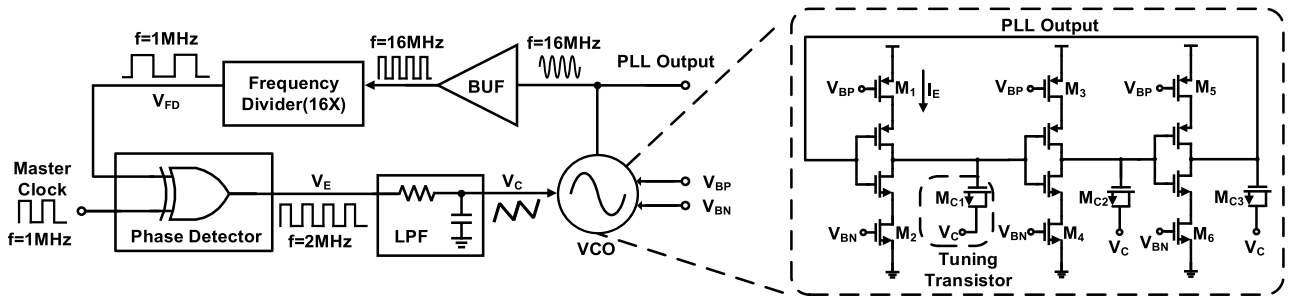

Fig. 8. PLL block diagram.

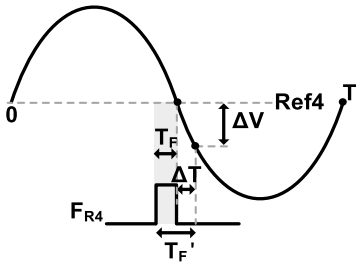

Fig. 9. Frequency variation diagram.

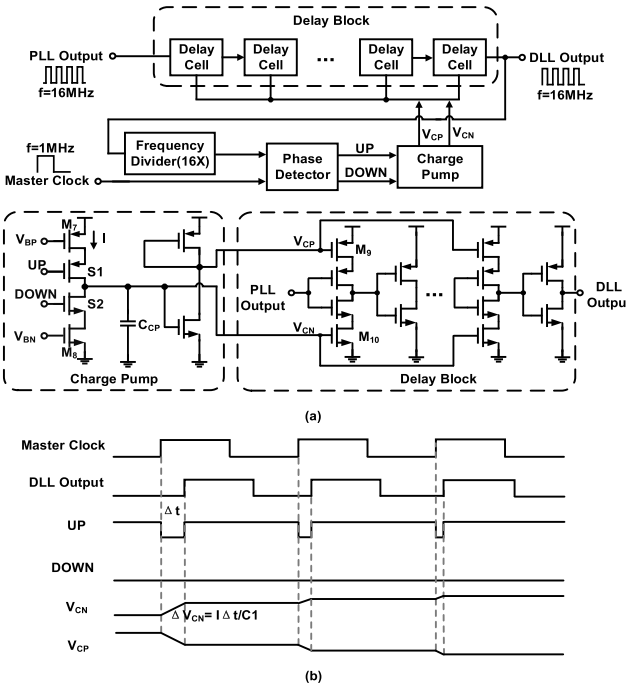

Fig. 10. DLL (a) block diagram and (b) timing diagram.

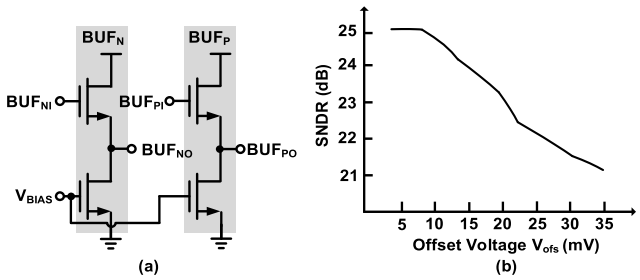

Fig. 11. (a) Buffer diagram and (b) relationship between offset voltage and SNDR.

sub-threshold region. Thus, the equivalent ΔV_{CN} for ± 6 ns variation of Δt should be within 28.8 mV as 150 mV/62.5 ns $= \Delta V_{CN}/12$ ns. Since $\Delta V_{CN} = I\Delta t/C_{CP}$, the value of I/C_{CP} should be smaller than 2.4×10^6. If a 30 fF value is chosen for C_{CP}, the current I requires a value smaller than 72 nA. By implementing M_7 and M_8 as hvt MOS transistors and the sizes to minimum can meet the requirement of the DLL.

B. Signal Buffer With Offset Cancellation

Before the sampling, the input I and the REF_{CLK} are passed through a signal buffer which indeed includes two buffers (BUF_P and BUF_N) and an offset cancellation circuit (four capacitors and some switches). The two identical buffers (shown in Fig. 11(a)) built with simple source-follower topology are implemented for buffering the signal (I) and the reference (REF_{CLK}), as well as avoiding the switches' kickbacks to the front analog circuit. BUF_{NI} and BUF_{PI} are the input terminals; BUF_{NO} and BUF_{PO} are the output terminals. V_{BIAS} is the biasing voltage for the buffers.

Due to the device mismatches, the output common mode voltages of BUF_P and BUF_N are different, which introduces references mismatches and eventually degrading the conversion accuracy. To demonstrate the design sensitivity to the offset, Fig. 11(b) plots the offset voltage V_{ofs} versus the SNDR. The buffers indicate one sigma offset mismatches of 40 mV from Monte Carlo simulations, which leads to more than 4 dB SNDR drop. Therefore, the offset cancellation technique is proposed to fix the offset mismatches from the input buffers.

Fig. 12 shows the detailed circuit implementation and its timing diagram. The offset cancellation is processed in three phases. Firstly, the offsets from the buffers are sampled and stored at the output loading capacitor (C_1 & C_2) by resetting the input to V_{CM} ($\Phi_{CM} = 1$). Then the input sampling phase starts ($\Phi_S = 1$), where the differential inputs I are double sampled onto C_3 and C_4, respectively. To cancel the offset in C_3 and C_4 ($\Phi_{SH} = 1$), they are connected in series with C_1 and C_2, respectively. The offset polarities of two series connected capacitors are opposite. Thus, they cancel out after sharing. Output voltages are V_{IP} and V_{IN}. The final signal amplitude remains the same as the input signal since the double sampling is used to amplify the signal by 2. $C_{1\text{-}4}$ have the same capacitance of 10 fF.

C. Comparator

The four-input comparator circuit schematic is depicted in Fig. 13. The comparator is StrongArm architecture with NMOS input pairs. Both the reference and the input pairs

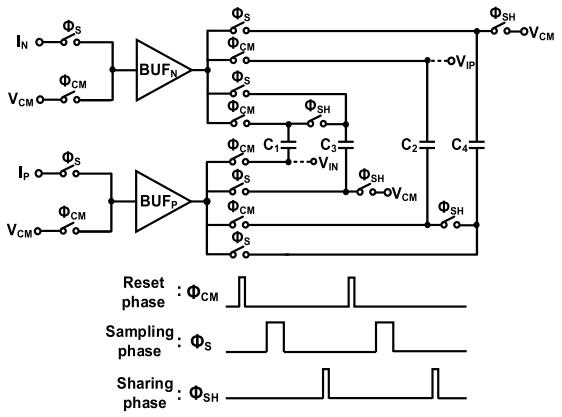

Fig. 12. Offset calibration circuit and timing diagram.

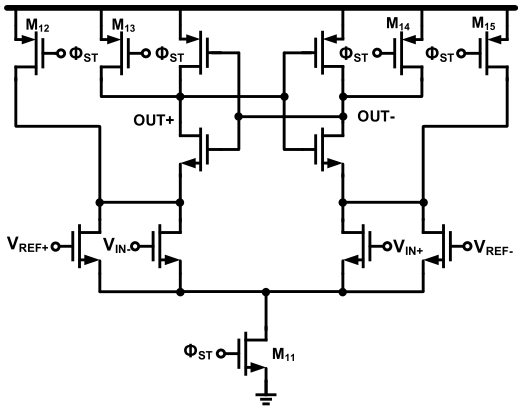

Fig. 13. Comparator circuit schematic.

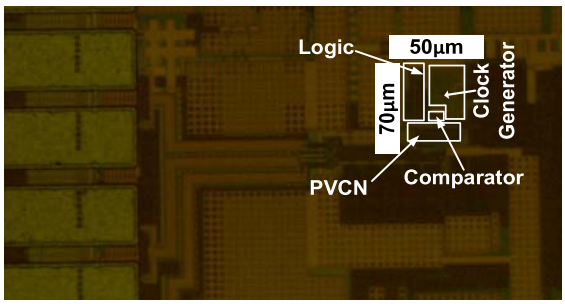

Fig. 14. Die micro photograph.

share the same branch and tail switches. When $\Phi_{ST} = 0$, transistors $M_{12\text{-}15}$ are on, and M_{11} is off to reset the outputs of the comparator (OUT+/−) to the supply voltage. When Φ_{ST} changes from the ground to the supply voltage, the tail transistor M_{11} is on, and $M_{12\text{-}15}$ are off, then a current path from the supply to the ground is conducted. The input and reference voltages are converted from the voltage to current domain through the input and reference pair transistors. Such current difference triggers the regeneration process of the back-to-back inverter and gives a decision at the output of the comparator. A latch circuit follows the comparator to ensure a fast and valid regeneration process within a given time.

TABLE I
PERFORMANCE COMPARISON

	[4]	[11]	This work
Technology(μm)	0.13	0.18	0.065
Architecture	Current Combiner	Charge - Redistribution	Time Domain Quantization
Power Supply(V)	1	1.2	1
Resolution(bits)	4	5	4
Sampling Rate(MS/s)	1	1	1
Power Consumption(μW)	25	12.9	7**
ENOB@ Nyq(bits)	3.61*	3.36	3.42
Chip Area(mm^2)	0.015	0.059	0.0035
FoM(pJ/c-s)	16.6*	2.5	1.36

*:Input frequency at 123.1kHz. ENOB at Nyquist rate is not provided.
**: Including signal buffer power.

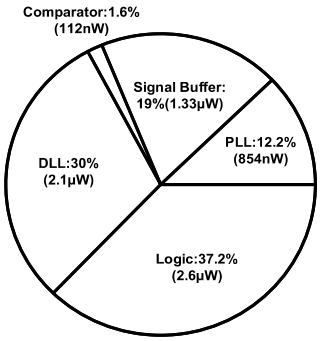

Fig. 15. Power breakdown of the phase ADC.

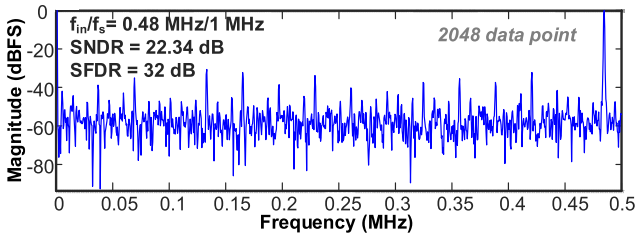

Fig. 16. Measured spectrum (2048-point FFT) at near Nyquist input.

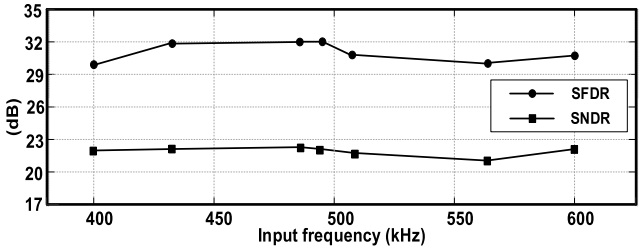

Fig. 17. SNDR and SFDR variation with input frequency.

IV. MEASUREMENT RESULTS

This 4-bit 1 MS/s phase ADC was fabricated in the 65-nm CMOS technology. The occupied active core area is 70 μm × 50μm as shown in the microphotograph in Fig. 14.

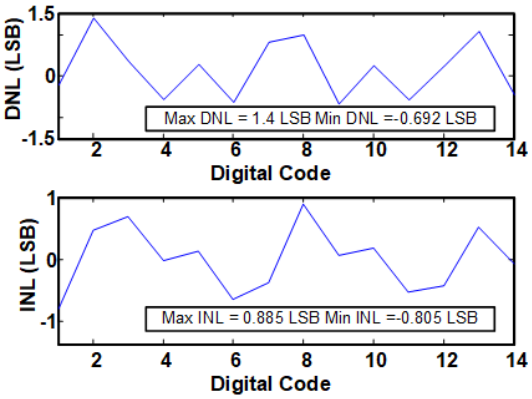

Fig. 18. Measured DNL and INL.

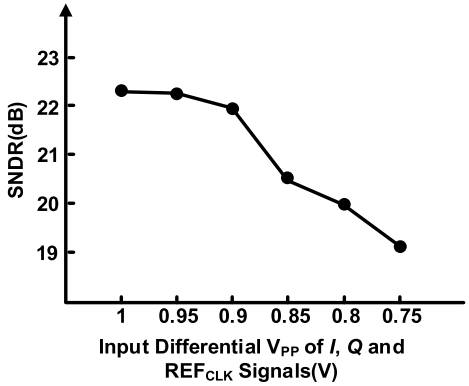

Fig. 19. Measured SNDR as a function of the differential V_{PP} voltages of the I, Q and REF_{CLK} signals.

The phase ADC works under a 1 V power supply and consumes only 7 μW power at 1 MS/s thanks to the proposed fully dynamic reference generation scheme. Fig. 15 shows the power breakdown diagram. The power consumption of the comparator, the signal buffer, the PLL circuit, the DLL circuit and the logic circuits are 112 nW, 1.33 μW, 854 nW, 2.1 μW and 2.6 μW, respectively. Different from voltage domain ADCs, the phase is considered as the variable of the ADC input for the dynamic measurement of phase ADCs. Therefore, the Q input signal is set to $A\sin[\pi \sin(2\pi ft)]$, where A stands for the amplitude of Q, f stands for the frequency and t stands for time. Likewise, the I input signal is set to $I = A\cos[\pi \sin(2\pi ft)]$ to match the Q counterpart. Fig. 16 shows the ADC output spectrum with input phase frequency of 0.48 MHz. The measured phase SNDR is 22.35 dB, resulting in a 3.42 bits ENOB at this near Nyquist input. The measured SNDR and the spurious-free dynamic range (SFDR) with input frequency sweeping are plotted in Fig. 17. It can be observed that SNDR and SFDR basically remained unchanged even the phase input rises to high frequency (above Nyquist). It is worth noting that, due to input transformer limitation, a low-frequency phase input cannot be provided. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) values are shown in Fig. 18. Fig. 19 depicts the measured SNDR as a function of the differential peak-to-peak voltages (V_{PP}) of the I, Q and REF_{CLK} signals. When the V_{PP} voltage decreases to 0.75 V, the SNDR of the phase ADC drops about 3 dB. The FoM used in table I is defined by:

$$FoM = \frac{P}{2^{ENOB} \times f_{in}}, \tag{2}$$

where P is the power consumption of the ADC, ENOB is the effective number of bits when the input is at Nyquist frequency, and f_{in} is the Nyquist input frequency. Table I shows the comparison of the proposed ADC with other state-of-the-art works. The proposed ADC demonstrates the best power efficiency with a small area.

V. Conclusion

In this paper, a low power phase ADC with time-domain reference generation concept is proposed. Benefitted from the fully dynamic power dissipation, the ADC achieves an outstanding FoM and attains a compact area. With only 7 μW power consumption at 1 MS/s, the ADC obtains an FoM at Nyquist input of 1.36 pJ/conversion-step, which is a suitable design for low power communication system based on the phase modulation scheme.

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