A 0.46-mm^2 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS

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***Abstract*—A unified receiver front-end (RFE) for mobile TV covering the VHF-III, UHF and L bands is described. Performance, power and area efficiencies are advanced in threefold: 1) a *gain-boosting current-balancing balun-LNA* exhibits high linearity, wideband output balancing and adequate S_{11} against gain control; 2) a *current-reuse mixer-low-pass-filter* merges quadrature-/harmonic-rejection mixing and third-order current-mode post-filtering in one block, enhancing linearity and noise just where both are demanding, while saving power and area for its simplicity; 3) a *direct injection-locked 4-/8-phase LO generator* relaxes the master LO frequency by avoiding frequency division. Fabricated in 65-nm CMOS the RFE measures 4-dB noise figure, 17-to-35-dB gain range, and $+32/-3.4$-dBm IIP2/IIP3 with no tuning. The power consumption ranges from 43 (170 MHz) to 55 mW (1.7 GHz) at 1.2-/2.5-V supplies. The die size is 0.46 mm^2.**

***Index Terms*—Balun, CMOS, local oscillator, low-noise amplifier, low-pass filter, mixer, mobile TV, multi-phase, radio frequency front-end, receiver.**

I. Introduction

With improved device parasitics in nm-length CMOS processes, wideband RF circuits offer the desired compactness and power efficiency in realizing multi-band multi-standard radios. This paper describes a receiver front-end (RFE) targeting the mobile-TV applications. It covers the VHF-III (174 to 248 MHz), UHF (470 to 862 MHz) and L (1.4 to 1.7 GHz) bands, where standards like T-DMB, ISDB-T, DVB-H and DMB-T are resided. In order to meet the noise and linearity specifications [1], while avoiding external baluns or repeated RFEs that were still common in existing solutions [1], [2], a number of circuit techniques are proposed to enhance the performance, power and area efficiencies [3]. Together they lead to state-of-the-art performance, while saving 58% area compared to the 1.1 mm^2 reported in [2]. The key design considerations are outlined as follows.

A wideband balun low-noise amplifier (LNA) can nullify the cost and insertion loss of an external balun, but might suffer from low IIP2 and weak output balancing compared to its fully-differential counterpart. The output balancing of a balun-LNA significantly affects the IIP2 of the mixers following it. The common-gate (CG) common-source (CS) balun-LNA [4] serves as an example. Although noise cancellation and admittance scaling techniques can lower the noise figure (NF) to <3 dB, the imbalance load and bias current between the CG and CS branches weakens the IIP2 and output balancing. Output buffers were employed to alleviate those issues at the expense of extra power. Alternatively, in [5], IM2 cancellation feedback was introduced to enhance IIP2. This technique, however, penalizes the output bandwidth (BW) and noise figure (NF), while the problem of weak output balancing remains unsolved. In this work, a *gain-boosting current-balancing* balun-LNA is proposed. It not only addresses the aforementioned issues, but also offers adequate input matching over variable gain control (VGC).

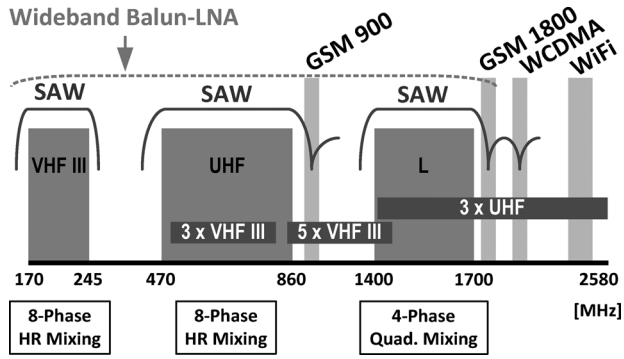

Fig. 1. Overview of SAW filtering, balun-LNA's bandwidth and mixing strategies.

Harmonic mixing and intermodulation distortion are critical concerns of wideband RFEs. The former is due to the hard switching nature of MOS mixers, i.e., blockers located at the harmonics of the LO become co-channel interferers after down-conversion. The latter is due to the potential co-existence of large amount of blockers throughout the passband. Regarding this, especially for *interoperable* terminals, external SAW filtering is still the most reliable solution [7]. As shown in Fig. 1, the SAW filters (e.g., [6]) can specifically notch to the very nearby cellular bands.

With adequate pre-filtering the linearity of the RFE will be mainly limited by the out-of-channel IIP2 and IIP3 [7]. In this paper, the mixer is merged with a current-mode third-order low-pass filter (LPF) for improving the out-of-channel linearity, while saving power and area for its simplicity. A third-order stopband rejection profile suffices for shifting most baseband (BB) functions to the digital domain via low-power analog-to-digital converters [2], [7].

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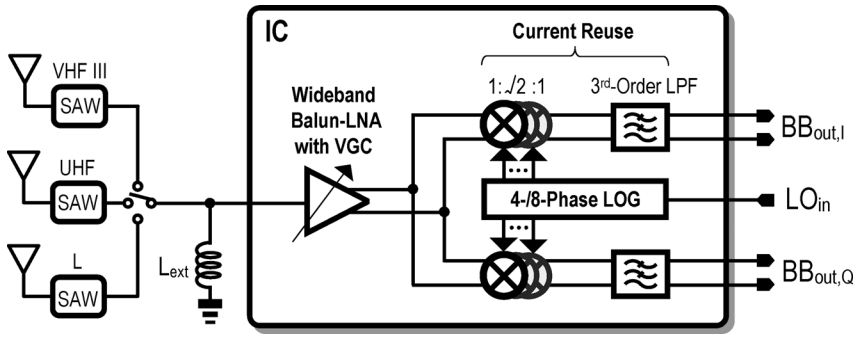

Fig. 2. Proposed full-band mobile-TV RFE.

When receiving the VHF-III and UHF bands, harmonic-rejection (HR) mixers[8] can relax the rejection profile of the external SAW filters, and minimize noise and distortion folding (i.e., the third and fifth harmonic bands are partially within the BW of the balun-LNA as marked in Fig. 1). The entailed 8-phase LO, if generated via frequency dividers, will necessitate a high master LO frequency ($f_{\rm LO}$). In fact, the frequency range ($\leq$0.9 GHz) of the RFE in [9] is limited by the required high $f_{\rm LO}$ (7.2 GHz) for generating the 8-phase LO, which significantly increases the power and complicates the design of the phase locked-loop (PLL) and voltage-controlled oscillator (VCO). In this work, a direct injection-locking 4-/8-phase LO generator (LOG) lowers the master $f_{\rm LO}$. This dividerless solution particularly suits this receiver-only application, as the problem of "VCO pulling" is irrelevant here in the absence of power amplifier.

The paper is organized as follows. Section II introduces the proposed RFE architecture, and discusses the technology features which play a key role in device sizing and topology selection. The conventional and proposed balun-LNAs are described in Section III. Section IV and Section V present the proposed current-reuse mixer-LPF and the direct injection-locked 4-/8-phase LOG, respectively. In Section VI, experimental results will be shown and the paper ends with conclusions.

II. RFE Architecture and Technology Features

Fig. 2 depicts the proposed RFE architecture headed by three external SAW filters. It integrates a wideband balun-LNA with VGC, dual I/Q mixers, a 4-/8-phase LOG and dual third-order BB LPFs merged with the mixers for current-reuse and current-mode filtering. One external inductor is entailed at the RF input. The differential signals from the balun-LNA are ac-coupled to the mixers to prevent the balun-LNA's even-order distortion products (i.e., the concern of narrowband IIP2 [10, p. 1545]) and $1/f$ noise from leaking to the BB. The mixer has two operating modes: 1) *HR mode* supports the VHF III and UHF bands, using a gain ratio of $1:\sqrt{2}:1$ among the three mixer cells and an 8-phase LO [8]; 2) *quadrature mode* supports the L band where HR is surplus as the harmonic bands are far out from the band of interest. In this case, the three mixer cells are parallelized and the LO is switched to 4 phases. A direct injection-locking LOG synthesizes the desired 4-phase and 8-phase LOs.

In nm-length CMOS processes the back-end features and options are highly related to the performances because of the parasitic effects. Here, the available dual supplies (1.2 and 2.5 V) and dual-oxide transistors (thin and thick) are employed to optimize the performances of the RFE. Dual-supplies free more design headroom in 65-nm CMOS SoC [1] and beyond [11].

The employed I/O pads are offered by the foundry. They have passed the 2-kV human-body mode (HBM) ESD tests, but add roughly 1-pF input capacitance that has to be taken into account in the design phase.

III. Wideband Balun-LNA

A. CG-CS Noise-Canceling Balun-LNA

Fig. 3 depicts its schematic. The single-to-differential stage (S2D) utilizes a CG amplifier (M_1) to generate the in-phase output. The source of M_1 is dc-grounded via an external big inductor $L_{\rm ext}$ to attain a wideband impedance match. The corresponding transconductance of M_1 ($g_{\rm m1}$) is 20 mS, given that $R_{\rm in} \approx 1/g_{\rm m1} = 50\ \Omega$. A CS amplifier ($M_2$) generates the anti-phase output, and assists noise canceling of M_1. The noise contribution of M_2 can be reduced by admittance scaling, e.g., $g_{\rm m2} = 4g_{\rm m1} = 80$ mS. To keep a balanced output in [4] a counterbalance load was used ($R_{\rm CS} = R_{\rm CG}/4$). This technique regrettably cannot ensure a *wideband* balanced output when driving the mixers (with the input impedance modeled as C_L). This fact, in addition to the bias current mismatch between the CG and CS branches, leads to low IIP2, weak output balancing and limited power supply rejection ratio (PSRR). Extra output buffers only can reduce the output imbalance at the expense of power, but the problem of low IIP2 remains unsolved.

B. Proposed Gain-Boosting Current-Balancing Balun-LNA With VGC

The S2D: The proposed balun-LNA [Fig. 4(a)] uses a new S2D. The first idea is to use an ac-coupled gain stage ($g_{\rm mx}$) to enhance the gain of the CS branch [Fig. 4(b)], avoiding scaling-up of $g_{\rm m2}$ with respect to $g_{\rm m1}$ (i.e., M_1 and M_2 are of equal size and bias current). The second idea is to reuse the gain generated by M_2 to enhance the gain of the CG amplifier by creating a loop gain $(1 + A)$ around M_1, where A is given by $|v_{\rm o1}{}_n/v_{\rm in}|$ [Fig. 4(c)]. Due to the single-stage structure of $g_{\rm mx} + g_{\rm m2}$, and the low impedance of $v_{\rm o1}{}_n$, A is ensured to be stable. This loop gain A not only boosts the effective gain of M_1 and lowers its noise contribution, but also reduces the minimum $I_{\rm DC}$ for M_1 to

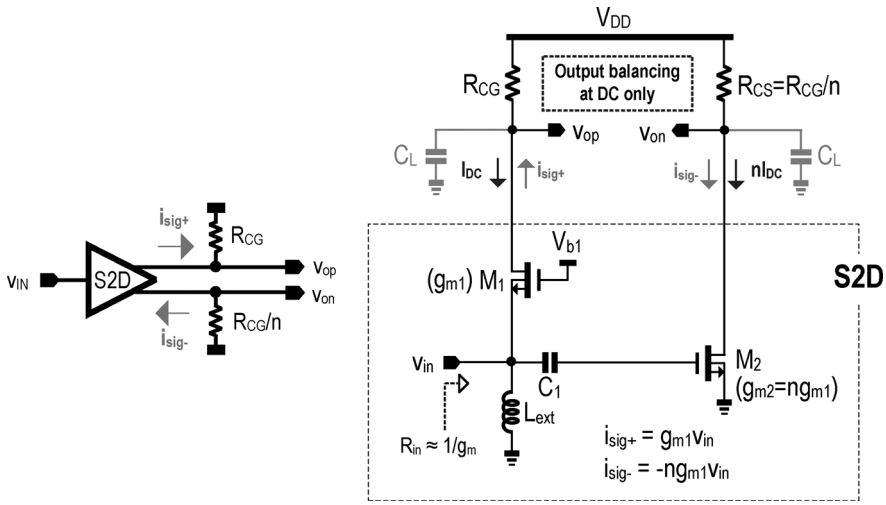

Fig. 3. CG-CS noise-canceling balun-LNA [4] (simplified bias).

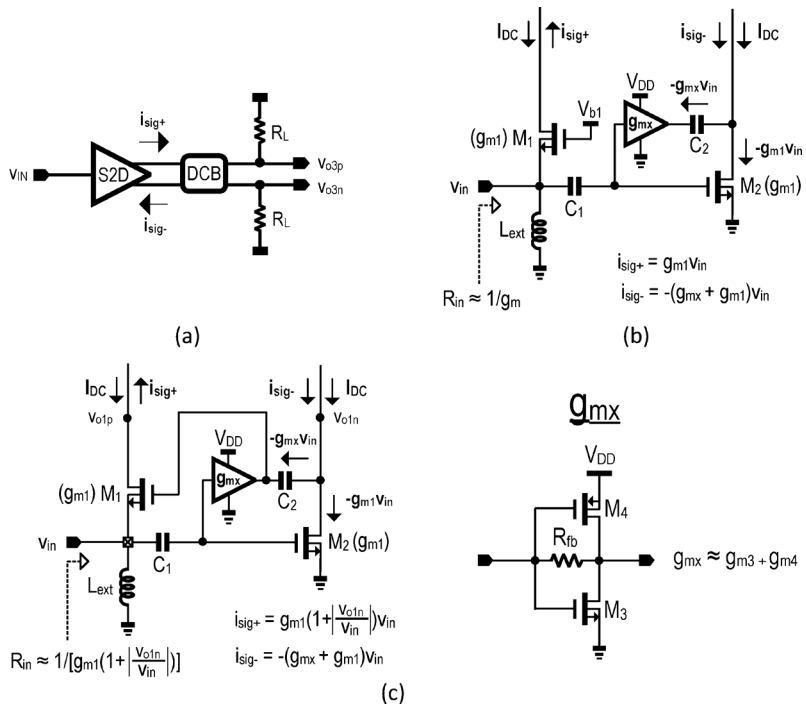

Fig. 4. Generation of the proposed S2D: (a) the overall balun-LNA structure. (b) Ac-coupled gain boosting avoids mismatch of $I_{\rm DC}$. M_1 and M_2 are of equal size and bias current. (c) The final topology: gain-boosting the CG via the CS, where the gain-boost stage ($g_{\rm mx}$) is a self-biased inverter amplifier (M_3 and M_4).

offer input impedance matching. An external big inductor $L_{\rm ext}$ simplifies the input impedance match and offers a DC-current path for the CG amplifier M_1.

In order to simplify the bias and save component count, $g_{\rm mx}$ is realized as an inverter amplifier (M_3 and M_4) with resistive feedback $R_{\rm fb}$ for self-biasing. This self-bias structure also handily biases M_1–M_2 as shown in Fig. 4(c). Comparing with the S2D topology in [4], just one capacitor C_2 and one resistor $R_{\rm fb}$ are added as M_3–M_4 can be counted as parts of M_2.

Differential Current Balancer (DCB): Balanced output impedance is critical to achieve wideband output balancing. Here, the differential balancing is realized in the current domain by inserting a DCB between the S2D and the load as shown in Fig. 5. The DCB serves as a differential current-control current source with unity gain, forcing $i_{\rm sig+} = -i_{\rm sig-} = i_{\rm sig}$. In principle, a cascode amplifier (M_5–M_6) with cross-coupled capacitors (C_3–C_4) might realize the DCB [12], as what it amplifies is the *difference* of the input. However, accounting for the finite output resistance of M_5–M_6, a double-cascode amplifier (M_5–M_8, C_3–C_6) is adopted to achieve wideband output balancing.

The DCB also benefits the S2D in two ways: 1) the condition $i_{\rm sig+} = -i_{\rm sig-} = i_{\rm sig}$ helps mapping the loop gain of the CG branch to the gain given by the CS branch, yielding $A = g_{\rm mx}/g_{\rm m1}$, which is a definable ratio insensitive to process if the channel-length modulation of M_1-M_4 is neglectable. 2) The DCB improves the balun-LNA's reverse isolation and linearity by lowering the swing at $v_{\rm o1p}$ and $v_{\rm o1n}$, where distortion arising from the nonlinear output resistance of M_1–M_4 can be minimized.

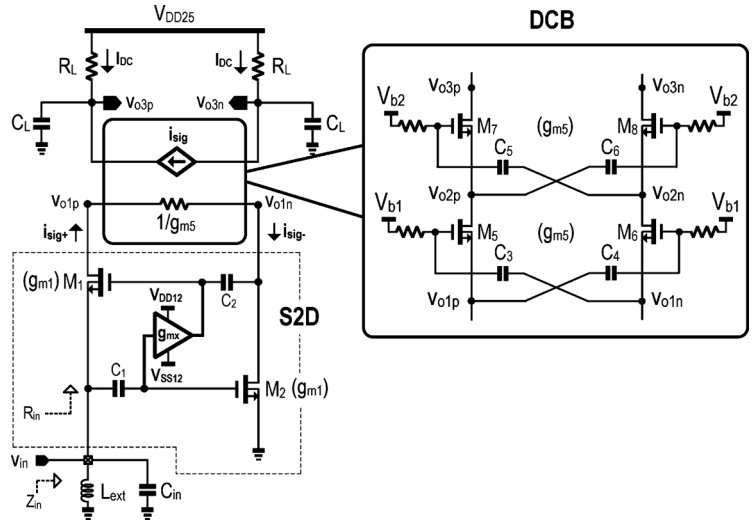

Fig. 5. The S2D combined with the DCB. M_1 and M_2 are of equal size and bias current generating the same g_{m1}.

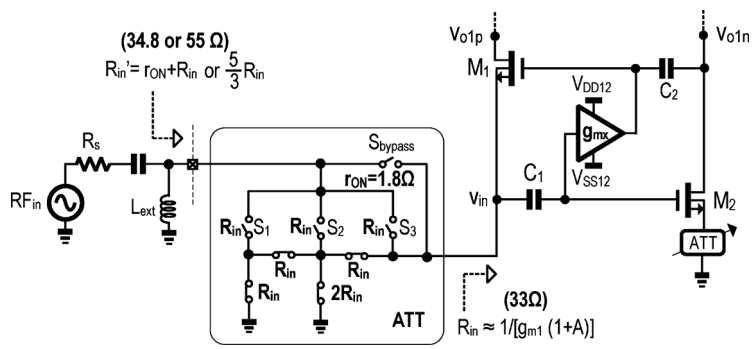

Fig. 6. The balun-LNA is preceded a passive ATT for coarse gain control.

The overhead of the DCB is the extra voltage headroom when compared with a typical cascode stage. The use of dual supplies (1.2 and 2.5 V) overcomes this limitation and allows more voltage gain without compromising the dynamic range (DR). A high-voltage design also offers opportunities to realize more functions in the current domain by cascoding them under one supply rail, potentially leading to a wider RF BW (i.e., less high impedance nodes), better linearity (i.e., small internal signal swing) and area savings (i.e., less ac-coupling capacitor between blocks).

Nevertheless, a high-voltage design with thin-oxide MOS requires node-voltage trajectory checks, to ensure no gate oxide and p-n junction are overstressed at transient and steady states. The bias scheme of the balun-LNA is designed as a single-ended replica of it, generating the bias voltages V_{b1} and V_{b2} for M_5–M_8. Such a scheme can detect the presence of V_{DD25} and V_{DD12}, ensuring no device is overstressed in power-up/down conditions. The reliability levels are guided by the foundry design rule manual.

Combining the S2D and DCB, the single-to-differential voltage gain $A_{\mathrm{v,diff}}$ and input impedance Z_{in} of the balun-LNA can be obtained

$$A_{v,\mathrm{diff}} = \frac{v_{\mathrm{o3p}} - v_{\mathrm{o3}n}}{v_{\mathrm{in}}} = 2g_{\mathrm{m_1}}(1+A)\left(R_L \parallel \frac{1}{sC_L}\right) \quad (1)$$

and

$$Z_{\mathrm{in}} = \frac{1}{g_{\mathrm{m1}}(1+A)} \parallel sL_{\mathrm{ext}} \parallel \frac{1}{sC_{\mathrm{in}}} \quad (2)$$

respectively. The demand of both high $A_{\mathrm{v,diff}}$ and low NF promotes setting a smaller Z_{in} via increasing g_{m1}, which is, however, constrained by the desire of input impedance matching. The minimum acceptable input reflection coefficient magnitude Γ_{in} can be determined as

$$|\Gamma_{\mathrm{in}}| = \left|\frac{Z_{\mathrm{in}} - R_S}{Z_{\mathrm{in}} + R_S}\right| \leq 0.32. \quad (3)$$

It corresponds to a S_{11} value of < -10 dB. Accordingly, the tolerable Z_{IN} for $R_S = 50\ \Omega$ ranges from 26 to 97 Ω. In this work, Z_{in} is set to 33 Ω ($g_{\mathrm{m1}} = 7.5$ mS and $\mathrm{g_{mx}} = 3\mathrm{g_{m1}}$) to enhance $A_{\mathrm{v,diff}}$ and lower NF, while yielding $S_{11} < -13$ dB (3 dB margin). Though acceptable here for the targeted frequency (0.17 to 1.7 GHz) in the employed 65-nm CMOS process, it should be noted that the impedance match BW is reduced when comparing it with a strict 50-Ω match.

The ATT: The balun-LNA is preceded by an nMOS-only R-2R network for coarse VGC as depicted in Fig. 6. It exploits the properties of partial signal reflection (i.e., Z_{in} deviates from R_S) and voltage division to realize the desired attenuation levels. The control range was set to 18 dB, which offers a reasonable tradeoff between IIP3 and NF at high input power

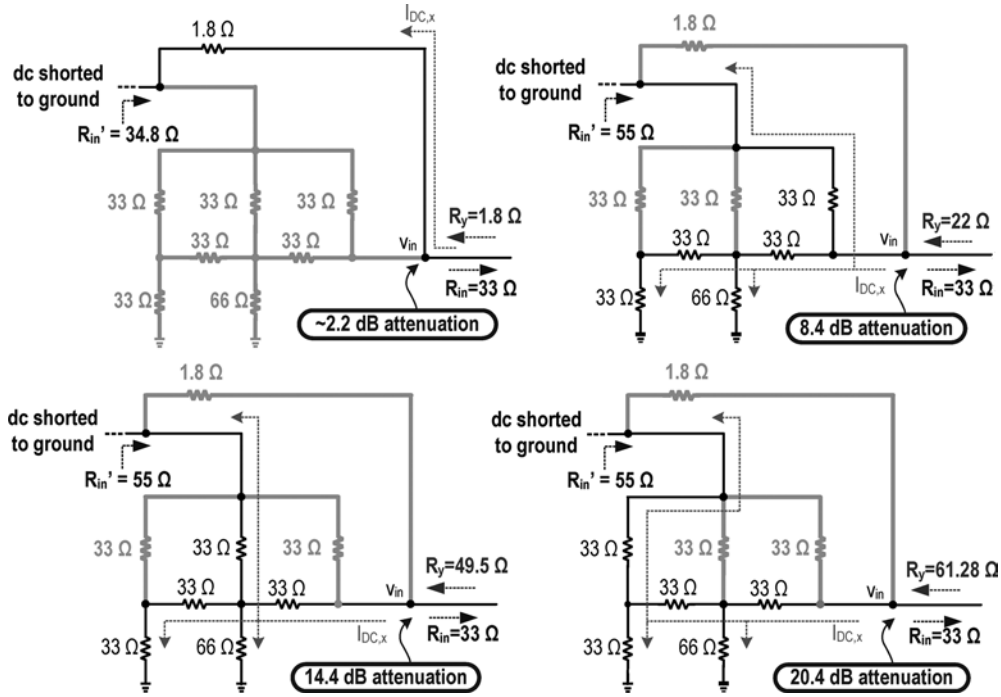

Fig. 7. Equivalent circuits of the nMOS-only ATT in each gain step.

levels. A 6-dB step size is related to the gain-tuning characteristic of an R-2R network when constant input impedance is sought. The gain switching is executed via $S_{\rm bypass}$, S_1, S_2, or S_3 as shown in Fig. 7. Operating at the low-impedance input node of the balun-LNA with $L_{\rm ext}$ provides the dc-ground, each nMOS enjoys a large V_{GS} of 1.2 V for high linearity, while offering VGC with a constant output BW. At the maximum gain, the ATT is bypassed with $S_{\rm bypass}$; it features a 1.8-Ω on-resistance ($r_{\rm ON}$) under a practical device size of 200/0.06. The combined $R'_{\rm in}$ varies between 34.8 Ω (ATT bypassed) and 55 Ω (with the ATT). Both values yield $\rm S_{11} < -13$ dB, giving room for process variation. The initial −2.2-dB attenuation at the highest gain is induced by the reflection and division between $r_{\rm on}$ and $R_{\rm in}$ (i.e.,

$$-2.2\ \text{dB} = 20\log\left\{\left[1-\frac{(R_S-R'_{\rm in})}{(R_{\rm s}+R'_{\rm in})}\right]\cdot\frac{R_{\rm in}}{(r_{\rm on}+R_{\rm in})}\right\}.$$

All MOS switches are operated in triode region with an ON-resistance value that is either $R_{\rm IN}$ or $2R_{\rm IN}$. The size of the former is obtained according to

$$\overbrace{\frac{1}{\mu C_{OX}\dfrac{W_{SW}}{L_{SW}}(V_{GS,SW}-V_{TH})}}^{\text{NMOS Switch}} = \underbrace{\frac{\overbrace{1}^{R_{\rm in}}}{\dfrac{1}{2}\mu C_{OX}\dfrac{W_{M_1}}{L_{M_1}}(V_{GS,SW}-V_{TH})(1+A)}}_{g_{\rm m1}}. \quad (4)$$

On the left of (4) $V_{GS,SW} \approx V_{\rm DD12}$, since all switched are switched [OFF, ON] by $[0, V_{\rm DD12}]$. On the right $V_{GS,SW} \approx V_{\rm DD12}/2$, which is set by the self-biased topology of $g_{\rm mx}$ [see Fig. 4(c)]. In the employed process, $V_{\rm DD12}$ is around 4x of the device's threshold voltage V_{TH}. Accordingly, an aspect ratio of $W_{\rm m1}/W_{SW} = 3/2$ can be obtained by assuming $\rm A = 3$ and $L_{SW} = L_{M1}$. A similar concept applies for the MOS switch with $2R_{\rm in}$ ON-resistance.

It is noteworthy that the bias current of M_1 has to be passed through the ATT. Considering the impedance back to the ATT (labeled as $R_{\rm y}$), the equivalent resistance at each attenuation step varies between 1.8 to 61.28 Ω. The source of M_2, thus, employs an ATT replica to track this variation (Fig. 6), matching the bias currents of the CG and CS branches against VGC.

Performance Optimization Via Using Dual $V_{\rm DD}$s: The NF of the balun-LNA is analyzed based on the simplified noise model shown in Fig. 8. For simplicity, channel-length modulation is neglected and $M_{\rm s}$ is used to represent the equivalent of M_2–M_4 in parallel. The transconductance $g_{\rm ms}$ of $M_{\rm s}$ correspondingly represents $g_{\rm m2}+g_{\rm m3}+g_{\rm m4}$. α and γ shown in Fig. 8 are the process- and bias-dependent parameters of the devices, respectively. The differential output noise voltages due to each source are obtained as

$$\upsilon^2_{n,R_S,\text{diffout}} = |V_{n,R_S,g_{\rm ms}}R_L|^2 \quad (5)$$

$$\upsilon^2_{n,M_1,\text{diffout}} = 0 \quad (6)$$

$$\upsilon^2_{n,M_S,\text{diffout}} = \left|I_{n,M_S}\frac{2R_L}{1+g_{\rm ms}R_S}\right|^2 \quad (7)$$

$$\upsilon^2_{n,M_5,\text{diffout}} = \left|I_{n,M_5}\left[\frac{g_{\rm m1}(1+A')}{g_{\rm m1}(1+A')+\frac{1}{R_S}}-\frac{1}{2}\right]R_L\right|^2 \quad (8)$$

$$\upsilon^2_{n,M_7,\text{diffout}} = 0 \quad (9)$$

$$\upsilon^2_{n,R_L,\text{diffout}} = |I_{n,R_L}R_L|^2 \quad (10)$$

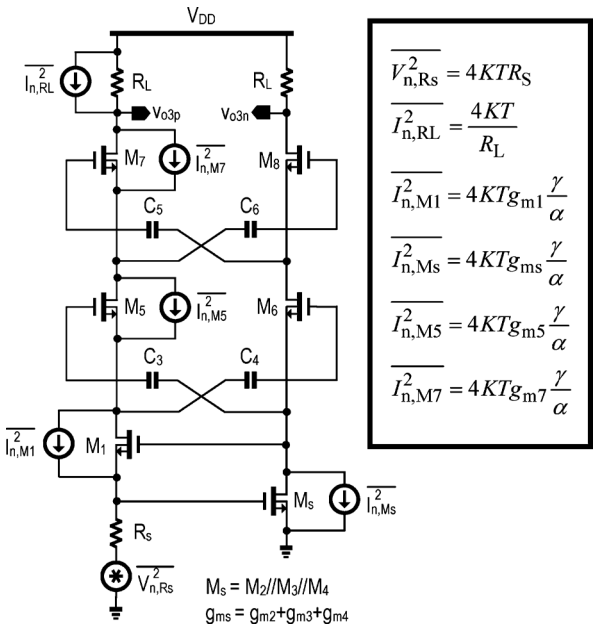

Fig. 8. Simplified noise model of the proposed balun-LNA. γ is the excess channel thermal noise coefficient. α is $g_{\rm m}/g_{\rm d0}$, with $g_{\rm m}$ the device transconductance and $g_{\rm d0}$ the zero-bias channel conductance.

where the loop gain around the CG branch is re-defined as $1+A'$ to match the set assumption in this section. With $g_{\rm m1} = g_{\rm m2}$, $1 + A'$ is related with a $g_{\rm m}$ ratio as given by

$$1 + A' = 1 + \frac{g_{\rm m3} + g_{\rm m4}}{g_{\rm m1}}. \tag{11}$$

The NF of the balun-LNA can be calculated by dividing the total output noise power due to all devices by the noise power of R_S. See equation (12) at the bottom of the page. If the input impedance match is exact ($R_{\rm in} = R_S$), we can set $g_{\rm m1}(1 + A') = g_{\rm ms} = 1/R_S$ to simplify (12) as

$$NF = 1 + \frac{\gamma}{\alpha} + \frac{2R_S}{R_L}. \tag{13}$$

Equation (13) is the same as that of CG-CS noise-canceling balun-LNA *without* admittance scaling: $g_{\rm mCG} = g_{\rm mCS} = 1/R_S$ [12]. The main difference here is the reduction of the minimum $I_{\rm dc}$ for 50-Ω matching by a factor of $1+A$. A smaller $I_{\rm dc}$ might compromise the linearity, but the presence of the DCB helps isolating the high-swing output node from the S2D, reducing the effect of S2D's nonlinear output resistance.

For a conservative value of $\gamma/\alpha = 4/3$, the NF is > 3 dB. For that reason, as mentioned before, the targeted $R_{\rm in}$ is 33 Ω to achieve better NF and gain. The factual value can be computed via (12) under $R_{\rm in} = 33\ \Omega$.

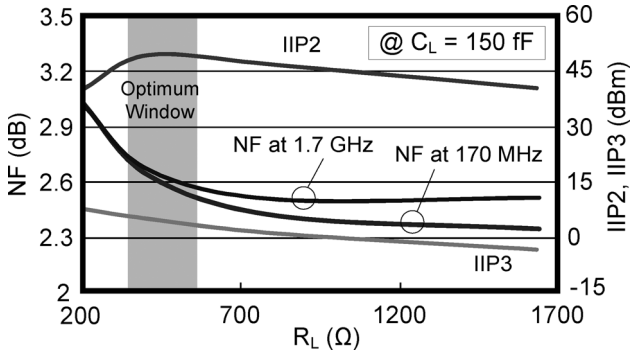

Fig. 9. Simulated IIP2, IIP3 and NF with respect to R_L. The optimum window of R_L is highlighted.

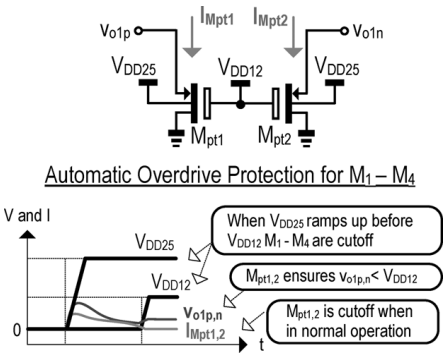

Fig. 10. A simple scheme for overdrive protection (the notations are referred to Fig. 5).

The 2.5-V supply allows a bigger R_L without degrading DR. In the size optimization the optimum range that can balance IIP2, IIP3 and NF was found to be within 340 to 570 Ω under a 150-fF load as shown in Fig. 9. In this region, the NF is < 2.8 dB and the IIP2/IIP3 is $> +45/+3$ dBm. R_L was chosen to be 410 Ω for a maximum IIP2. The in-band NF justified at boundaries of the desired BW (0.17 and 1.7 GHz) has a difference of < 0.1 dB. The corresponding mid-band gain is 25.6 dB and the output BW is around 2.6 GHz.

Startup Considerations: Mixed-voltage circuits require the concern of improper power-up/-down sequences. As depicted in Fig. 10, in case $V_{\rm DD,12}$ has a delay in start-up with respect to $V_{\rm DD25}$, M_1–M_4 are in the cutoff region overstressed by $V_{\rm DD25}$. The proposed solution is to add two small-size thick-oxide PMOS transistors $M_{\rm pt1}$ and $M_{\rm pt2}$ to $\rm v_{o1p}$ and $\rm v_{o1}$$_n$, respectively. With them, the dc voltages at $v_{\rm o1p}$ and v_{o1n} can be controlled to be within $V_{\rm DD12}$ when M_1–M_4 are still in cutoff region. Once $V_{\rm DD12}$ ramps successfully, $M_{\rm pt1}$ and $M_{\rm pt2}$ are automatically turned off. A similar operation holds in power-down condition when $V_{\rm DD12}$ is removed before $V_{\rm DD25}$.

$$NF = 1 + \frac{v_{n,M_1,\rm diffout}^2 + v_{n,M_S,\rm diffout}^2 + 2v_{n,M_5,\rm diffout}^2 + 2v_{n,M_7,\rm diffout}^2 + 2v_{n,R_L,\rm diffout}^2}{v_{n,R_S,\rm diffout}^2} \tag{12}$$

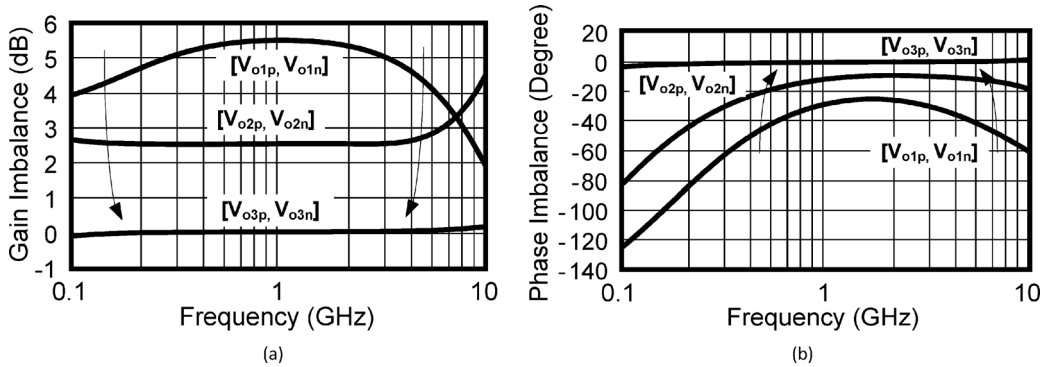

Fig. 11. Simulated gain (a) and phase (b) balancing progress inside the balun-LNA.

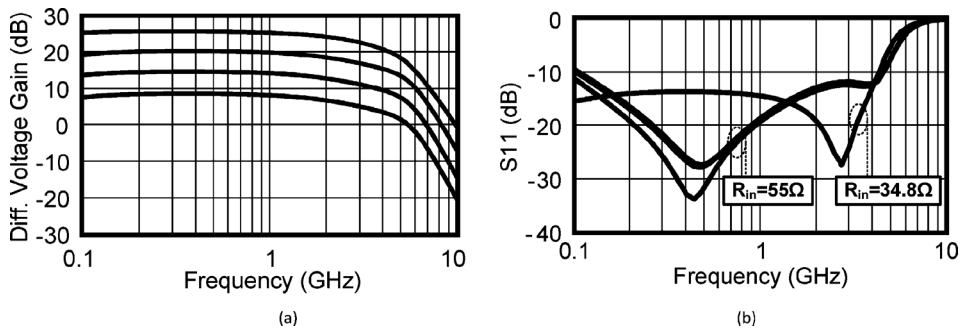

Fig. 12. Simulated balun-LNA's (a) AC responses and (b) S_{11} against gain control.

Differential Balancing: The progression of gain and phase balancing within the balun-LNA are assessed as shown in Fig. 11(a) and (b), respectively. The gain-phase imbalances are corrected progressively from $[v_{\rm o1p}, v_{\rm o1n}]$ to $[v_{\rm o2p}, v_{\rm o2n}]$ after the 1st balancing, and eventually to $[v_{\rm o3p}, v_{\rm o3n}]$ after the 2nd balancing. The in-band gain and phase mismatches are < 0.037 dB and $< 1.87°$, respectively. From 0.1 to 10 GHz, the former is still acceptably small (< 0.2 dB), whereas the latter is limited at the low frequency side ($< 3.5°$) due to the high-pass characteristic of C_3–C_6 (2-pF MiM capacitors) that were not oversized due to the add-on parasitics. The output balancing can be affected by device mismatches. A matching-conscious layout is entailed between M_1 and M_2, the differential R_L and DCB.

PSRR -The voltage gain from each supply and ground rail to the differential output ($V_{\rm o3p} - V_{\rm o3n}$) has been simulated to assess the PSRR. Due to a symmetrical R_L and the equal (and high) output impedance of the DCB, the PSRR with respect to $V_{\rm DD25}$ is > 48.1 dB. This is a significant result as $V_{\rm DD25}$ is generally just utilized for I/Os featuring weaker quality when comparing it with the core supply. Differently, the PSRR with respect to $V_{\rm DD12}$ and $V_{\rm SS12}$ are just 13.5 and 12.75 dB, respectively. Multiple pads were therefore assigned between $V_{\rm DD12}$ and $V_{\rm SS12}$ to minimize noise coupling and the effect of bondwire inductance on performance degradation.

VGC on $\rm S_{11}$ and Linearity: Accounting a bondwire inductance of roughly 3.5 nH, and a 1-pF input parasitic capacitance due to the bondpad and ESD protection circuitry, the simulated AC responses and S_{11} against gain control are shown in Fig. 12(a) and (b), respectively. $S_{11} < -10$ dB is achieved up to 4 GHz. For the linearity against VGC, from the highest to lowest gain levels, the IIP2 ranges from $+45$ to $+59$ dBm, whereas the IIP3 ranges from $+5.6$ to $+17$ dBm.

IV. Current-Reuse Mixer-LPF

A. Circuit Description

Typically in wireless receivers, the mixer and BB LPF are separately designed, and the signal transfer is processed in voltage. It implies that the out-of-channel interferers are amplified at the output of the mixer prior to adequate filtering. Here, with the use of a 2.5-V supply, more voltage headroom promotes the use of a *current-mode* LPF to interface (cascode) with the mixer, offering adequate filtering prior to BB I-V conversion. Fig. 13 shows the I-channel of the proposed I/Q mixer-LPF. A polyphase double-balanced topology is selected to lower the LO-to-BB leakage and even-order distortion while rejecting the third and fifth harmonics of the LO. The HR mixer core is based on a switched-$g_{\rm m}$ cell [13], which is favored against the Gilbert cell in terms of operating voltage. Moreover, the LO path induces only common-mode noise at the outputs that can be rejected differentially. Also thanks to the 2.5-V supply, $M_{\rm m1}$–$M_{\rm m4}$ can feature a large V_{GS}, and use source degeneration ($R_{\rm deg}$) to enhance their linearity and output resistance.

The LO buffers realized as CMOS inverters use cross-connected weak latches to minimize the duty-cycle distortion. Small LO buffer's ON-resistance reduces the RF-to-LO coupling since $M_{\rm m1}$–$M_{\rm m4}$ can be well-grounded when they are

in ON state. Assuming a square-wave like LO, the conversion gain (CG) in 4-phase and 8-phase operations are given by

$$CG_{4P}(s) = cg_{\mathrm{m,eff}}(2+\sqrt{2})\left(R_{\mathrm{BB}} \parallel \frac{1}{sC_{\mathrm{BB}}}\right) H_{\mathrm{Biq}}(s) \quad (14)$$

and

$$CG_{8P}(s) = cg_{\mathrm{m,eff}}(2\sqrt{2})\left(R_{\mathrm{BB}} \parallel \frac{1}{sC_{\mathrm{BB}}}\right) H_{\mathrm{Biq}}(s) \quad (15)$$

where $\mathrm{c} = 2/\pi$, accounting that only the 1st harmonic of the LO contributes to the gain. $g_{\mathrm{m,eff}}$ denotes the effective transconductance of M_{m1}–M_{m4} with resistive degeneration, i.e., $g_{\mathrm{m,eff}} = g_{\mathrm{m,Mm1}}/(1+g_{\mathrm{m,Mm1}}R_{\mathrm{deg}})$. $CG_{4\mathrm{p}}(\mathrm{s})$ intrinsically shows 1.6-dB higher gain than $CG_{8\mathrm{p}}(\mathrm{s})$ since the polyphase paths in the 4-phase mode are directly parallelized. This gain difference is indeed helpful as the L band that uses a 4-phase LO is located much closer to the -3-dB cutoff frequency of the balun-LNA, where more gain droop exists. $H_{\mathrm{Biq}}(\mathrm{s})$ is the frequency response of a current-mode Biquad [14] with Q and cutoff frequency Ω_0 as given by

$$H_{\mathrm{Biq}}(s) = \frac{i_{\mathrm{out}}(s)}{i_{\mathrm{in}}(s)} = \frac{\frac{g_{mf}^2}{C_{f1}C_{f2}}}{s^2 + s\frac{g_{mf}}{C_{f1}} + \frac{g_{mf}^2}{C_{f1}C_{f2}}},$$
$$Q = \sqrt{\frac{C_{f1}}{C_{f2}}}, \qquad \omega_0 = \frac{g_{mf}}{\sqrt{C_{f1}C_{f2}}}. \quad (16)$$

This Biquad exhibits several distinct advantages [14]: 1) the Q of the complex pole pair is insensitive to process; 2) there is no passband loss as the current gain at dc is unity; 3) a constant-Q BW control can be achieved with C_1 and C_2 tuned together; 4) the Biquad exhibits a zero in the noise transfer function of M_{f1}–M_{f4} (to be described later), resulting in in-band noise reduction. This property breaks the fundamental kT/C limit of in the classic LPFs where the noise behavior should follow the LPF's profile [14]; 5) high linearity is achieved since filtering is performed in the current mode, while C_{f1} filters out the high-frequency signals prior to reaching the active elements (M_{f1}–M_{f4}); 6) the noise and linearity are tradable with the cutoff frequency. A higher cutoff rejects more in-band noise because of the zero exhibited at DC.

These good noise and linearity properties render it a wise "first filter" in direct-conversion receivers. Here, by integrating it with the mixer having a real pole load $[R_{\mathrm{BB}}//(1/\mathrm{s}C_{\mathrm{BB}})]$, a third-order LPF can be constructed without extra bias currents, V-I and I-V converters that dominate the NF [14]. The BB output common-mode voltage is controlled via a common-mode feedback circuit around M_{L1}–M_{L2}. The targeted cutoff frequency is 12 MHz to balance the NF and selectivity. An automatic cutoff tuning is beyond the scope of this work, but should be considered when accounting for process and temperature variations. A constant-Q BW tuning can be achieved via co-tuning C_{f1}, C_{f2} and C_{BB}. M_{f1}–M_{f4} are realized as thick-oxide MOS with a big device size to minimize NF and reduce channel-length modulation. The latter is essential for an accurate filtering profile.

The protection circuit depicted in Fig. 10 is also applied here at $v_{\mathrm{o1p,BB}}$ and $v_{\mathrm{o1}n,\mathrm{BB}}$ to prevent M_{m1}–M_{m4} (thin-oxide devices) from being overstressed during the start-up/power-down condition.

B. Noise Figure

The simplified noise model of the mixer-LPF is shown in Fig. 14. Similar to the noise analysis in Section III, it can be derived that the single-side band (SSB) NF is given by

$$NF_{\mathrm{SSB,MixLPF}}(s) = \underbrace{\frac{1}{c^2} + \frac{2\gamma}{g_{\mathrm{m,eff}}R_S c^2} + \frac{\frac{2}{R_{\mathrm{BB}}}}{R_S c^2 g_{\mathrm{m,eff}}^2 H_{\mathrm{Biq}}^2(s)}}_{\text{switche-gm mixer contribution}} + \underbrace{\frac{2\gamma g_{mf}\left[\frac{s\frac{g_{mf}}{C_{f2}}}{s^2+s\frac{g_{mf}}{C_{f1}}+\frac{g_{mf}^2}{C_{f1}C_{f2}}}\right]^2}{R_S c^2 g_{\mathrm{m,eff}}^2 H_{\mathrm{Biq}}^2(s)}}_{\text{LPF contribution}} + \underbrace{\frac{2\gamma g_{mf}\left(\frac{sC_{f2}}{sC_{f2}+g_{mf}}\right)^2}{R_S c^2 g_{\mathrm{m,eff}}^2 H_{\mathrm{Biq}}^2(s)}}_{\text{LPF contribution}} \quad (17)$$

where C_{BB} is omitted and the noise due to the R_{deg} is ignored to simplify the expression. The first three terms of (17) are originated from the switched-g_{m} mixer the same as those derived in [13]. The last two terms are due to the Biquad, both are noise-shaped by an in-band zero as expected. Further design details of the mixer and LPF are omitted as their individual designs have been extensively addressed in [13] and [14], respectively.

C. Simulation Results

The filtering characteristic of the mixer-LPF is shown in Fig. 15. The passband gain and stopband rejection are increased progressively. The bias scheme of the mixer-LPF is a singled-ended replica of it generating V_{b} and the gate bias voltage of M_{m1}–M_{m4}, reducing the effects of process variation and mismatch. In Monte Carlo simulations, the -3-dB cutoff frequency shows a mean of 12.9 MHz with a reasonable σ of 0.636 MHz. The passband gain variation is from 8.6 to 12.2 dB. A stable 60-dB per decade stopband attenuation is achieved at the output. Other simulated performances metrics are summarized in Table I.

V. Multi-Phase LOG

A. Brief Overview

Multiphase LOGs have been extensively studied in wireless/wireline applications. A solution based on inverter-based ring-VCO [15] is compact and has wide-range tunability, but the phase noise is still high for most high-tier wireless systems. Lowering the phase noise promotes the use of coupled LC-VCOs [16]. The overhead is the excessive number of inductors which will occupy a considerable amount of chip area. A delay-locked loop (DLL) offers another way to realize a multiphase LOG [17]. Regrettably, since it is based on delay

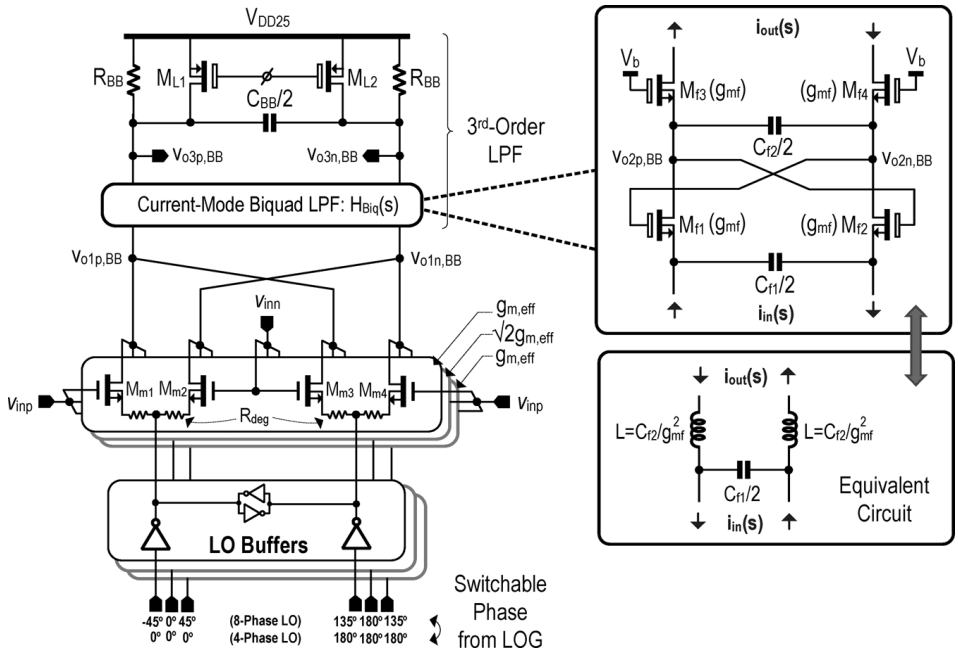

Fig. 13. Proposed current-reuse I/Q mixer-LPF topology.

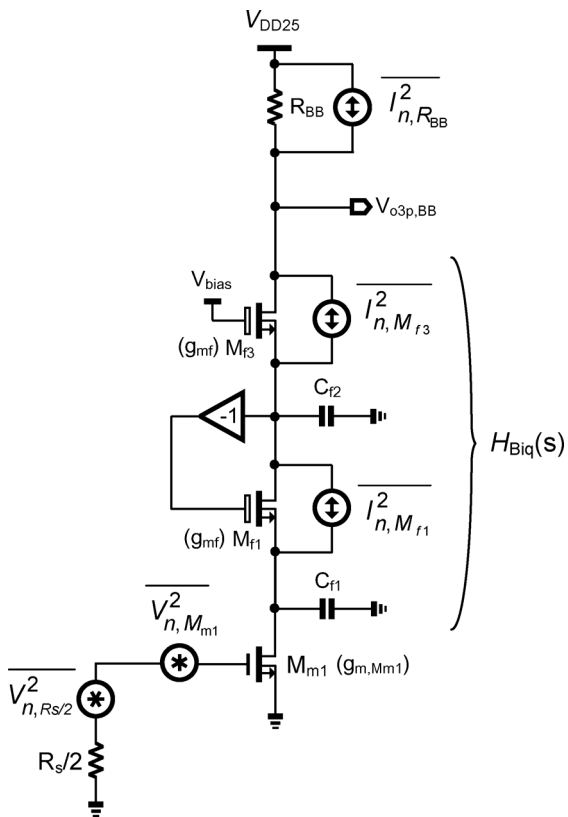

Fig. 14. Noise model of the current-reuse mixer-LPF.

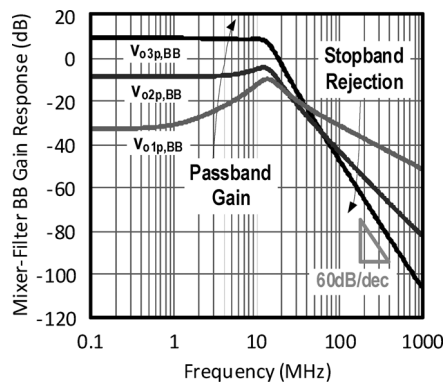

Fig. 15. Simulated mixer-LPF's gain-filtering characteristics.

TABLE I
PERFORMANCE SUMMARY OF THE CURRENT-REUSE MIXER-LPF (SIMULATION)

Parameters		Value
-3dB Cutoff (MHz) (Monte Carlo Simulation)	Mean	12.9
	σ	0.636
LPF Stopband Profile (dB)		60/decade
Conversion Gain (dB)		10.5
DSB NF (dB)		15.2
Out-of-Channel IIP3 (dBm)		+15.7
Input Capacitance (fF)		43
Power (mW)		9.8

* 2 tones at [f_{LO}+20MHz, f_{LO}+31MHz]
IMD_3 @ 9MHz, IMD_2 @ 11MHz after mixing

units, the phase-noise performance is heavily dependent on the number of output phases required. Currently, the most common solution is LC-VCO plus frequency dividers [7]. For instance, a quadri-phase LO can be generated via a divide-by-2 circuit. This division implies that the associated PLL and VCO have to operate at a doubled frequency of the output. Thus, the design complexity dramatically rises with the number of phases required, without mentioning the power, phase noise and phase error overheads. Moreover, the PLL and VCO will be more sensitive to parasitic capacitances, implying narrower locking and tuning ranges, respectively.

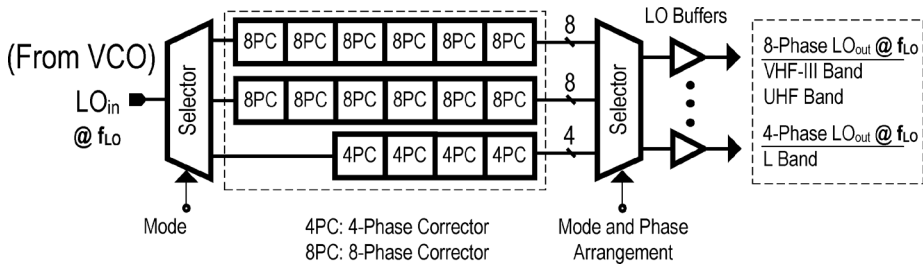

Fig. 16. A direct Injection-locked 4-/8-phase LOG.

B. Open Loop Multi-Phase LO Generators (Conventional and Proposed)

Recently, an open-loop quadri-phase clock generator for wireline applications was proposed to surmount these constraints [18]. Unlike the active polyphase filter entailing both inverters and capacitors [19], each phase corrector involves only inverters in a ring oscillator configuration with interpolation for multi-phase outputs, resulting in a much more compact area with a wider tuning range. The phase precision can be optimized by increasing the number of phase correctors in cascade. A master LO direct injection-locks the chain and defines the steady-state frequency. The tuning range depends on the reference LO and the lock range of the phase correctors; both can be optimized via proper sizing of the associated inverters. The prime advantages of this method are its simplicity (i.e., open loop and inverter only), wide bandwidth and the lack of power-hungry buffers. Moreover, the frequency of the driving source can be the same frequency as the multi-phase outputs. The achieved frequency range in [18] for a quadri-phase output is 0.37 to 2.5 GHz, but the phase error is limited to 5°.

Here, the proposed 4-/8-phase LOG extends such a concept, appropriately narrowing the coverage of the LOG by using three chains of 4-/8-phase correctors individually optimized for a specific band. As such, and through circuit-level optimization, the phase error is controlled within 1° (simulation), being more suitable for wireless applications.

The block schematic of the proposed 4-/8-phase LOG is depicted in Fig. 16. It is based on two chains of 8-phase corrector (8PC) and one chain of 4-phase corrector (4PC); each is dedicated to a specific mobile-TV band for minimum phase error. Selectors with logic arrangement feature assign the correct LO phase to each mixer in different modes. The injection signal $\mathrm{LO_{in}}$ might cover the desired bands by using a 1.27-to-1.92-GHz PLL+VCO [20] (not integrated in this work) with selectable output division ratios (1, 2, 3, 6 and 8). This LO plan corresponds to 3.8x relaxation of the PLL+VCO's operation frequency when comparing it with [9]. Note that, here, the required division ratios can be of *any* number as they are unrelated to the phases of $\mathrm{LO_{out}}$. In the L band, the PLL+VCO works at the same RF frequency.

C. Circuit Implementation and Simulation Results

Only the circuit implementation of the 8-phase path is presented as the 4-phase one can be considered as its subset extensively analyzed in [21]. As shown in Fig. 17(a), $\mathrm{LO_{in}}$ drives a chain of all-digital 8PC to progressively improve the phase precision of the 8-phase $\mathrm{LO_{out}}$. A high-level algorithm has been developed in MATLAB to optimize the device size, number of stages and frequency range using a linearized model [21]. At the transistor level, each 8PC comprises 32 inverters classified into two types and three sets as depicted in Fig. 17(b). *L*-type features a larger device size than *S*-type for optimizing the phase correctability of each 8PC. Set A is to interpolate the intermediate phases. Set B is to suppress the self-oscillation frequency and thereby enlarging the locking window. Set C is for injection lock and direct stage-to-stage cascading. The entire LOG is implemented with thin-oxide MOSFETs operating at a 1.2-V supply.

The phase precision of the LOG is mainly limited by the routing in layout, where the transistor intrinsic *RC* value is sensitive to the parasitics. The LOG was laid out and extracted to tune out this effect in several iterations. In the post layout simulation (PLS), the phase error for 8-phase output is optimized to be $< 1°$ for the VHF-III and UHF bands. This precision fairly meets our target of HR ratio of 33 dB, even under a possible gain mismatch up to 5%. For the 4-phase output, the phase error is controlled to be less than 1.5° for the L band, which corresponds to an image rejection ratio of around 38 dB for a possible gain mismatch up to 2.5%.

Similar to ring oscillators, the robustness of the phase corrector can be improved by adopting a supply regulator and a Bandgap reference to cope with the voltage and temperature variations, respectively [22], [23]. Simulations show that the phase noise of the multi-phased LO will not be degraded by more than 1 dB (at 1-MHz frequency offset) if the random noise superimposed on the supply is less than 80 mV.

VI. Measurement Results

Prototypes of the RFE were fabricated in 65-nm CMOS. Deep n-well was employed for essential bulk-source connection of certain nMOS devices (e.g., the ones in cascode). The chip micrograph is shown in Fig. 18. The active die area is 0.46 mm^2. A production socket was employed to facilitate tests of multiple samples under the same fixture and environment. Particular attention has been paid to the layouts of the LOG and 8PC to avoid parasitic mismatches that can lead to systematic phase error in the LOG.

A. The RFE

The RFE measures 35 ± 1-dB maximum voltage gain, 4 ± 0.2-dB NF, 43-to-55 mW power consumption over the desired bands [Fig. 19(a)]. The BB gain responses show

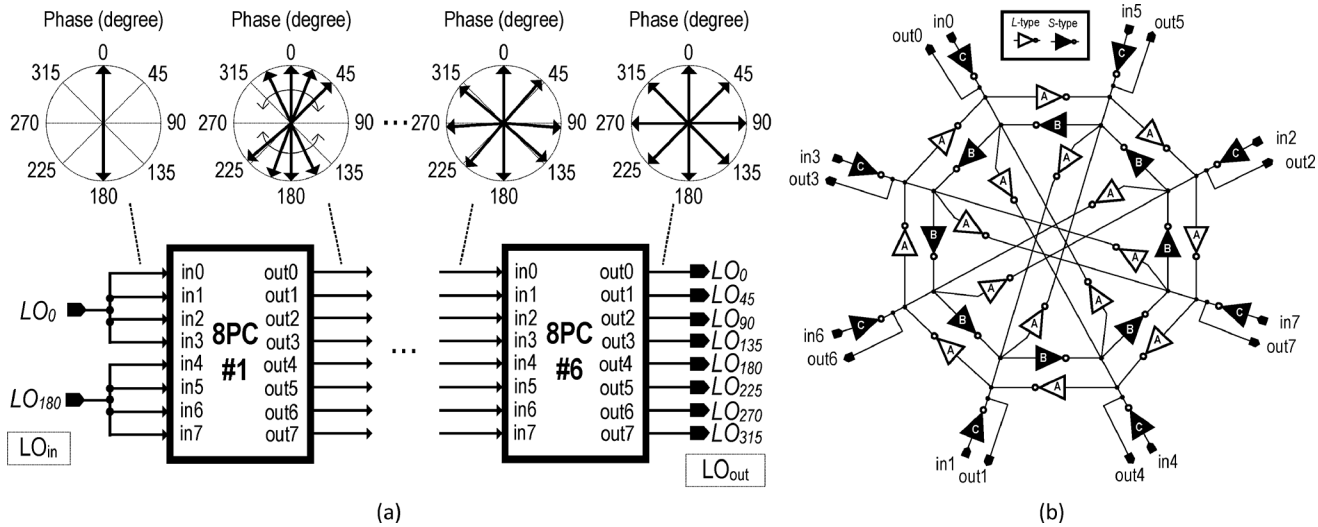

Fig. 17. The 8-phase path of the LOG: (a) architecture and operating principles, and (b) schematic of each 8PC.

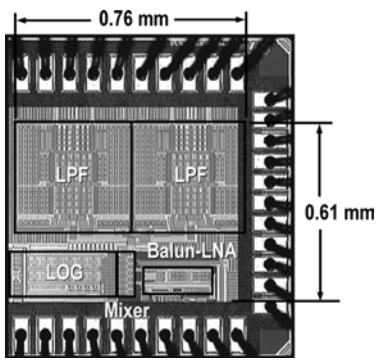

Fig. 18. Chip micrograph of the implemented RFE.

60-dB/dec rejection and a constant cutoff of around 12 MHz against gain [Fig. 19(b)]. The cutoff was not made tunable in this prototype. The key distortion specification is justified by the out-of-channel linearity [1]; two tones are applied at [f_{LO} + 20 MHz, f_{LO} + 31 MHz] with a power level sweeping from -40 to -20 dBm. The measured IIP3 is around $-3.4/+11$ dBm at the highest/lowest gain by tuning the ATT gain steps [Fig. 19(c)]. The IIP2 yields less variation (32 to 35 dBm) against gain change. The concerned HR ratios (HRRs) are $HRR_3 = 35$ dB and $HRR_5 = 39$ dB, aligning with that achieved in a typical HR mixer [8]. Note that to increase the data accuracy; the IIP2/HRR_3/HRR_5 is averaged from 12 samples with σ of 3.9/1.8/2.4 dB. The worst S_{11} is close to -10 dB [Fig. 19(d)], which is degraded comparing with the simulations [Fig. 12(b)]. The bondwire, test socket and PCB parasitics should account for the discrepancy. The S_{11} curves are consistent to the designed values of 34.8 Ω at high gain mode (without ATT) and 55 Ω at low gain modes (with ATT).

Based on transient measurements, we can justify that the BB differential outputs [Fig. 20(a)] and I/Q outputs [Fig. 20(b)] are of high-precision balancing, less than 0.5 dB gain and 1.2° phase errors in downconverting a single tone from 205 to 1 MHz.

B. The LOG

The performance of the LOG in each band was characterized using a signal generator as LO_{in}. The added phase noise [Fig. 21(a)–(c)] is well below to that achieved in [1] which uses a practical PLL+VCO as LO_{in}. Thus, the phase noise induced by the LOG should be tolerable when the PLL+VCO is present.

The injection-locking characteristic of the LOG is of interest. When LO_{in} is deactivated [Fig. 22(a)], LO_{out} is free-running at its natural oscillation frequency of around 240 MHz and noticeable spurious tones appear throughout the spectrum. With LO_{in} activated with a frequency of 205 MHz, LO_{out} tracks LO_{in} at the same frequency and the dynamic range is > 60 dB [Fig. 22(b)]. Note that the 2nd-6th harmonics will be suppressed by the differential I/Q mixer with HR. These results demonstrate that a high-purity multi-phase LO can be achieved without frequency division.

C. Performance Comparison

Benchmarking with the state-of-the-art wideband RFEs that attain 4-dB NF [9], [24] in Table II, this work succeeds in extending the operating BW and BB selectivity with comparable power, while reducing the external parts, chip area and f_{LO} that can ease the design of the PLL and VCO. We note that the on-chip HRR can be further enhanced by incorporating the two-stage HR technique [9]. Though the pre-gain pre-filtering technique [24] also can enhance the HRR and lower the power, it involves hard tradeoffs in impedance match, IIP3 and consistency of in-band performances.

VII. Conclusion

A 65-nm CMOS RFE composed of a wideband balun-LNA with VGC, current-reuse I/Q mixer-LPFs and a direct injection-locked 4-/8-phase LOG has been described. Comparing with the existing wideband RFEs, the external parts and repeated RF circuitry are reduced and the required master LO frequency is relaxed. The RFE exploits a dual 1.2/2.5-V supply, allowing more functions to be implemented in the current domain.

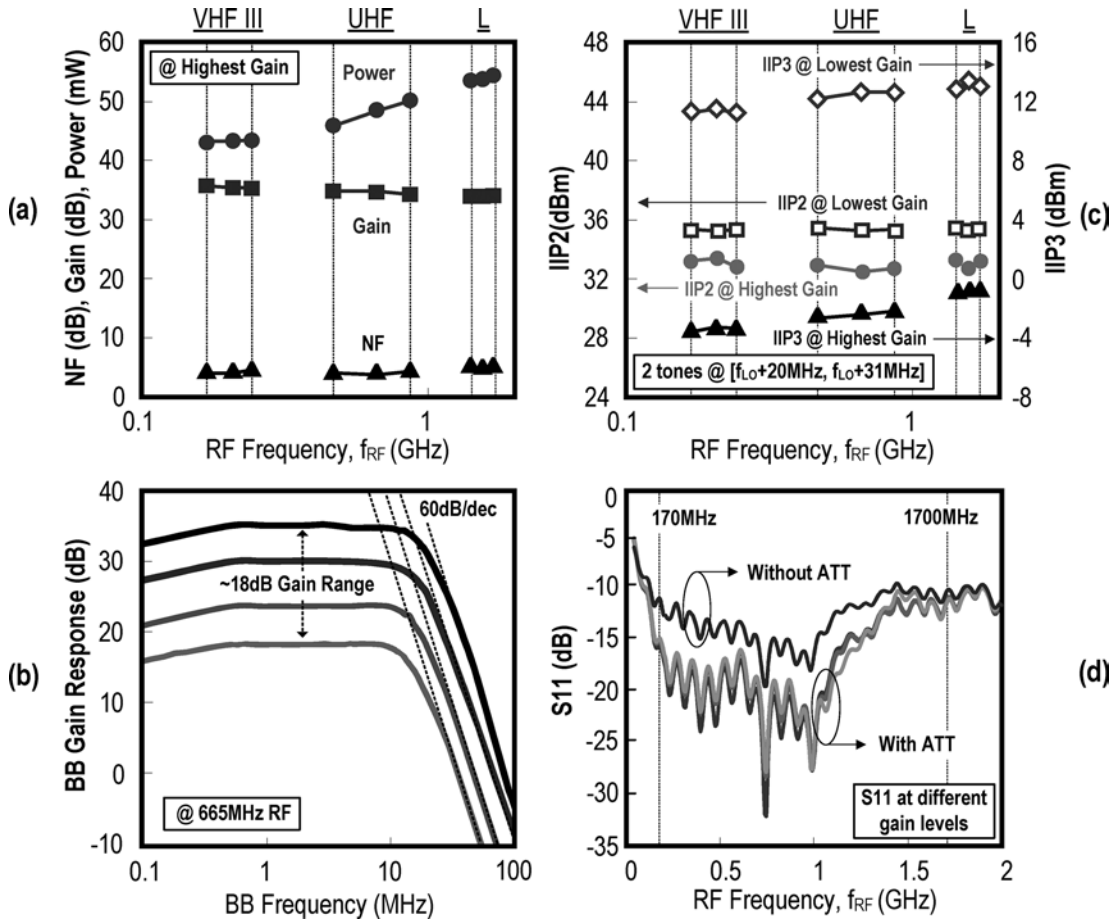

Fig. 19. Measured RFE's (a) NF, gain and power. (b) BB gain responses. (c) IIP2 and IIP3. (d) S11.

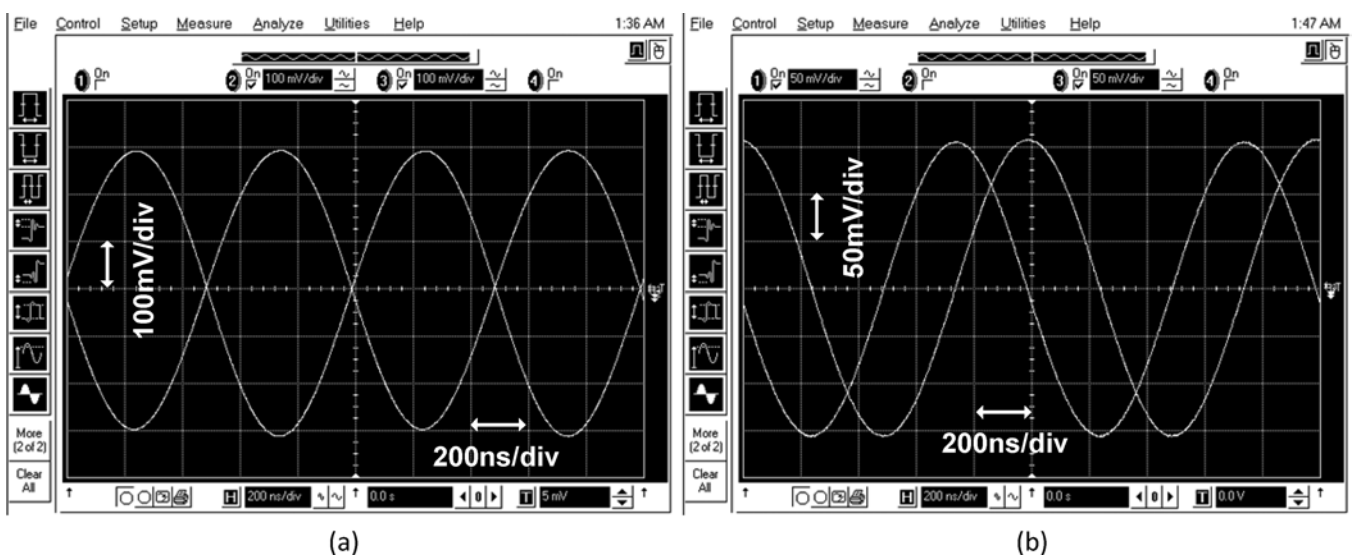

Fig. 20. Measured RFE's (a) differential and (b) I/Q outputs under single-tone downconversion from 205 to 1 MHz.

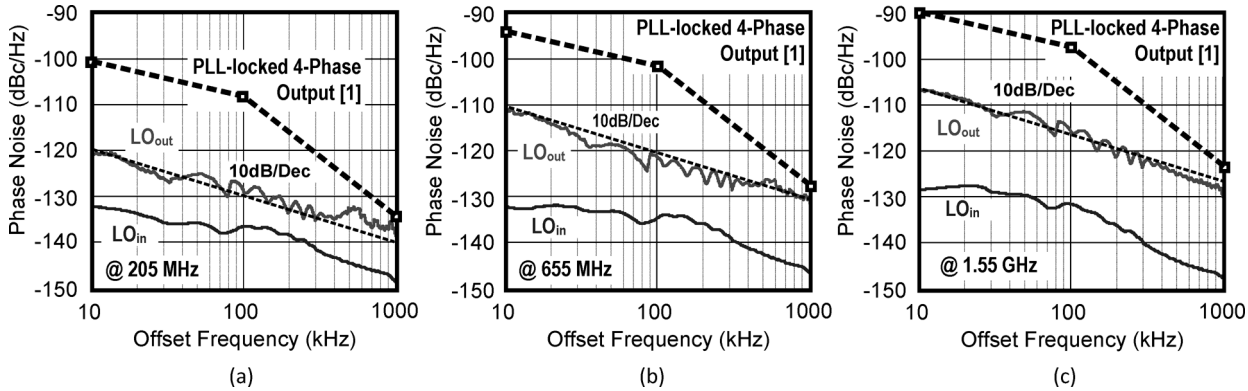

Fig. 21. Measured phase noise of the LOG in each band comparing with the data given in [1]. (a) 8-phase at 205 MHz. (b) 8-phase at 655 MHz and (c) 4-phase at 1.55 GHz.

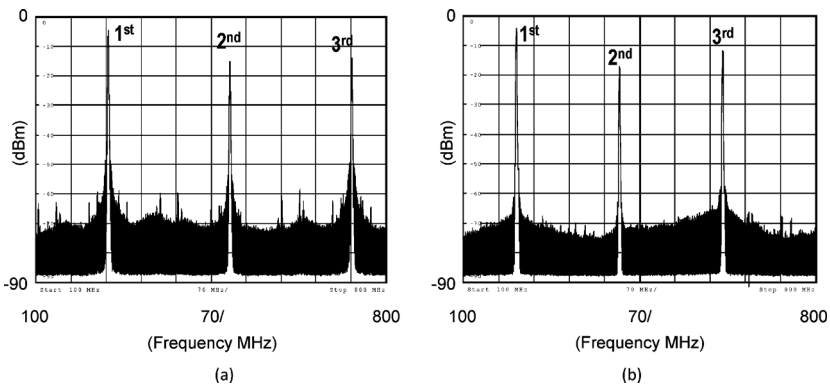

Fig. 22. Measured injection-locking characteristic of the LOG: (a) free-running at $\sim$ 240 MHz. (b) Injection-locked at the desired 205 MHz.

TABLE II
MEASUREMENT SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART WIDEBAND RFEs

Parameters	This Work and [3]	ISSCC 2009 [9]	JSSC 2010 [24]
Operation Frequency f_{RF} (GHz)	**0.17 to 1.7** [A]	0.4 to 0.9	0.3 to 0.8
Required Master LO Frequency f_{LO} (GHz)	**$f_{LO} = f_{RF}$ (4 and 8 Phases)**	$f_{LO} = 8\, f_{RF}$ (8 Phases)	$f_{LO} = 4\, f_{RF}$ (8 Phases)
Maximum Gain (dB)	**35**	34	22 to 28 [C]
RF Gain Control (dB)	**17 to 35**	No	No
External Components	**1 Inductor**	2 Inductors and 1 Balun	2 Inductors
Area (mm^2)	**0.46**	1	0.5
BB Filter Order	**3rd-Order LPF (1 biquad + 1 real)**	2nd-order LPF (2 real poles)	1st-order IIR LPF (minor channel selectivity)
Power (mW) @ f_{RF} (GHz)	**55 @ 1.7** [D]	60 @ 0.9	18 @ 0.8
Input Impedance Matching	**Matched**	Matched	Unmatched
DSB NF (dB)	4 [Spec: 4] [B]	4	0.8 to 4.3 [C]
IIP3 (dBm)	-3.4 [Spec: -5] [B]	3.5	-14 to -9 [C]
IIP2 (dBm)	32 [Spec: 27] [B] (Balun LNA)	46 (Differential LNA)	38 to 49 [C] (Balun LNA)
HRR_3 (dB)	35	60	60
HRR_5 (dB)	39	64	60
Supply Voltage (V)	1.2 and 2.5	1.2	1.2
Technology	65nm CMOS	65nm CMOS	65nm CMOS

A: VHF III, UHF and L bands B: from [1] C: In-band variation
D: Balun-LNA (11.6 mW), I/Q mixer-LPFs (19.6mW), LOG + LO buffers (24mW at 1.7GHz, 12mW @ 170MHz)

The output balancing of the balun-LNA is enhanced by a capacitively cross-coupled cascode stage, and baseband selectivity is efficiently implemented via a current-domain Biquad merged with the mixer. Device reliability is ensured via a hybrid use of thin- and thick-oxide MOSFETs and voltage-conscious biasing. The fabricated prototypes meet the key specifications of mobile TV with a small die size of 0.46 mm^2.

ACKNOWLEDGMENT

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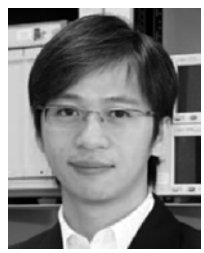

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