A 10-bit 500-MS/s Partial-Interleaving Pipelined SAR ADC With Offset and Reference Mismatch Calibrations

Yan Zhu, *Member, IEEE*, Chi-Hang Chan, *Member, IEEE*, Seng Pan U, *Fellow, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

***Abstract*— A 10-bit 500-MS/s partial-interleaving pipelined successive approximation register (SAR) analog-to-digital converter (ADC) architecture is presented that implements a full-speed 2-bit/cycle SAR at the front end with interleaved residue MDACs and SAR ADCs at the back end. This architecture achieves high speed, while preventing the interleaving spurs. In addition, the design considerations and calibration techniques for gain and offset are also introduced. A histogram stage gain error (HSGE) calibration is implemented to correct the conversion nonlinearities in the digital domain. Measurement results on a 65-nm CMOS prototype show an signal-to-noise distortion ratio (SNDR) of 55.9 dB at dc input and a figure of merit (FoM) of 32 fJ/conversion step at 1.2 V supply.**

***Index Terms*— Offset calibration, partial interleaving (PI), pipelined-SAR, stage-gain error calibration.**

I. Introduction

BATTERY-POWERED mobile applications strongly call for low-power and high-speed ADCs. For moderate resolution (>9 bit), SAR and pipelined SAR [1]–[7] ADCs can achieve low power but not high speed. Among the reported designs, SAR-type ADCs employing a single channel face a limited speed (<300 MS/s) [1]–[4]. Even utilizing a two-way interleaved scheme, such as [5]–[7], their speed may not be as high as some signal channel pipelined ADCs [8], [9]. Indeed, incorporating larger number of interleaving channels can further extend the speed of SAR-type ADCs [10], [11] but their power efficiency are not good, due to the implementation of power hungry track and holds (T/Hs) or precise clock distribution paths. For instance, if a 10-bit TI SAR ADC is designed to achieve a conversion rate of 500 MS/s, where the ADC is built with five time-interleaved channels, it is necessary to suppress 1σ of timing mismatch at 280 fs. In general, designing the clock skew at hundreds of femtoseconds is challenging and the time calibrations [11]–[13] are necessary to suppress time spurs implying extra digital overhead. Therefore, in order to achieve both high resolution and high speed without utilizing time calibration, one of the main design challenges would come from the sampling front end.

A partial-interleaving (PI) pipelined-SAR architecture [14] was proposed that implements a high-speed 2-bit/cycle SAR ADC for the front-end sampling and conversion, where the residue multiplying digital-to-analog converter (MDAC) and the second-stage ADC are interleaved at the back end. The architecture eliminates the sampling mismatches from the interleaving scheme that also significantly save the power budget for clock generation as well as additional time calibration. This paper analyzes some conversion nonidealities in the PI pipelined-SAR architecture including mismatches from offset and gain, the back-end interleaving switches and the stage-gain error. The on-chip offset-cancellation technique [7] is optimized to compensate offsets from both Op-Amp and comparator. In addition, the stage-gain error is estimated and corrected in the digital domain by a proposed histogram stage gain error (HSGE) calibration.

II. ADC Architecture

Fig. 1 shows the ADC architecture and its timing diagram. The first stage contains a high-speed 6-bit, 2-bit/cycle SAR ADC and ping-pong residue MDACs ($MDAC_{1,1}$ and $MDAC_{1,2}$). The use of interpolation can reduce the number of required capacitive DACs for 2-bit/cycle operation from original 3 to 2; therefore, two differential DACs (DAC_1 and DAC_2) are used for the front-end sampling and conversion. Only the DAC_1 is shared by the TI-MDACs. As the DAC_2 is not involved in amplification, for conversion matching it contains a dummy array, whose total capacitance is the same as MDAC [14]. The second stage consists of two-way TI-SAR ADC to determine the fine 5-bit output. Each SAR is built

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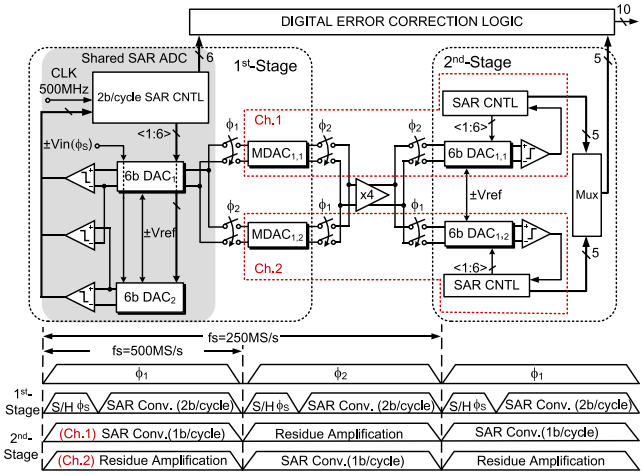

Fig. 1. ADC architecture and timing diagram.

with a 6-bit split-DAC, a comparator, and SAR control logic, where an extra bit is implemented for offset cancellation [7]. Two stages have 1-bit overlapping for digital error correction, which relaxes the conversion accuracy of the first stage to 7 bit.

During the sampling phase ($\phi_s = \phi_1 = 1$), the input signal V_{in} is sampled onto the DAC_1, DAC_2, and $\text{MDAC}_{1,1}$ simultaneously. In the conversion phase ($\phi_1 = 1$), the first stage resolves the coarse 6 bit in three conversion cycles (1.2 ns). When the conversion is completed ($\phi_2 = 1$), the $\text{MDAC}_{1,1}$ disconnects from the DAC_1 and employs to the input of the Op-Amp. The residue generated at the top plate of $\text{MDAC}_{1,1}$ is amplified and then sampled by $\text{DAC}_{1,1}$ in the second-satge SAR. Meanwhile, the first-stage DAC_1 switched to $\text{MDAC}_{1,2}$ starts an incoming sampling. When the fine 5 bit are determined in the second stage, they pass to digital error correction logic for the final 10-bit outputs. The front-end SAR ADC operates at 500 MS/s, while each interleaved channel works at 250 MS/s with an equivalent duration of 2 ns to perform the amplification and conversion, respectively.

This design implements a stage gain of 4 [3] instead of 8 or 16 [4]–[7]. The lower stage gain reduces the output swing of the amplifier and increases the closed-loop bandwidth that is appropriate for high-speed designs. With a flip-around operation [7], the required open-loop gain is $\geqq$42 dB. Moreover, as the amplification period is 2 ns, assuming the slew rate occupies 20%, the required gain bandwidth (GBW) is $\geqq$1.38 GHz. The op-amp implemented as a telescopic with gain-boosting topology [7] achieves 1.7-GHz bandwidth and 69-dB dc gain, which is sufficient to suppress the Op-Amp's finite gain error as well as the memory effect.

III. Circuit Techniques and Implementation

The proposed PI pipelined-SAR ADC architecture interleaves the residue amplification instead of sampling network that reduces the timing and bandwidth mismatches for high-frequency input, as the signal amplified to the TI channel is the residue after 6-bit quantization that would be static. However, the back-end TI channels still suffer the mismatches from gain and offset. In addition, the signal feedthrough via the TI switch affects the amplification accuracy. This section discusses the design nonidealities due to signal coupling from the TI switch as well as the mismatches from offset, gain, and reference voltages. The corresponding calibration and circuit techniques are also introduced.

A. First-Stage SAR ADC

The implementation of the first stage SAR ADCs is shown in Fig. 2. It consists of a 6-bit DAC_1, ping-pong residue MDACs, an SA controller (CNT), and offset calibration logic (CAL LOG). The input signal is precharged at the top plate of the entire array. During bit cycling, the $\text{MDAC}_{1,1}$ involved in the SA conversion is grounded, which scales down the reference voltages by 2 [4], [7]; therefore, two reference voltages $\pm V_{\text{ref}}$ match with the full-scale rail V_{FS} (1.2 V_{p-p}). Meanwhile the other $\text{MDAC}_{1,2}$ performing the flip-around $\times 4$ amplification feeds back 16 units of total 64C to the output of the Op-Amp. The TI switches S_{S1} and S_{S2} implemented in series with the sampling switch S_{S0} at the top plate increases the *RC* time constant required for each bit settling, while the settling accuracy is relaxed to $\pm 1/2^8$ V_{FS} due to 1-bit digital error correction. The 6-bit DAC is segmented to unit element per 2 bit instead of binary array to improve the conversion linearity and avoid the complex decode logic in SAR controller. The desired unit capacitor matching ($\Delta C/C$) is 0.8%. A custom-designed unit capacitance of 5.5 fF is formed with fringe structures (2 μm $\times$ 2.4 μm) using the metal layers (first to fifth). The 6-bit DAC and each MDAC contain the same total units of 64C (352 fF). The total input capacitance is 1.4 pF (single ended, excluding PAD, and ESD device), half of which is from DAC_2 in Fig. 1. The synchronous SAR control logic is designed with a bit cycle of 400 ps.

Moreover, one benefit of the PI architecture is the high immunity to the reference noise during the amplification, since the 48 units in TI-MDACs are connected to common-mode voltage V_{cm} instead of the reference voltages, which provides a differential cancellation of the common-mode variations. The reference noise due to switching transition is critical, especially in the TI-scheme, where the multiple channels are sharing the same reference source and performing the SA conversion simultaneously, the conversion in each channel interferes with each other through the reference voltages, and finally leading to signal-dependent errors [15].

B. Optimized Offset-Cancellation Technique

In this design, the offset mismatch is contributed from three comparators in the first stage to perform 2-bit/cycles operation, the Op-Amp and two comparators in the second stage. Since the first-stage SAR and the Op-Amp are shared by two channels and the use of digital error correction relaxes the total input referred offset requirement to $\pm 1/2^7$ V_{FS}, i.e., 18.75 mV_{p-p}. When its value exceeds the requirements, large conversion distortion occurs because the residue saturates the full scale of the second stage. Therefore, the offset voltage of three comparators needs to be suppressed within desired level. Assuming that the offset-mismatch components δ_{OM} are Gaussian random variables with a standard deviation of σ_{OM},

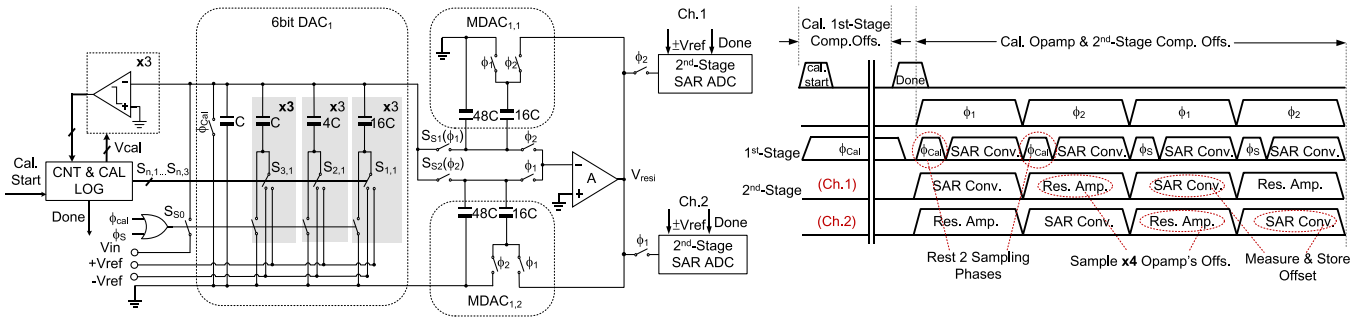

Fig. 2. First-stage SAR ADC and offset calibration timing diagram of two stages.

the SNDR considering the offset mismatch can be calculated as [16]

$$\text{SNDR} \approx 20\log\left(\frac{\text{Amp}_{\text{in}}}{\sqrt{2}\sigma_{\text{OM}}}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \quad (1)$$

where Amp_{in} is the amplitude of the input signal, and M (>1) is the number of TI channels. Since 2 bit/cycle is determined by three comparators, it can be equivalent to the operation in the three TI channels. Considering that the limited SNDR of a 6-bit ADC is 38 dB, the expected SNDR from offset mismatch needs to be designed higher than this level. To achieve 42-dB SNDR with Amp_{in} of 1.2 V and M of 3, the $\sigma_{\text{OM}-1\text{st}}$ of offset mismatch in the first stage should be <8.2 mV. The offset mismatches in the second-stage comparisons cause spurs. As this design targets 10-bit resolution (SNDR = 62 dB), also 4-dB design margin is left for offset mismatch. According to (1) and stage gain of 4, the $\sigma_{\text{OM}-2\text{nd}}$ of input referred offset mismatch from the second stage should be suppressed less than 2.4 mV.

The offsets coming from the comparators as well as the Op-Amp are all calibrated on-chip. Fig. 2 shows the timing sequences of the offset calibrations. The comparator used in the first-stage SAR ADC is dynamic comparators [17] with PMOS input. When the calibration is activated (Cal.Start = 1 and $\phi_{\text{Cal}} = 1$), the DAC_1 will disconnect from the MDACs and reset to the common mode for the offset calibration in the first stage. As the calibration accuracy is relatively relaxed comparing with the second stage, the offsets can be compensated simply by adjusting the differential currents with extra calibration input pair [18]. Once the offset calibration in the first stage is completed, it will output a Done signal to enable the calibration for the second-stage SAR ADCs. In our previous design [7], the offset-cancellation technique compensates only the offset from the comparator in the second stage. The offset in the Op-Amp, which will be amplified by the stage gain, is tolerated by sizing up the input pairs. It increases the Op-Amp's input parasitic and degrades its noise performance. Therefore, in this design, the offset-cancellation technique is optimized to cover both offsets from the Op-Amp and the comparators in the second stage to improve the robustness of the design. As shown in Fig. 2, the first-stage SAR needs to reset during ϕ_{Cal}, before the normal sampling ϕ_S is enabled. Then, the first-stage SAR ADC performs the 6-bit conversion and generates a residue on $\text{MDAC}_{1,1}$. The residue together with the offset from the Op-Amp is amplified by 4 to the second-stage DAC. Similar to [7], the total offset, including the signal sampled from the first stage and the comparator's offset in the second stage, will be converted into 6-bit offset codes and stored in the CAL LOG. Since this action repeats twice, the offset can be measured in sequence and stored in the second stage. Once the calibration is completed, the ADC will be resumed to its normal operation.

C. Time-Interleaved Switches

While the PI operation avoids the timing mismatch, the TI switches S_{S1} and S_{S2} introduce the other nonidealities including sampling distortions from varying on-resistance, charge-injection, and signal feedthrough. According to the PI operation of the TI switches, (S_{S1}/S_{S2}) needs to be kept on during both sampling and conversion phases. Therefore, S_{S1}/S_{S2} cannot be bootstrapped to the input signal and the transmission gate switch is used, whose on-resistance varies from 27 to 42 Ω with W/L of an NMOS = 15/0.06 μm and a PMOS = 30/0.06 μm under a 1.2 V_{p-p} input. Thus, it limits the sampling total-harmonic-distortion (THD) to −76 dB.

The TI-switch also imposes the signal-dependent charge-injection ΔV_{CI}. Fortunately, the charge-injection error is not significant, as the switches are turned off at the end of conversion, where the residue is comparatively small (<18.75 mV_{p-p}). To guarantee 10-bit accuracy, ΔV_{CI} should be suppressed less than 563 μV_{p-p}. Assuming half of the charge is injected to the MDAC, the junction capacitance of the switch is required to be <6% of the total capacitance from MDAC, which is not more than 22.5 fF.

Except the nonlinear junction capacitor, the drain–source parasitics from the TI-switch cause the signal feedthrough, which disturbs the residue amplification. As shown in Fig. 3, while the $\text{MDAC}_{1,2}$ is amplifying the residue to the DAC in the second stage, the 6-bit DAC of the SAR connecting with $\text{MDAC}_{1,1}$ is performing the successive approximation. The signal coupling via parasitics of $S_{S2,p}$ and $S_{S2,n}$ to the Op-Amp's virtual ground causes oscillation, which affects the settling time and accuracy of the amplification. Therefore, the signal feedthrough compensation is required. In Fig. 3, the cross-coupled technique is utilized at the top plate of TI MDACs to provide signal cancellation from $V_{1,p}$/$V_{1,n}$ to $V_{2,n}$/$V_{2,p}$. The dummy compensation capacitor is implemented with MOS capacitor, which has the same size of the TI switches for better matching.

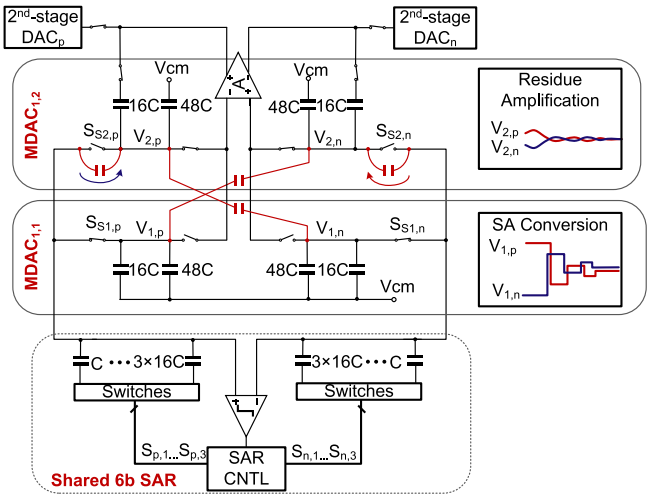

Fig. 3. PI operation in the first stage with cross-coupling signal compensation for TI switches.

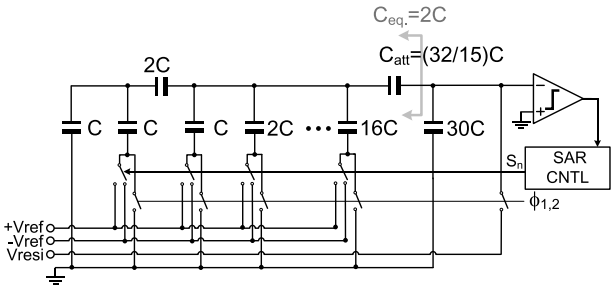

Fig. 4. Second-stage 6-bit SAR ADC.

Though the timing mismatch is avoided through architecture optimization, there still exists bandwidth mismatch between the ping-pong residual sampler, which comes from the mismatch of the sampling capacitor and the resistance of the sampling switch. The capacitor matching can achieve $\sigma\ (C_s)/C_s$ better than 0.1%, where C_s is the sampling capacitor. Its mismatch can be ignored. The switch resistance mismatch usually dominates. The matching requirement can be quite stringent, if the channel bandwidth is limited. Typically, the sampling bandwidth will be designed sufficiently large to reduce the sensitivity to the bandwidth mismatch. This design achieves a sufficient bandwidth of 8 GHz. In addition, according to Monte Carlo simulations it shows σ(BW)/BW of 1% that fulfills the design target. According to measurement results, the spur due to bandwidth/skew mismatch is below −73 dB at Nyquist input.

D. Second-Stage SAR ADC

The first stage resolves 6 bit and its reference voltage is ±1/2 V_{FS}. With the stage gain of 4 and 1-bit overlapping, the reference voltages for the second-stage SAR ADC are ±1/16 V_{FS} that is obtained by using a 6-bit split-DAC to scale down the reference voltages by 16 [7]. As shown in Fig. 4, the expected output equivalent capacitance C_{eq} is 2C ideally. With the 30 units kept grounded, $\pm V_{ref}$ is attenuated by 16. This approach saves additional reference generation as well as the power consumption, and also reduces the loading of the Op-Amp for better slew rate. On the other hand, since this design uses top-plate sampling, the mismatch of C_{att} and the top-plate parasitics cause a reference mismatch between two stages, which is discussed in Section III-E. The capacitance of C and C_{att} is implemented as 5.5 and 12 fF, respectively, which draws the total equivalent output capacitance to 176 fF. An asynchronous logic [19] used in the SAR controller achieves less than 330 ps for each bit cycling. The ADC determines 1 more bit only during the offset cancellation to attain the calibration accuracy.

E. Histogram-Based Reference Mismatch Calibration

Gain mismatch is originated by the mismatch in channel's dc gain, which is derived from the capacitor mismatches as well as finite Op-Amp gain error among the channels. Since the first-stage SAR and Op-Amp are shared, the gain mismatch between two channels is contributed from the TI-MDAC and the second-stage DACs, which can be represented as

$$\sigma_{\mathrm{GM-Sum}} = \sqrt{\sigma^2_{\mathrm{GM-MDAC}} + \sigma^2_{\mathrm{GM-2nd}}/G^2} \tag{2}$$

where the $\sigma_{\mathrm{MG-Sum}}$ is the total input referred gain mismatches. The $\sigma_{\mathrm{GM-MDAC}}$ and $\sigma_{\mathrm{GM-2nd}}$ represent the gain mismatch between MDACs and the second-stage DACs, respectively. The SNDR due to the channel gain mismatches can be derived as [16]

$$\mathrm{SNDR} = 20\log\left(\frac{1}{\sigma_{\mathrm{GM-Sum}}}\right) - 10\log_{10}\left(1-\frac{1}{M}\right). \tag{3}$$

According to (3) with target SNDR of 66 dB and M of 2, the $\sigma_{\mathrm{MG-Sum}}$ of total input referred gain mismatches should be <0.07%. Therefore, it requires that the gain mismatches $\sigma_{\mathrm{GM-MDAC}}$ is <0.05% and the $\sigma_{\mathrm{GM-2nd}}$ is <0.2%. The channel gain mismatch decided by the inhered capacitor matching is optimized by symmetrical layout routing. Eventually, the gain mismatch is not the main design limitation while the reference mismatch between two stages dominates.

Ideally, in an n-bit pipelined-SAR ADC implemented with a stage gain of G and 1-bit overlapping, the ratio between two reference voltages V_{ref1} and V_{ref2} in the first and second stages, respectively, can be represented as

$$\alpha_{id} = \frac{V_{\mathrm{ref1}}}{V_{\mathrm{ref2}}} = \frac{2^{i-1}}{G} \tag{4}$$

where i is the number of bit in the first stage. Since the signals are sampled at the top plate of the DACs in both first and second stages, the parasitic capacitance C_{P1} and C_{P2} (shown in Fig. 5) cause a ratio mismatch between two reference voltages, which can be derived as

$$\alpha_{\mathrm{err}} = \frac{2^{2i-j-1}(2^j C + C_{P2})}{G(2^i C + C_{P1})} \tag{5}$$

where j is the number of bit in the second stage. The ratio error appears as the same transfer characteristic of the stage-gain error at the ADC's output. Fig. 5 shows a 5-bit example where the first and second stages are both built with a 3-bit SAR ADC and the stage gain is set as 4 with 1 bit overlapping.

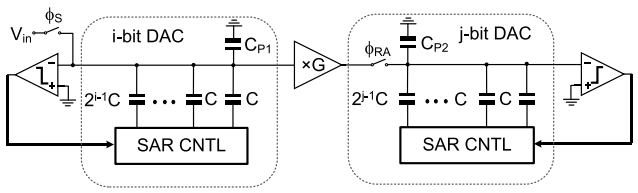

Fig. 5. n-bit ($n = i + k - 1$) pipelined-SAR ADC with i-bit in the first stage, k-bit in the second stage, and 1-bit overlapping.

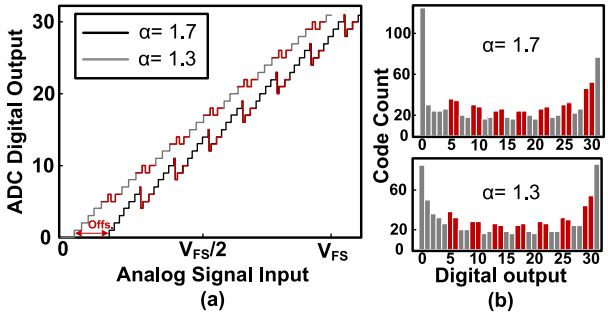

Fig. 6. (a) Transfer characteristic of 5-bit pipelined-SAR ADC with respect to $\alpha = 1.3$ and $\alpha = 1.7$. For the clarification, offset is added to the case of $\alpha = 1.7$. (b) Corresponding output code histogram of two cases with a sine wave input.

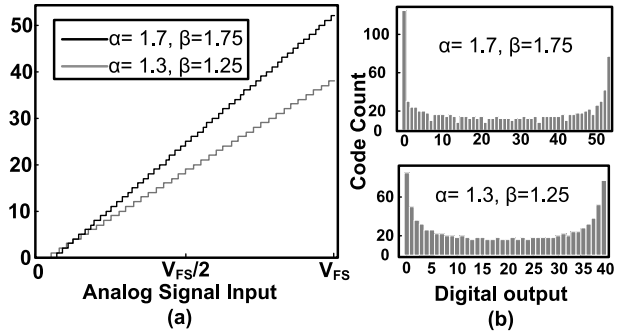

Fig. 7. (a) Calibrated transfer characteristic of 5-bit pipelined SAR with respect to $\alpha = 1.3$ and $\alpha = 1.7$. (b) Corresponding output code histogram of two cases with a sine wave input.

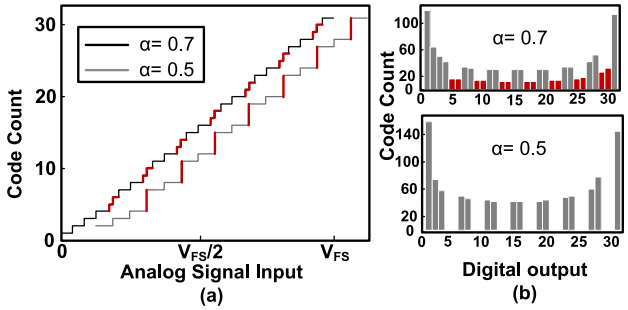

Fig. 8. (a) Transfer characteristic of 5-bit pipelined-SAR with respect to $\alpha = 0.5$ and $\alpha = 0.7$. (b) Corresponding output code histograms of two cases with a sine wave input.

According to (4), ideally, if two reference voltages match with each other, α should be 1 and the output of the ADC is linear. Once there is a large mismatch, systematic nonlinear errors appear at the output of the ADC. The transfer curves and the code histograms of the digital output are shown in Fig. 6, respectively. The digital outputs are nonmonotonic, which result in the corresponding positive differential nonlinearity (DNL) appeared in the code histogram in Fig. 6(b). Indeed, the nonlinearities can be compensated in the digital domain as

$$D_{\text{out,cal}}[B_{n+1}\dots B_1] = \text{fix}\left[\beta\sum_{n=1}^{i}2^{n+j-2}B_{n+j} + \sum_{n=1}^{j}2^{n-1}B_n\right] \tag{6}$$

where B_n equal to 1 or 0 represents the digital output. $[B_{n+1}\dots B_1]$ is the full output code before the digital error correction. By multiplying a gain factor β to i bit in the first stage, the nonlinear errors can be corrected correspondingly. The calibration concept is similar as [20], but the design consideration is different. Fig. 7 shows the calibrated outputs. However, the gain factor β cannot be easily estimated via the code histogram statistic, once α is larger than 1. Since the output transfer curve of the ADC fails to be monotonic, the code distribution under different value of α cannot be differentiated from each other. Observing the example from Fig. 6(b), the code histograms of $\alpha = 1.7$ and $\alpha = 1.3$ look similar, which contained periodic positive DNL of ≈1.2 LSB, while the expected compensation values of β are different in these two cases, as shown in Fig. 7(b).

In contrast, if $\alpha < 1$, the output characteristic is monotonic, and a corresponding gain factor β can be easily estimated via code histogram statistic. In Fig. 8, the smaller α leads to negative DNLs or missing codes. The nonlinearities are periodic and have a static interval of 2^{j-1}. The nonlinearities can be corrected in the digital domain through multiplying a gain factor β to j-bit outputs of the second stage

$$D_{\text{out,cal}}[B_{n+1}\dots B_1] = \text{fix}\left[\left(\sum_{n=1}^{i}2^{n+j-2}B_{n+j} + \beta\sum_{n=1}^{j}2^{n-1}B_n\right)\Big/\beta\right]. \tag{7}$$

The gain factor β can be derived as

$$\begin{aligned}\beta &= \frac{2^{j-1}}{2^{j-1} - [\text{His}_{\text{err}}(m) + \cdots + \text{His}_{\text{err}}(m + 2^{j-1})]}\\ \text{His}_{\text{Av}} &= [\text{His}(m) + \text{His}(m+1)\cdots + \text{His}(m + 2^{j-1})]/2^{j-1}\end{aligned} \tag{8}$$

where $\text{His}(m)$ is the code count of each output, His_{Av} is the average count of total m outputs D_{out}, and $\text{His}_{\text{err}}(m)$ is the output code containing negative DNLs, which is defined as

$$\begin{aligned}&\text{if}\quad \text{His}(m) \geqslant \text{His}_{\text{Av}}\\ &\qquad \text{His}_{\text{err}}(m) = 0\\ &\text{if } \text{His}(m) < \text{His}_{\text{Av}} \;\;\&\;\; \text{His}(m) \neq 0\\ &\qquad \text{His}_{\text{err}}(m) = \text{His}(m)/\text{His}_{\text{Av}}\\ &\qquad \text{if}\quad \text{His}(m) = 0\\ &\qquad\qquad \text{His}_{\text{err}}(m) = 1.\end{aligned} \tag{9}$$

The statistical range is 2^{j-1} codes and starts from the middle code $m = 2^{n-1}$, as for a sine wave input, the digital outputs

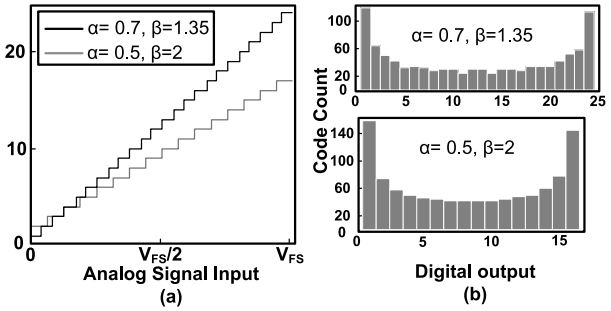

Fig. 9. (a) Calibrated transfer characteristic of 5-bit pipelined SAR with respect to $\alpha = 0.3$ and $\alpha = 0.7$. (b) Corresponding output code histogram of two cases with a sine wave input.

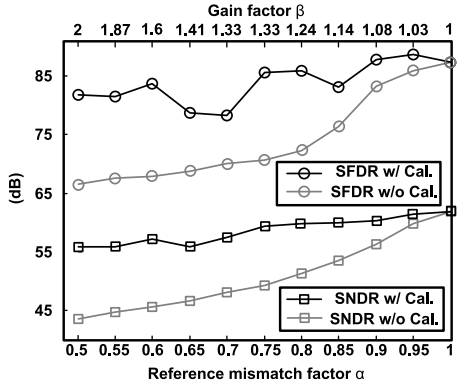

Fig. 10. Reference mismatch factor α versus the dynamic performance of a 5-bit pipelined-SAR ADC without and with HSGE calibration.

are more equally distributed in the middle than those at the two sides. In Fig. 8(b) with $\alpha = 0.7$, 2^{j-1} equals to 4; therefore, β is estimated from His (16) to His (19). As the His_{Av} is 21, His_{err} (17) and His_{err} (18) are 0.52. The gain factor β calculated according to (8) is 1.35. Similarly, with $\alpha = 0.5$, His_{err} (17) and His_{err} (18) are 1. β of 2 can be estimated according to (8) and (9). Fig. 9 shows the calibrated output characteristic. The proposed HSGE calibration involves no feedback to the analog circuitry that simplifies the circuit implementation.

To verify, the HSGE calibration behavioral simulations were performed, which modeled the conversion nonlinearities due to the reference mismatch in a 10-bit pipelined-SAR ADC. A two-stage structure was built with the 6- and 5-bit SAR ADCs with one bit overlapping for digital error correction. The values of the unit capacitors are Gaussian random variables with a standard deviation of σ ($\Delta C/C = 0.1\%$). Fig. 10 shows the dynamic performance of 100 times Monte Carlo results before and after calibration. The ratio α is set less than 1, and a corresponding gain factor β can be estimated by the calibration algorithm to compensate the nonlinearities. Both SNDR and spurious-free dynamic range (SFDR) are significantly improved after calibration. Fig. 11 shows the output spectrum before and after calibration with $\alpha = 0.85$. The reference mismatch gives rise to the odd harmonics and spurs that limits the SNDR and SFDR to 53.5 and 70.1 dB, respectively. After calibration, the spurs are removed and the odd harmonics are suppressed to lower than -81 dBFS, thus improving the SNDR and SFDR by 6.4 and 9.1 dB, respectively.

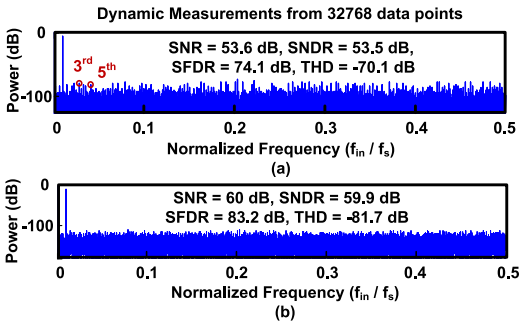

Fig. 11. FFT of the digital output ($\alpha = 0.85$). (a) Before calibration. (b) After calibration.

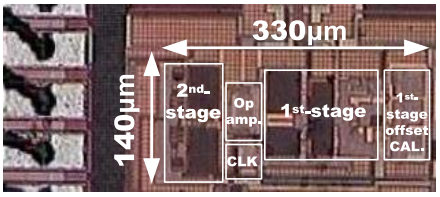

Fig. 12. Die chip photograph.

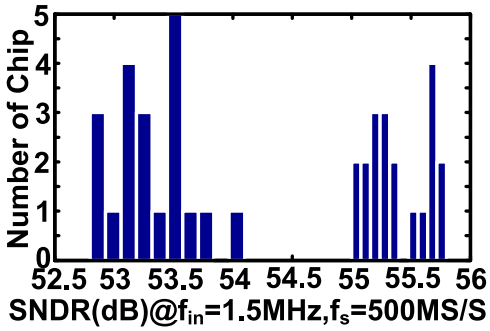

Fig. 13. Measured performances of a total of 20 chips without and with calibration.

Conventionally, the least mean square (LMS) method requires an accurate reference channel [20] and an adaptive filter updating at the background [21]. It has large hardware overhead and long time for convergence. Since the nonlinearity corrected here is mainly caused by the parasitics due to the use of the top-plate sampling rather than the finite Op-Amp gain error. It contains a periodic pattern in DNL that can be easily detected statistically. The proposed histogram method just collects the data within a code interval for gain estimation, which causes less hardware overhead. The digital gate count of the calibration algorithm is around 1 K and the estimated place and route area equal to 0.002 mm^2 with the power consumption of 800 μW at 500 MHz.

IV. Measurement Results

A 10-bit 500-MS/s PI pipelined-SAR ADC was fabricated in a 1P7M 65-nm CMOS process with low-VT option and metal–oxide–metal (MOM) capacitors. Fig. 12 shows the die photograph of the design; the active area is 0.046 mm^2 (330 $\mu\text{m} \times 140$ μm). The total power consumption is 8.2 mW at 1.2 V supply. The analog power consumption is 4.5 mW,

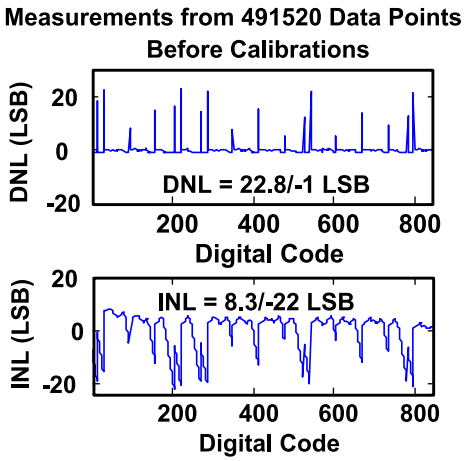

Fig. 14. Measured static performances without calibrations.

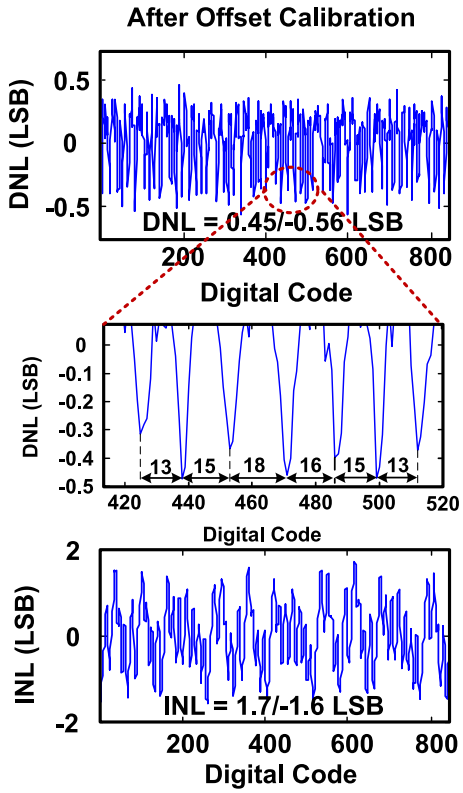

Fig. 15. Measured static performances with offset calibration.

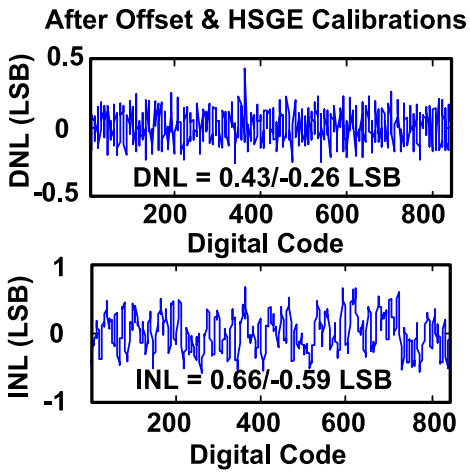

Fig. 16. Measured static performances with offset and HSGE calibrations.

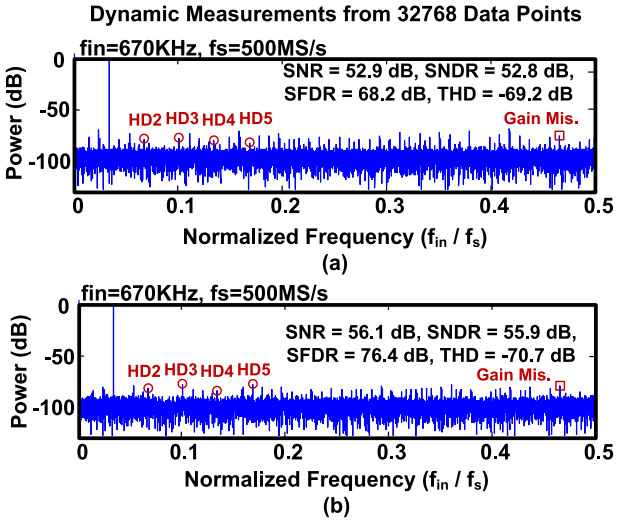

Fig. 17. Measured FFT of the digital output at dc input (decimated by 25). (a) With offset calibration and without HSGE calibration. (b) With offset and HSGE calibrations.

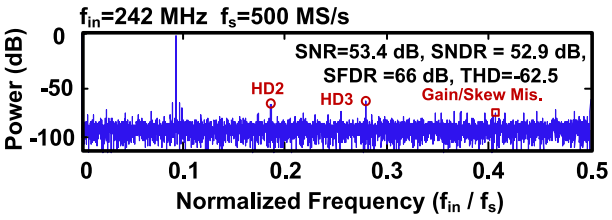

Fig. 18. Measured FFT of the digital output at Nyquist input (decimated by 25).

including T/H, DAC, comparators and Op-Amp, and the digital power consumption, including clock generator, SAR logic, and offset calibration, is 3.7 mW. The offset calibration is implemented on-chip, and the reference mismatch between the two stages is postprocessed according to the HSGE calibration algorithm. The calibration is controlled by MATLAB running on a PC, but the controller could be easily described in VHSIC hardware description language (VHDL). According to simulation results, excluding the nonidealities due to the mismatches from capacitors, reference, offset and gain, the thermal noise in the Op-Amp limits the SNDR to 56.5 dB. Fig. 13 shows the measured performance of the total available 20 chips at 1.2-MHz input and 500-MS/s sampling rate. The achieved average SNDRs before and after calibration are 53.6 and 55.4 dB, respectively, which matches the target specifications.

The measured static performances with and without offset and HSGE calibrations are shown in Figs. 14–16. Before offset calibration, the digital output contains large DNL and integral-nonlinearity (INL) >20 LSB, as the second-stage SAR operation is fully saturated by the offsets from the first stage and the Op-Amp. Once the offset calibration is active,

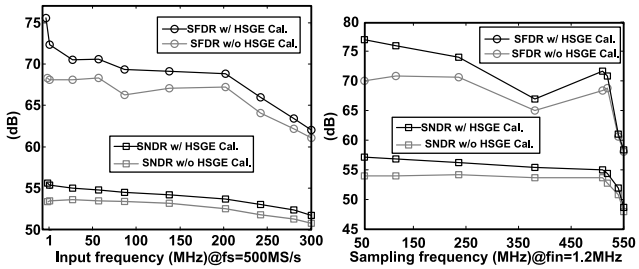

Fig. 19. Measured dynamic performance without and with HSGE calibration.

TABLE I
COMPARISON WITH STATE-OF-THE-ART ADCS

	[22] ISSCC' 13	[23] ISSC' 14	[24] VLSI' 13	This Work w/ Offs.& HSGE Cal.	This Work w/ Offs. Cal.
Architecture	TI-SAR	TI-SAR	Pipeline	Pipeline-SAR	Pipeline-SAR
Technology (nm)	45	65	65	65	65
Resolution (bit)	10	10	10	10	10
Sampling Rate (MS/s)	900	1000	800	500	500
Supply Voltage (V)	1.2	1.2	1.2	1.2	1.2
Input Swing ($V_{p\text{-}p}$)	N/A	N/A	N/A	1.2	1.2
SNDR(dB)	53.7	53	55	55.9	52.8
Power (mW)	10.8	18.9	19	8.2	8.2
FoM (fJ/conv.-step)	30	51.8	52	32	46
Area (mm^2)	0.038	0.78	0.18	0.046	0.046
Offset Calibration	N/A	Off-chip	Off-chip	On-chip	On-chip
Gain/Reference Calnibration	W/O	Off-chip	Off-chip	Off-chip	W/O

the /DNL/ and /INL/ are compensated within 0.6 and 1.7 LSB, respectively. Since the DAC in the first stage is segmented to unit element per 2 bit, the worst INL usually happening at the MSB transition is suppressed. According to the analysis in Section V, the reference mismatch causes linearity errors, which are expected to occur in an interval with approximating 16 codes. The error is clearly demonstrated in the DNL plot, where the negative DNLs happen periodically. The INL plot exhibits a systematic sawtooth pattern. The DNL and INL after the HSGE calibration are shown in Fig. 16 and the systematic errors in DNL and INL are both suppressed within 0.5 and 0.7 LSB, respectively.

Fig. 17 shows the measured fast Fourier transform (FFT) at 670-kHz input frequency, where Fig. 17(b) reports the peak SNDR after the offset and HSGE calibrations. The stage gain error causes a brunch of spurs spreading among the whole spectrum that degrades the SNR and the SFDR to 52.9 and 68.2 dB, respectively. Once the calibration is active, the spurs are suppressed. The third harmonic limits the SFDR to 76.4 dB. Therefore, the SNDR and the SFDR are both improved by 3.1 and 8.2 dB, respectively. The third and fifth harmonics are increased after calibration, which is potentially caused by the finite calibration accuracy, as the final digital code is rounded to 10 bit. Fig. 18 shows the measured FFT at near Nyquist input. The SNDR drops by 3 dB and the SFDR is dominated by the third harmonic. The spurs from offset, gain, and timing mismatches are all suppressed below -66 dB, which demonstrates the benefit of the proposed PI pipelined-SAR architecture and the effectiveness of the proposed calibration techniques. Fig. 19 shows the measured dynamic performances with and without HSGE calibration. The performance summary and comparison with state-of-the-art ADCs are shown in Table I. Comparing with some high-resolution and high-speed ADCs, this design achieves competitive conversion accuracy and speed with good power efficiency in 65-nm CMOS.

V. CONCLUSION

This paper presents the detailed circuit designs and considerations of a PI pipelined-SAR architecture. The conversion errors due to the mismatches from offset, gain, and reference are discussed and corresponding calibration techniques to correct these nonlinear errors are presented. The offset-cancellation technique is optimized to compensate offsets from both Op-Amp and comparators in the second stage, which increases the robustness of the design. The nonlinear behaviors of the reference mismatch between two stages have been analyzed, and a corresponding HSGE calibration has been proposed to improve both dynamic and static performance of the conversion. The proposed techniques are implemented in a 10-bit 500-MS/s PI pipelined-SAR ADC in 65-nm CMOS, which achieves an SNDR of 55.9 dB with 8.2-mW power dissipation and an FoM of 32 fJ/conversion step.

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