A 64 fJ/step 9-bit SAR ADC Array With Forward Error Correction and Mixed-Signal CDS for CMOS Image Sensors

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***Abstract*—A 9 b Successive-Approximation-Register (SAR) Anglog-to-Digital Converter (ADC) with pilot-Digital-to-Analog Converter (pDAC) technique for image sensor applications is described in this paper}. Its Forward Error Correction (FEC) improves its robustness against device mismatch. It performs mixed-signal Correlated-Double-Sampling (CDS) using only the ADC's built-in capacitor array without any additional amplifier or memory. The ADC measures $490\mu\mathrm{m} \times 7.4\mu\mathrm{m}$ and is demonstrated in a low-power CMOS image sensors with column parallel ADCs. Measurement results from the prototype image sensor in $0.18\mu\mathrm{m}$ technology shows that the ADC's Differential Non-Linearity (DNL) is reduced from 3.5 LSB to 1.2 LSB by its mixed-signal FEC algorithm, making its Figure-of-Merit (FoM) 64 fJ/step. Furthermore, when combined with the ADC's mixed-signal Correlated-Double-Sampling, the column FPN is reduced from 3.2% to 0.5% without any additional circuit.**

***Index Terms*—CMOS image sensor (CIS), column-parallel SAR ADC, correlated double sampling (CDS), error correction, single-ended ADC.**

I. Introduction

SUCCESSIVE APPROXIMATION REGISTER (SAR) Analog-to-Digital Converters (ADC) have received renewed interest in recent years because it is suitable for low-power applications with moderate sampling rate and resolution at aggressively scaled technology nodes. The steady increase in image sensor resolution, frame-rate, and mobility by technology scaling has made low-power data conversion circuit design an important topic. Column parallel SAR ADCs are becoming popular in state-of-the-art image sensors [1]–[4] for this very reason.

The main challenge of column parallel SAR ADCs for image sensors lies in achieving adequate resolution in a very small capacitor array due to constraints on the available circuit area. The typical mismatch for a 20 fF MIM capacitor (minimum design rule in $0.18\mu\mathrm{m}$ technology) is approximately 1% standard deviation [3], while this figure is close to 6% for MOM capacitors [5]. A bigger capacitor array results in better ADC accuracy, but the extra circuit area is prohibitively expensive in a column parallel CMOS image sensor. Furthermore, a smaller capacitor consumes much less switching power, and just as importantly, it also settles faster and thereby requires less power in the reference generator [6]. Earlier low-power switching techniques usually offer limited energy savings [7] at the expense of large and complex feedback control [8]. Schemes offering more aggressive energy and area savings such as the merged capacitor switching [9] and multi-step capacitor-splitting [10] are prone to charge-sharing parasitics during LSB quantization and require a large number of switches. The pilot-Digital-to-Analog-Converter (pDAC) ADC in [11] suffers from high Differential-Non-Linearity (DNL) and poor ADC Figure-of-Merit (FoM) due to its input dependent error correction range, analog Correlated-Double-Sampling (CDS), and conservative comparator design.

The pDAC described in this paper addresses the shortcomings of [7]–[10] and especially [11] by introducing input independent Forward-Error-Correction (FEC), mixed-signal CDS, parasitic effect reduction, and the ability to use energy efficient dynamic comparators. The resulting SAR ADC from these techniques is one of the smallest and most energy efficient designs with the best FoM among ADCs found in state-of-the-art image sensors. The prototype image sensor is described in Section II. The pDAC architecture is presented in Section III followed by the mixed-signal CDS scheme in Section IV. Fabrication issues such as device mismatch and parasitics are treated in Section V. Measurement results from the prototype chip are discussed in Section VI before final conclusions are made in Section VII.

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II. Image Sensor

A. Column Circuit

A CMOS image sensor featuring column parallel SAR ADCs is shown in Fig. 1(a). The pixel array is 920 × 256 pixels. Each column ADC in Fig. 1(b) is shared between 4 horizontal pixels. The 1.75 T pixel is chosen to obtain greater sensitivity through the amplifying action of the transfer-gate (TG) transistor. It also allows each of the 4 pixels to be multiplexed for readout. The FD nodal voltage is sampled onto the SAR DAC's top-plate twice via the source follower: once after FD reset and once after pixel charge transfer. Two quantizations are made with the option of performing mixed-signal Correlated Double Sampling (see Section IV) during the second quantization. Each pixel within

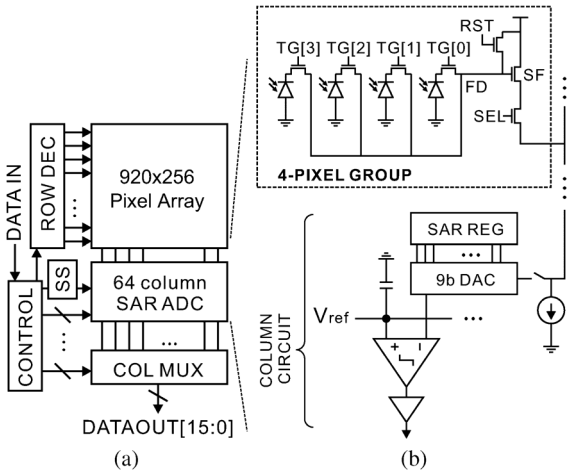

Fig. 1. The (a) image sensor and (b) its column circuit from pixel to source follower to SAR ADC.

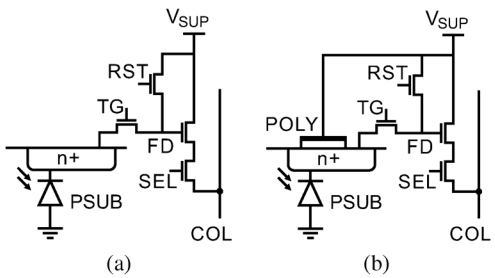

Fig. 2. A pixel with (a) a conventional photo-diode versus (b) photo-diode and capacitance boosting POLY layer.

the 4 pixel group is double quantized before the row decoder $(ROWDEC)$ increments to the next row. The row decoder has two multiplexers: one for pixel select and one for pixel reset. The exposure time can be controlled by setting the time difference between these two multiplexers. The output from each column is multiplexed onto the 16 b output data bus (16 columns at a time) before processing the next bit.

B. Pixel Structure

For very small pixels, the photo-diode (PD) capacitance alone (Fig. 2(a)) may not be large enough to ensure sufficient gain during its charge transfer to the FD node. As an experiment, gate POLY is added in Fig. 2(b) in an attempt to increase the PD capacitance. In practice, due to layout constraints, less than 25% of the PD surface area is covered by the POLY layer. The increased PD well-capacity can be used to trade for larger FD voltage swings by biasing the TG transistor at a lower voltage. The disadvantage of adding this POLY layer is that it will reduce the quantum efficiency and introduce fixed-pattern-noise (FPN) due to non-uniformity and surface defects.

III. Low-Power pDAC

A. Concept and Background

The core of the pDAC scheme is the idea of using only a small *pilot* portion of the total capacitor array, the pDAC, to determine the MSBs [11]. The rest of the capacitor array is disconnected during this phase. Using a decimated array to calculate these MSBs mitigates the dominant DAC power consumption associated with the MSB capacitors which has the largest load and signal magnitude. An implementation of a 9 bit ($N = 9$, $k = 6$, $p = 4$) pDAC SAR ADC is shown in Fig. 3. The unit capacitor, C, is a $5\mu\text{m} \times 5\mu\text{m}$ (minimum design rule) MIM capacitor with a typical capacitance of 28 fF.

For a N bit split capacitor array consisted of a k bit MSB array and a $N-k$ bit LSB array joined together by a bridging capacitor, C_B, its ith capacitor (illustrated in Fig. 3(a)) conforms to:

$$C_{MSB} = \sum_{i=N-k+1}^{N} C_i \tag{1}$$

$$C_{LSB} = \sum_{i=0}^{N-k} C_i \tag{2}$$

$$C_B = \frac{2^{N-k}}{2^{N-k}-1} C \tag{3}$$

The pDAC splits the first p MSBs of the k bit MSB array into a small group of sub-capacitors, C_{i0}:

$$p = k - 2 \tag{4}$$

$$C_i = \sum_j C_{ij} \tag{5}$$

$$C_{i0} = \frac{1}{3} C_{i1} \tag{6}$$

$$C_{pDAC} = \sum_{i=N-p+1}^{N} C_{i0} \tag{7}$$

The pDAC capacitors, C_{i0}, are chosen to be $(1/4)$ of the conventional size (with the exception of C_{N0}) because it yields a reasonable trade-off between circuit complexity and power savings. Splitting these capacitors into smaller sizes will increase the device mismatch error between C_{i0} and C_{i1} which would require a larger error correction margin to accommodate. Presently, an additional bit decision is inserted between the pDAC phase and LSB phase to introduce redundancy into the system. The correct quantization result can be recovered by an error correction algorithm performed after data read-out.

The earlier pDAC scheme described by [11] had an input-dependent error correction range. It worked because this range is large at input points where dominant mismatch error between C_{i0} and C_{i1} occurs, but its accuracy is always worse than the conventional SAR scheme at input regions of small error correction range.

The pDAC described here has an input-independent FEC scheme achieved by introducing a different configuration for the C_N ($N = 9$ for a 9 b ADC) capacitor. Although the C_{N0} weight is still $1/3$ of C_{N1}, they are scaled to be smaller than $\sum_j C_{Nj}$ to make room for the error correction capacitor C_{N2} (C_{92} in Fig. 3). The C_{N2} weight is only used during the FEC phase, so its operation is input-independent. Consequently, the error correction range is made uniform throughout the input range. The simulated and measured results both show that this uniform error correction range helps to improve the ADC's Differential Non-Linearity (DNL) under large device mismatch. The magnitude of this error correction range will be analyzed in Section III-B-2. In addition to FEC, the non-binary weighting of C_{N0} means it is smaller than the sum of its LSB pDAC weights (C_{i0}) which further protects the ADC against non-linearities caused by any mismatch in C_{N0} and C_{N1} [12].

B. Circuit Operation

The basic pDAC operation is illustrated in Fig. 3. In the sampling phase (Fig. 3(a)), the input signal is sampled onto the top-plate of the capacitor array. The capacitive load seen by the signal source and reference generator is approximately $64C$.

1) MSB Phase: The pDAC sub-array, C_{pDAC}, is used to determine the four MSB bits $(L_{[9:6]})$ as shown in Fig. 3(b). The pDAC array is one quarter of the size of the MSB array with the exception of C_{92}. Once the 4 MSBs are determined, the rest of the MSB and LSB capacitors are connected on the fifth clock without any trial-and-error. This approach reduces the DAC's power consumption. The driving requirement of the reference generator is also relaxed for the same sampling speed. The C_3 capacitor is asserted during the MSB phase to create an artificial offset. This allows the error correction to be bipolar while the DAC itself remains unipolar and is analogous to dithering [13]. However, unlike conventional dithering which is randomly injected by a secondary bipolar DAC [14] and may need to be filtered over a long sequence [3], the FEC offset in pDAC is deterministic and integrated into the unipolar SAR DAC. It virtually incurs no circuit area overhead. The DAC output, V_{DAC}, during $N \geq i \geq N-p+1$, is:

$$V_{DAC_i} = V_{ref}\left(\frac{C_{i0}+\sum_{j=i+1}^{N} C_{j0}L_j+(C_{N-k}\|C_B)}{C_{pDAC}+C_{N-k}\|C_B+C_{par}}\right)+V_{sig} \tag{8}$$

The parasitic capacitance C_{par} is estimated by post-layout extraction. It is dominated by bottom-plate parasitics. Layout techniques on how to mitigate the effect of C_{par} will be covered in Section V-B. Ideally,

$$C_{par} + C_{N-k}\|C_B \approx 2C \tag{9}$$

Otherwise, additional error against the scaling relationship of (6) will be introduced by the mismatch of C_{i0} weights which will lead to reduced FEC margin. When (9) holds, it also ensures

$$C_{N0} < \frac{1}{2}\left(C_{pDAC} + C_{N-k}\|C_B + C_{par}\right) \tag{10}$$

which provides additional redundancy to protect against errors in the MSB code transition.

2) FEC Phase: If the pDAC is not exactly one quarter of the nominal MSB capacitor array, a bit error made during pDAC switching will be much larger than 1 LSB, and missing codes will occur because V_{DAC} can never converge to V_{ref} in subsequent bit-trials. This scenario is probable because the smaller pDAC will have worse device mismatch than the full-sized capacitor array. This problem is addressed by introducing a redundant bit-trial in Fig. 3(c).

During the error correction clock, C_{N-k} is restored to GND, this creates a negative perturbation on V_{DAC}. Both positive and negative errors from earlier bit-trials can be recovered by the C_{N2} weight (C_{92} in this case) under the accuracy of the full-sized capacitor array. For $i = N-p$:

$$V_{DAC_i} = V_{ref}\left(\frac{C_{N2}+\sum_{j=i+1}^{N}(C_{j0}+C_{j1})L_j}{C_{MSB}+C_B\|C_{LSB}}\right)+V_{sig} \tag{11}$$

Since the switching of C_{N2} is input-independent, the error correction range is uniform throughout the input range, and it is approximately ± 16 LSBs in this implementation.

3) LSB Phase: The 5 LSBs in the SAR ADC are obtained using the conventional switching sequence (Fig. 3(d)). Since the entire array is connected at this point, the final conversion result will enjoy the same precision and accuracy as the conventional switching scheme. The final SAR ADC output is decoded by:

$$D_{SAR} = \left((2^{p-1}-1)L_N + \sum_{i=N-p+1}^{N-1} 2^{i+p-N-1}L_i + L_C\right)\times 2^{N-p} + \sum_{i=1}^{N-p} 2^{i-1}L_i \tag{12}$$

IV. Mixed-Signal CDS

A. Comparator

The SAR ADC's comparator circuit shown in Fig. 4 is based on the design reported in [15]. But since there is no requirement on small input offset error here, the calibration DAC and its registers in [15] are removed to save circuit area making it approximately 80% smaller than [15]. Compared to the design in [16], an additional PMOS transistor is added here to reset the source of M1 and M2 during the reset phase to remove input-dependent hysteresis. The comparator inputs to the gates of $M1$ and $M2$ each have a gate capacitance (C_g) of 0.85 fF (post-layout extraction). This input capacitance is small because $M1$ and $M2$ are minimally sized at $0.46\mu\text{m}/0.19\mu\text{m}$ (width/length) and $0.46\mu\text{m}/0.18\mu\text{m}$ respectively while the entire comparator measures $41\mu\text{m}\times 5\mu\text{m}$. This small capacitance makes the kick-back noise negligible. This class of dynamic amplifiers is energy efficient, but they are not normally suitable for ADC array applications without additional compensation circuits to remove their large input offset errors. A mixed-signal CDS technique is introduced in the next section to address this problem.

B. Pre-loaded DAC Offset Cancellation

Correlated-Double Sampling (CDS) is a useful technique for suppressing low frequency noise components and fixed pattern offset errors, but it also incurs additional resource overhead. In digital CDS, the memory size and its power consumption is doubled in order to store two ADC results. In analog CDS, a large capacitor is needed to store the analog value and the CDS operation may be much slower than the ADC itself [1] unless additional power consumption is allocated to speed up the CDS amplifier.

In this section, a method for performing mixed-signal CDS using the SAR ADC's capacitor array is introduced. It can mitigate the comparator offset error without additional auto-zeroing capacitors or digital adders. The idea is similar to the concept sketched in [17] and is discussed here with additional analytical detail. The basic schematic is shown in Fig. 5.

The input, V_{in}, is sampled on to the top-plate of the capacitor array. During this sampling phase, instead of holding the bottom-plates of the DAC capacitors at ground as it is in the usual case, they are held at a digital value D_R. After the first sampling phase, the bottom-plates are restored to ground and charge-redistribution will settle the capacitor voltage to

$$V_C(1) = V_{RST} - Q^{-1}(D_R) \tag{13}$$

where $V_C(1)$ is the DAC output, Q^{-1} is the DAC function (it converts a digital word into its equivalent DAC output voltage), and V_{RST} is the pixel output voltage after the pixel floating

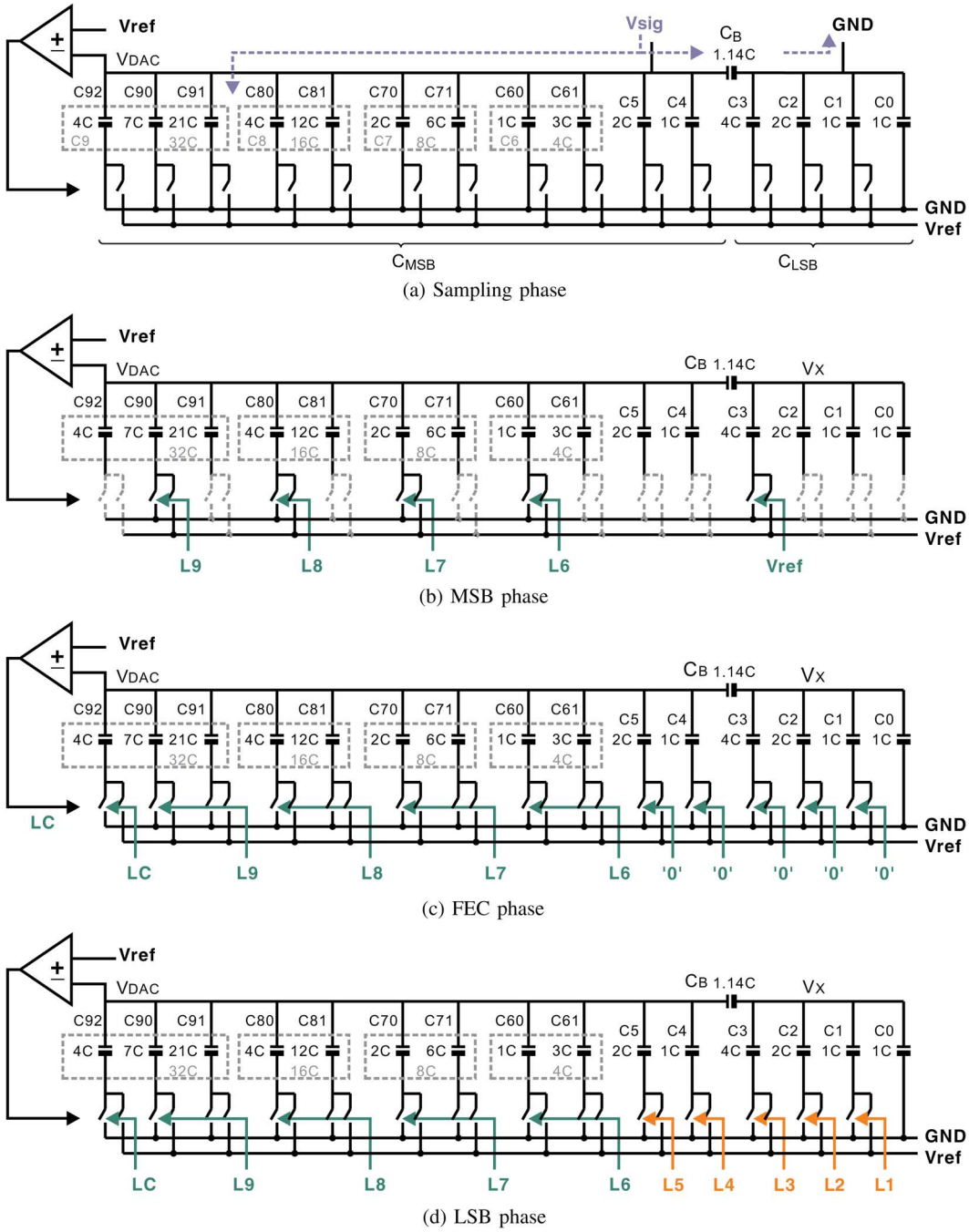

Fig. 3. (a) Sampling Phase. (b) Resolve the first 4 MSBs by pDAC switching. (c) Error correction with the 4 C sub-capacitor. (d) Resolve the rest of the LSBs by conventional DAC switching.

drain (FD) node is reset. When the SAR ADC quantization is finished, the digital value stored in the SAR register is:

$$D(1) = Q(V_{ref} + V_e - V_C(1)) \tag{14}$$
$$= Q\left(V_{ref} + V_e - V_{RST} + Q^{-1}(D_R)\right) \tag{15}$$

where Q is the quantization function, V_e is the comparator offset, and V_{ref} is the SAR ADC reference voltage. Taking the complement of $D(1)$ and expanding $V_C(1)$ yields:

$$\overline{D(1)} = Q(V_{ref}) - Q\left(V_{ref} + V_e - V_{RST} + Q^{-1}(D_R)\right) - 1 \tag{16}$$

If the bottom-plates of the DAC capacitors are held at $\overline{D(1)}$ during the second sampling phase and restored to ground after sampling, the voltage across the capacitor array will settle to

$$V_C(2) = V_{pixel} - Q^{-1}\left(\overline{D(1)}\right) - V_Q \tag{17}$$
$$= V_{pixel} - V_{ref} + V_{ref} + V_e - V_{RST} + Q^{-1}(D_R) - Q^{-1}(1) - V_Q \tag{18}$$
$$= V_{pixel} + V_e - V_{RST} + Q^{-1}(D_R) - Q^{-1}(1) - V_Q \tag{19}$$

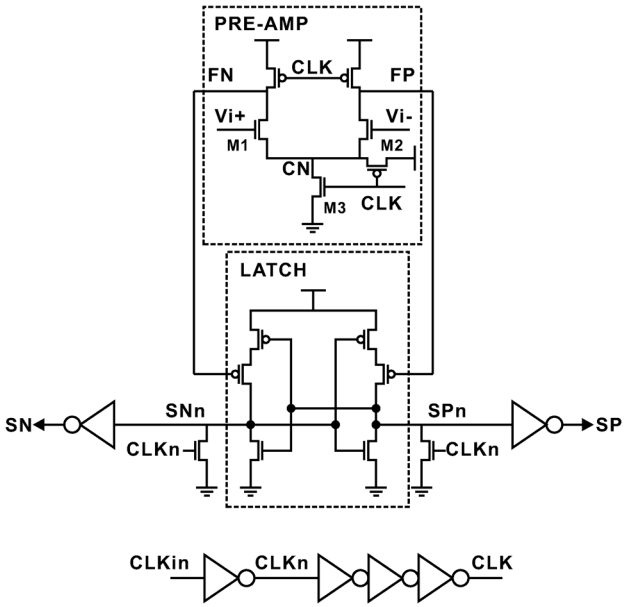

Fig. 4. Schematic of the SAR comparator.

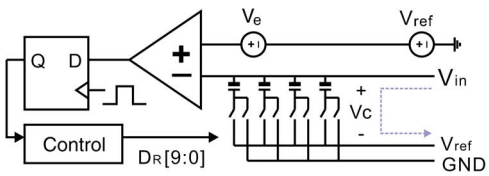

Fig. 5. A mixed-signal CDS scheme using pre-loaded SAR DAC.

where V_{pixel} is the FD voltage after pixel charge transfer and V_Q is the error term that includes both quantization error and reset noise. The quantization of $V_C(2)$ approximates to

$$D(2) = Q\left(V_{ref} + V_e - V_C(2)\right) \tag{20}$$

$$= Q\left(V_{ref} + V_e - V_{pixel} - V_e + V_{RST} - Q^{-1}(D_R) + Q^{-1}(1) + V_Q\right) \tag{21}$$

$$\approx Q\left(V_{ref} - V_{pixel} + V_{RST} - Q^{-1}(D_R) + Q^{-1}(1) + V_Q\right) \tag{22}$$

$$\approx Q\left(V_{ref} - \left(V_{pixel} - V_{RST} + Q^{-1}(D_R)\right) + V_Q\right) + 1 \tag{23}$$

$$\approx Q\left(V_{ref} - (Q^{-1}(D_R) - (V_{RST} - V_{pixel})) + V_Q\right) + 1 \tag{24}$$

and the offset error, V_e, is cancelled. In the case of pDAC, the above equations are still valid if the error correction bit L_C is inverted independently as an additional bit entry to $\overline{D(1)}$. In this case, Q^{-1} and Q functions reflect (12). When the DAC settles after sampling, and before it enters pDAC mode, the compensation voltage created by $\overline{D(1)}$ during sampling is applied to all capacitors. So V_e does not change with respect to the pDAC mode and is negated during subsequent quantization. Like digital CDS, the accuracy of this mixed-signal CDS is limited by its quantization error and reset noise (V_Q). Although analog CDS can achieve high accuracy, the resulting increase in power consumption and circuit area is prohibitively expense. The main advantage of this mixed-signal CDS is that it does not require additional storage memory or adder.

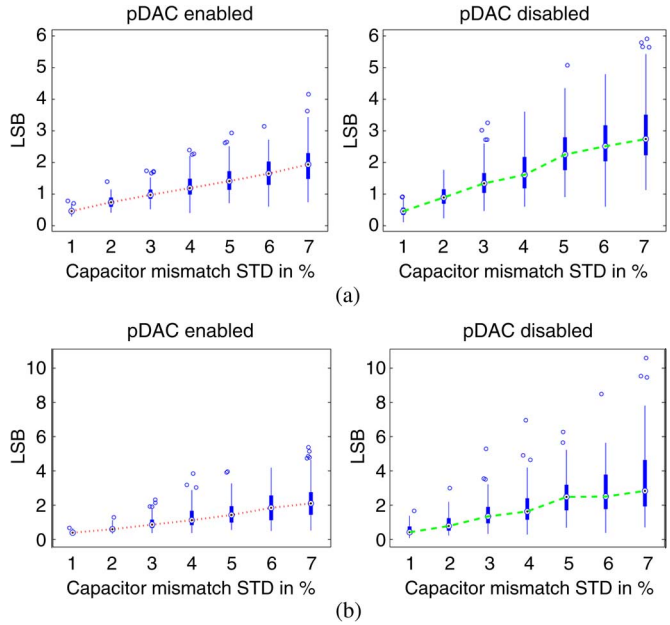

Fig. 6. Maximum (a) INL and (b) DNL for different capacitor mismatch standard deviations at 9 b ADC resolution. Line plots trace the Monte Carlo distribution mean.

V. Fabrication Issues

A. Device Mismatch

The effect of capacitor mismatch on the reported pDAC architecture is verified with 100 instances of Monte Carlo simulation. The percentage of capacitor mismatch is defined to be a Gaussian distribution with a standard deviation (STD) normalized to the unit capacitor. The parasitic capacitor, C_{par}, is assumed to be 2 unit-capacitors (with mismatch) in these simulations. The absolute capacitor mismatch error is randomly generated for each Monte Carlo instance according to these statistics, and the ADC input is linearly swept by circuit simulation to extract the DNL and INL values for each given instance. The maximum DNL and INL from each given Monte Carlo instance is collated for a given value of STD. Fig. 6 plots the distribution of these maximum DNL and INL values under increasing STD. The values of STD is chosen to cover the typical range reported in [3] and [5].

For small mismatches, the conventional switching method leads to smaller non-linearities because it can enjoy the advantage of higher precision in its MSB weights. At increased capacitor mismatch, large non-linearity errors begin to emerge due to wrong bit decisions made by poorly matched MSB weights. The pDAC scheme has an advantage under these circumstances because the combined redundancy of its FEC and non-binary MSB can compensate for linearity errors caused by the MSB weights.

B. Parasitic Effects

Each SAR ADC column layout measures $490\mu\text{m} \times 7.4\mu\text{m}$. Its size is dominated by a large DAC capacitor array. Considerable savings are made by overlapping the MIM capacitors on the active circuit. This, however, poses some challenges because the bottom-plate of some of these capacitors (C_{i1} and all non-pDAC capacitors) are left floating during pDAC operation. Any parasitic capacitance, C_{par}, on these bottom-plates will lead to errors in the MSB weights (8). The strategy adopted here is to

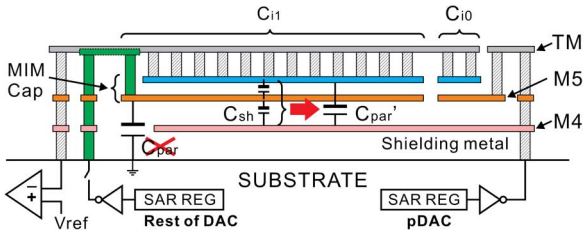

Fig. 7. Using M4 to shield the floating capacitor during pDAC operation.

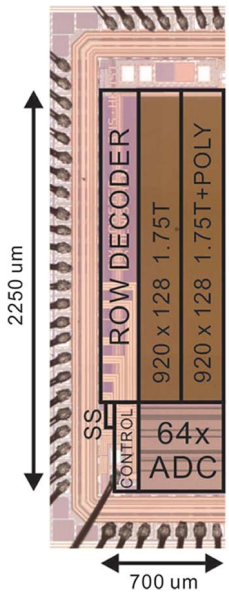

Fig. 8. Prototype HIGHSTED, CMOS image sensor with pDAC SAR ADC array and mixed-signal CDS.

use the fourth metal layer $(M4)$ as a shield between the MIM capacitor ($M5$ and $M6$) and the active circuits ($M3$ and below). This concept is illustrated in Fig. 7.

The $M4$ shielding layer is segmented and driven by the bit decisions from the pDAC section. Essentially they form an enlarged pDAC and they are always held at a well defined voltage throughout the quantization phase. Because the size of each shielding segments (C_{sh}) is designed to correlate with the capacitor weights (C_{i0}) to which they are connected to as shown in Fig. 7, the DAC voltage produced by their parasitic capacitance, C'_{par}, also correlates to C_{i0}:

$$C'_{par} = C_{i1} \| C_{sh} \approx C_{sh} \propto C_{i0} \tag{25}$$

This scaling effect mitigates the error introduced by C_{par} and allows for a very compact column circuit. Without shielding, C_{par} can introduce additional DNL errors in the excess of 10 LSBs in post-layout simulation.

VI. Measurement Results

A. Prototype Chip

The prototype image sensor in Fig. 8 is fabricated in Global Foundry 1P6M 0.18μm mixed-signal technology. Its ADC performance is summarized in Table I and its imaging performance is summarized in Table II. The pixel array, ADC, reference circuit, and digital logic are powered by 1.8 V supplies while the IO pads and transfer-gate switches (for ADC sampling) are powered by the 3.3 V supply. The choice of 3.3 V transfer-gate switches for ADC sampling instead of bootstrapped switches helps to reduce the circuit area.

TABLE I
Summary of a Single ADC

	with pDAC	without pDAC
Process	0.18 μm 1P6M CMOS	
Supply voltage	3.3 V, 1.8 V	
Area	7.4 × 490 μm^2	
Clock frequency	2.06 MHz	2 MHz
Pixel resolution	920 × 256	
Frame rate	9 fps	
Read noise	5300 μV_{rms} (1.5 LSB)	
Sample rate	66.67 kSa/s	
DNL	1.2 LSB	3.5 LSB
INL	4 LSB	4 LSB
column FPN (CDS)	0.5%	3.2%
ER	8.20 bit	6.97 bit
ADC power	1.25 μW	1.27 μW
Energy consumption	18.7 pJ/Sa	19.0 pJ/Sa
FoM (ADC only)	64 fJ/step	152 fJ/step

TABLE II
Summary of Pixel Performance

	without POLY	with POLY
Pixel size	1.85 μm × 1.85 μm	
Fill factor	20 %	
Well capacity (e^-)	2935	4994
Conversion gain ($\mu V/e^-$)	55	70
Dark current (e^-/sec)	< 707	<1805
Dynamic range (dB)	80	73
Sensitivity (V/Lux.sec)	0.023	0.026
Pixel noise (μV_{rms})	11900	15100

The Figure-of-Merit (FoM) is calculated for a single ADC (without CDS) based on its effective resolution, ER, defined as

$$ER = log_2\left(\frac{2^b}{\epsilon}\right) \tag{26}$$

where 2^b is the measured ADC input range, and ϵ is the maximum between worst-case DNL and input-referred rms noise. This definition is appropriate for image sensors since the output from the pixel array can be considered to be a DC signal [18]–[22] as opposed to a full-range sinusoid. The comparator in the reported ADC has been designed with a built-in 200 mV input offset (subject to 60 mV standard deviation observed in Monte Carlo simulations) to safeguard against DAC saturation during mixed-signal CDS. Measurements from 4 ADC channels indicate an average offset value of 192 mV with a standard deviation of 51 mV. Consequently the ADC reported in Table I has a measured code range of $2^b = 440$ (offset is 250 mV) instead of 511. This discrepancy is taken into account in the reported ER. The ADC Figure-of-Merit (FoM) is calculated from ER:

$$FoM = \frac{P}{F_s \times 2^{ER}} \tag{27}$$

where P is the circuit power consumption, and F_s is the sampling frequency.

TABLE III
COMPARISON OF ADCS FOR IMAGE SENSORS. THE REPORTED SAR ADC IS ONE OF THE SMALLEST AND MOST ENERGY EFFICIENT ADCS WITH THE BEST FOM FOUND AMONG IMAGE SENSORS DESPITE OF IT USING AN OLDER 0.18μm TECHNOLOGY

Year	2009	2009	2011	2011	2009	2012	2012	2012
Ref	[23]	[24]	[18]	[19]	[2]	[1]	[5]	This work
ADC architecture	2-step SS	Cyclic	$\Delta\Sigma$	Cyclic	SAR	SAR	SAR	SAR
Technology (μm)	0.35	0.18	0.13	0.13	0.18	0.13	0.18	0.18
Supply (V)	2.8	1.8, 3.3	2.8, 1.2	2.8, 1.5	3.3, 1.8	2.8, 1.5	-	1.8, 3.3
Column area (μm^2)	11.2×484	5.6×1112	**4.5×600**	18×240	8.4×1320	9×425	15×700	**7.4 × 490**
Normalized column area	1.9	2.2	**1.0**	1.6	4.0	1.4	3.8	**1.0**
Resolution	320×240	640×428	1692×1212	1696×1212	4112×2168	1600×1200	256×256	920 × 256
Pixel pitch (μm)	5.6	5.6	2.25	2.25	4.2	2.25	15	**1.85**
Sensitivity (V/lux.s)	0.52	7.1	-	0.11	-	1.6	68.5	0.026
Conv. gain ($\mu V/e^-$)	46	61	80	80	45	-	-	52
Well capacity (e^-)	18500	-	11000	11000	27800	-	-	4994
Read Noise (μV_{rms})	490	336	152	1000	17.6	2400	3202	5300
Dynamic Range (dB)	64.8	71	75	59	84	52	56.5	73
Clock (MHz)	25	-	48	25	41.25	7	25	2.06
ADC sample rate (kSa/s)	168	166	145	1210	108	180	384	33.3
Frame rate (fps)	700	390	120	250	50	150	1500	9
CDS	Analog	Digital	Digital	Analog	Digital	Analog	Analog	Mixed
ADC resolution (b)	11	13	12	10	14	10	10	9
DNL(LSB)	+0.53/-0.78	0.5	+0.55/-0.63	+0.59/-0.83	1	-	0.34	1.2
INL(LSB)	+1.42/-1.61	3.2	+3.7/-0.8	+2.8/-3.6	+2/-15	-	0.6	4
column FPN	0.10%	0.06 LSB	0.01%	0.10%	0.38e^-	0.4 LSB	0.52%	0.5%
Energy (pJ/pixel)	670	2780	731	584	2434	764	3967	**53**
FoM (fJ/step)	327	339	179	570	149	746	3874	**140**

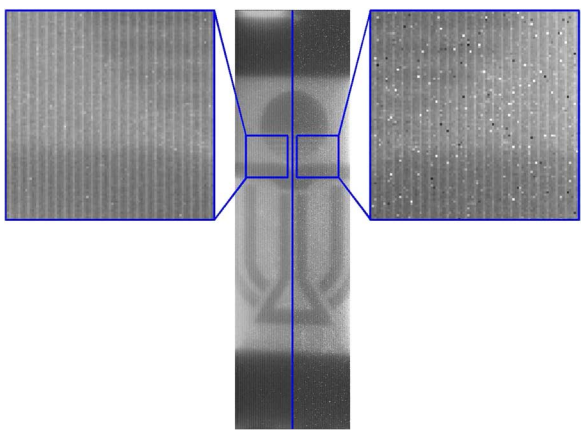

Fig. 9. Image captured from prototype chip. Left half of the array consists of pixels without POLY layer while right half of the array consists of pixels with POLY layer.

The prototype image sensor has a 920 × 256 pixel array. All power consumption figures are measured at this resolution. Fig. 9 shows the test image from the two 920 × 128 pixel blocks each using one of the two structures described in Fig. 2 from Section II-B. It is evident from the results in Table II and Fig. 9 that while adding the POLY layer increased the well capacity and photo-sensitivity, leading to improved image contrast, it also introduced significant pixel FPN due to surface detects and non-uniformity. The vertical stripes in Fig. 9 is a result of first order gain FPN caused by parasitic capacitors in the 1.75 T pixel layout. The column FPN in Table I is measured by connecting the input of the ADC array to a common signal.

The performance of the prototype image sensor is compared against other published works in Table III. The prototype's FoM in Table III includes contributions from mixed-signal CDS (two ADC samples), pixel source-follower, and additional shutter-related digital control. For other entries in Table III, because image sensors typically do not quote their standalone ADC noise, their FoMs are calculated with ER substituted by their nominal resolution which assumes zero noise and non-linearity. Despite this, the reported prototype chip has the lowest FoM and energy consumption per pixel quantization. Its higher non-linearity error when compared to other entries in Table III is a consequence of fabrication vendor, process scaling, and choice of unity capacitor size.

B. Non-linearity and FPN

The SAR ADC measurements are characterized by sweeping the input of the ADC with a signal generator and comparing the SAR ADC's output to the data captured from an Agilent MSO7034A oscilloscope's internal 12 bit ADC. The DNL and INL measurements are given in Fig. 10(a) and Fig. 10(b), respectively. The large DNL error due to missing codes at 125th and 350th code entry in the conventional DAC is resolved by the reported FEC algorithm. The INL, on the other hand, is limited by the accuracy of the full capacitor-array. It can only be reduced by using a bigger capacitor-array or calibration. Compared to the other SAR entries in Table III, the DNL and INL of this work reflects a trade-off resulting from using a smaller capacitor array.

The input referred offset error across the entire ADC array (160 ADCs) is measured by applying the same input signal to all ADCs. Its standard deviation is recorded in Table IV. Without CDS, this error is large due to the mismatch of the comparator's input transistors. These transistors can not be sized to be too big,

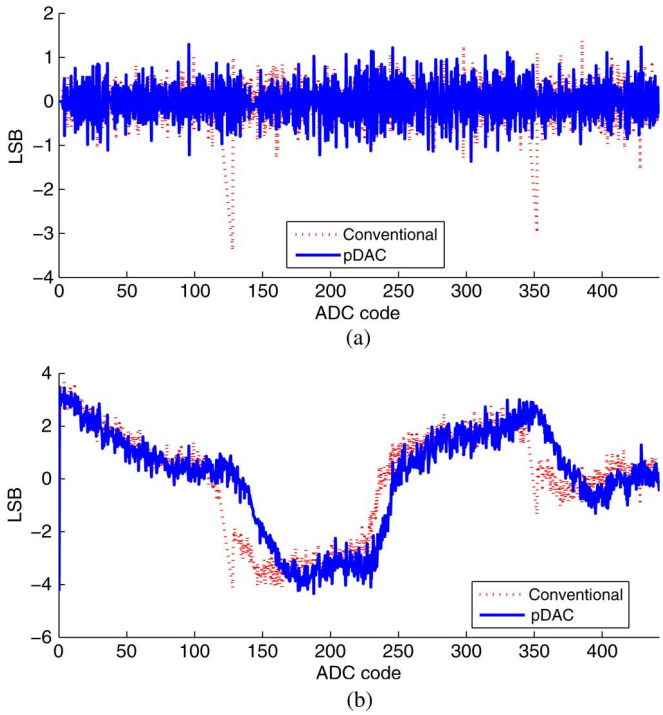

Fig. 10. (a) DNL and (b) INL(normalized to the LSB) of the 9 b SAR ADC.

TABLE IV
RMS OFFSET ERROR (LSB) ACROSS 160 ADCS

	with CDS	without CDS
with pDAC	2.6	10.5
without pDAC	16.5	10.3

otherwise their load will introduce non-linearity and attenuation to the DAC output. When mixed-signal CDS is applied, the FPN can only be reduced if the DAC is accurate. Without pDAC, the post-CDS offset error is limited by the large DNL due to missing codes. When the CDS is combined with pDAC's FEC, the offset error is dramatically reduced. Its accuracy becomes limited by the INL error and is consistent with Fig. 10(b).

C. Power Consumption

Fig. 11 shows the total simulated energy consumption per sample of the SAR ADC (DAC and comparator) for increasing ADC resolutions. The MSB array size is doubled for every additional bit, while the LSB array is unchanged (k is fixed at $k = N - 3$). The comparator's energy consumption per bit is fixed according to the measured results and it scales linearly with N. The assumption here is that, for higher resolutions, lower comparator speed can trade for higher SNR while keeping the energy per comparison the same [25]. Presently, for the $N = 9$ case, the pDAC scheme only led to a measured 1.21% saving (2.9% in simulation) because the capacitor array is very aggressively sized ($N = 9$ and $k = 6$). The dynamic comparator alone makes up for more than 60% of the total energy consumption. For larger capacitor arrays ($N = 12$, $k = 9$), the comparator is estimated to only make up for 38% of the ADC energy consumption, while the pDAC can reduce the average DAC energy consumption by 60% yielding as much as 38% reduction in total energy consumption. This is a significant improvement over the

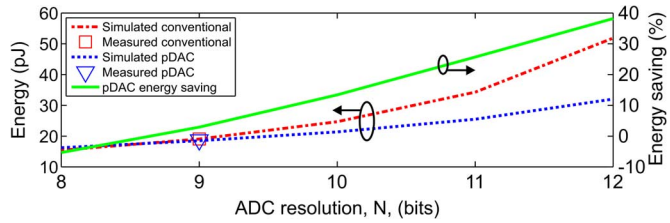

Fig. 11. Simulated and measured ADC energy consumptions over a range of resolutions.

low-power switching technique in [7] where 37% DAC energy saving is achieved for a 10 b conventional binary weighted capacitor array (equivalent to $k = 10$).

VII. CONCLUSION

A CMOS image sensor with compact low-power SAR ADC array is presented. The degradation in the ADC resolution due to the aggressively sized capacitors is mitigated by the reported pDAC scheme with error correction and parasitic effect reduction. The large input offset error in the energy efficient dynamic comparator is reduced to the level of ADC quantization noise by the reported mixed-signal CDS scheme without any additional digital circuit. The resulting SAR ADC, with its best-in-class FoM, is one of the smallest and most energy efficient ADCs among image sensors. These techniques are well suited for applications where the size of the SAR ADC array and its column FPN must be small.

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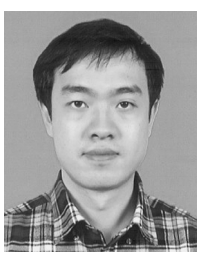

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