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Design and analysis of energy recyclable bidirectional converter with digital controller for multichannel microstimulators

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Abstract The power supply modulated microstimulator system can drive an expandable electrode array with reduced heat generation across the current drivers and high stimulation efficiency. Here, we present a comprehensive analytical modelling of the system to investigate internal and external energy flow during biphasic stimulation pulses spanning over varying loading configurations (e.g. number of electrodes, and stimulation current amplitude) that were not covered by existing works on the power supply modulated microstimulators. This paper fills the research gap by presenting the systematic tools for attaining insights of a stimulator system featuring a bidirectional DC–DC converter with an algorithmic digital controller. The models employed here are based on traditional analytical methods such as transfer functions and state-space dynamic models incorporating various circuit elements incurring power loss. With the models, the behaviour and power efficiency under a wide range of parameters associated with stimulator are attained. Numerical assessment reveals that the digital controller can track the output supply voltage at the phase transition boundaries just in tens of switching cycles. The system was also studied on a verification platform, where the internal signals of the digital controller were carefully examined. Measurement results show that the system behavior well matched to the simulation results, demonstrating the effectiveness of the analytical system model for obtaining key insights for generic large-scale micro-stimulator designs.

Keywords Electrical stimulator · Power supply modulation · Energy recycling DC–DC converter

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1 Introduction

In biological nervous system, neurotransmitter induces potential depolarization through the well-known chain reaction controlled by the molecular mechanics of the Na/K/Ca cation gated channels which modulate the cellular gradient of the molecular density. All those neurons can be innervated by artificially modulating displacement current at a location near the nerve under stimulation. Thus the primary function of a stimulator is to steer charge into and out of the nerve over a wide range of operating conditions with high precision. To achieve this goal, a stimulator should be capable of driving a variable current corresponding to the excitatory threshold charge of the nerve (typically over 100 nC [1]) through stochastically varying tissue-electrode impedance. Driving the actual neuronal network requires a high-density electrode array that is accessed from a multichannel microstimulator.

There are several design challenges related to multichannel microstimulator. First, the power supply has to be adaptively adjusted according to the electrode voltage compliances to reduce the heat generation of the current

drivers and to improve the stimulation efficiency. The maximum allowable temperature rise in implant devices should be regulated under 4.5°C [2]. According to a study performed in cadaver eyes with apically implanted heating elements [3], temperature increases at the center of the implanted sites are linearly proportional to the dissipated power at the sites, with 1°C per 67.8 mW, translating into a power budget of about 300 mW to stay under the safety ceiling. The microstimulators where the current drivers are connected to a fixed supply can lose a lot of energy across the current controlling transistors as heat. Second, the power supply is required to continuously respond to the dynamic state evolution under various loading configurations (e.g. number of electrodes and stimulation current amplitudes) with continuous output voltage levels. Third, to exploit the energy instantaneously stored on electrodes during the anodic stimulation phase, the energy recycling technique should be implemented for the charge accumulated on the double-layer capacitors of the electrodes to be reclaimed back to the energy source. Fourth, it shall be able to be compatible with energy reservoir that stores energy from various power generators, such as thermoelectric, piezoelectric, and photoelectric energy harvesters. Fifth, multichannel scalability should be carefully considered to accommodate a flexibly expandable electrode array. Lastly, the supply modulating controller should be coherently incorporated with the stimulation pattern management logic block to ensure the interoperation of the power supply generator and stimulating current drivers for handling the time-varying configuration of the electrode array.

A number of microstimulators employing power supply modulators to reduce the energy loss across the current driver can be considered as partial solutions for the above concerns. The microstimulators with inductive coupler and integrated voltage regulators [4, 5] can adaptively generate various voltage levels according to the compliance voltage requirements determined by the stimulation pattern profile and electrode characteristics. However, those microstimulators are based on AC–DC converter aren't compatible with multi-source energy harvesters, because they directly convert the energy stored in inductor to the DC power supply for the current drivers. Therefore DC–DC converter based power supplies should be employed to draw energy from multi-source energy harvester. Both capacitive [6] and inductive [7] DC–DC converter were considered for microstimulator design. However, the capacitive DC–DC converter based stimulator in [6] suffer from low efficiency when it has to deal with varying number of electrodes, especially when driving small currents. And the inductive DC–DC converter based stimulator in [7] is not suitable for high-density array driver application because it requires a dedicated DC–DC converter with traditional analog PWM control.

In this paper, a power supply modulated stimulator architecture employing a software-defined reconfigurable bidirectional switching mode power supply (SMPS) is presented and analyzed as a solution that fulfills all the five design requirements that are presented above. The proposed power supply for a generic multichannel stimulators modulate the voltage at an intermediate energy storage capacitor (IESC) instead of directly delivering charge into the electrodes. A generic stimulator in which the stimulation current drivers are decoupled and connected to a power supply modulating DC–DC converter is demonstrated in [8]. The power supply incorporated in [8] takes advantages of two main stimulator-application-specific features to achieve a fast tracking speed ($<10\,\mu s$) at low switching frequency (<1 MHz). Taking those application-specific features into account, some of the important performance measures for traditional power supply controllers can be traded off for a compact, low-power, digital controller. Conventional performance requirements that can be alleviated in the proposed controller include fast adaptation to load transient with regulated output voltage dipping, smooth step response without excessive oscillatory output behaviour, and fast reference tracking speed without output voltage peaking. Two important features of the stimulation waveform make this alleviation possible.

The first feature to be exploited is found during the initialization step at the beginning of the phase transition boundaries, when the output voltage exhibits abrupt ramp-up or -down. At the phase transition boundaries, the current drivers start to conduct current into the electrodes only after the power supply voltage reaches a predefined voltage that can operate the current controlling transistors in the saturation mode. Therefore, the short-term output voltage peaking can be tolerated during the initialization of a new phase, because the current drivers are ensured to be inactivated at the moment. The second useful feature is that the time rate of the target voltage change is slow at less than tens of mV/μs without load transient, once the power supply voltage crosses the initial target voltage level required for current drivers. After reaching an initial operable voltage, a stimulator slowly changes its state variables such as duty ratio and pulse skipping frequency, adapting to an operating condition determined by the number of simultaneously driven electrodes and current amplitude at a stimulation phase.

In this paper, an in-depth evaluation effort of the proposed multichannel microstimulator system is provided, complementing the key concepts and silicon prototype demonstrated in [8]. The comprehensive analysis and simulation assessments for the proposed stimulator achieve following aims:

1. To show how the energy is consumed in each circuit element, the flow of energy from the power source to the electrodes with corresponding energy loss sources during biphasic stimulations is identified.
2. To calculate the influence of the individual subsystem on the overall performance, the transfer functions corresponding to the system blocks are derived using the linearization techniques.
3. To observe the time-domain behavior of the system with varying system and component parameters, a state-space model is provided.
4. To ensure the stability of the system, simulations covering a wide range of the system configurations were performed and some phase-portraits at the parameter corners are provided.
5. To observe real-time trajectories of the internal states during a biphasic stimulus, an experimental system was built and demonstrated.

The rest of the paper is organized as follows. Section 2 describes the operation of the proposed system from various aspects including a biphasic stimulation scenario, a single switching cycle, and algorithm. Then, the dissection of power consuming elements in the system and analytic system models are presented in Sect. 3. Section 4 assesses the reliability of the system from corner simulations and proof-of-concept system emulations. Section 5 concludes the paper.

2 System description

The overall block diagram is shown in Fig. 1. Here, an electrode was approximated by a resistor (R_a) in series with a capacitor (C_{dl}). Similar to [7], the proposed stimulator system employs an switching mode power supply (SMPS) operating in forward buck and reverse boost modes during anodic and cathodic stimulation phases, respectively. However, the proposed system doesn't require a current sensor that increases circuits complexity causing extra power consumption per channel.

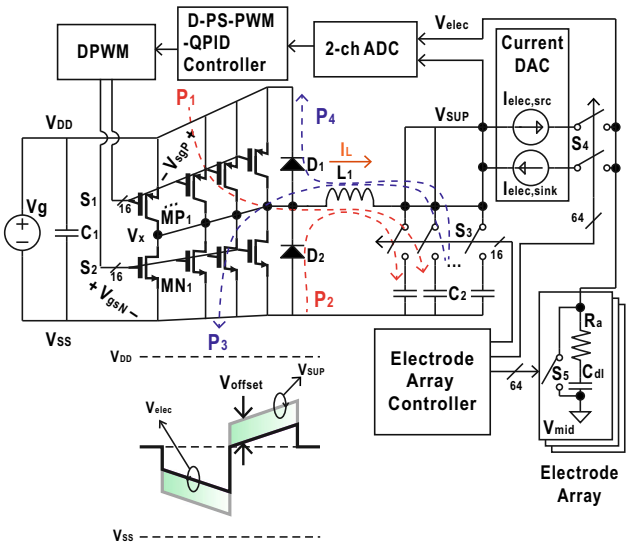

Fig. 1 The generic high-density micro-stimulator system with power-supply modulation and energy recycling

The micro-stimulator system shown in Fig. 1 maneuvers the SMPS, which is tethered to an array of current drivers to efficiently generate biphasic stimuli to the electrode array. In the cathodic stimulation phase, the modulated power supply (V_{SUP}) tracks a reference voltage, which is set to $V_{elec} - V_{offset}$. The offset voltage have to be larger than the voltage headroom of the current control transistors (conducting $I_{elec,src}$, $I_{elec,sink}$), and vice versa in the anodic stimulation phase. In the anodic stimulation phase, on the other hand, V_{SUP} follows the reference voltage which is set to $V_{elec} - V_{offset}$. The system comprises the power source V_g, the input filtering capacitor C_1, an array of complementary power switches (M_{P1}, M_{N1}), 2 diodes (D_1, D_2), an inductor (L_1), an array of the intermediate energy storage capacitors (C_2), a current DAC, a 2-ch ADC, and a digital controller (D-PS-PWM-QPID) for giving instructions to a digital pulse width modulation (DPWM) block that turns on and off the power switches. The load-adaptive power transistor scaling (APTS) and intermediate capacitor scaling (AICS) schemes are employed for attaining a reasonable power conversion efficiency (PCE) of the SMPS regardless of loading conditions, by reducing the switching loss incurred by charging and discharging of the gate capacitance of the power transistors (PT) and the intermediate energy storage capacitor (IESC). These schemes are popular techniques that used when the loading dynamic range is large and the voltage conversion ratio (VCR) coverage is wide [9, 10]. For maintaining reasonable PCE ($\sim 80\%$), the effective switching frequency is adjusted to a lower level by means of 'pulse skipping' when driving small load power, as is employed in [11].

2.1 Time domain description

The proposed system uses the buck converter for forward energy transmission from the power source to the double layer capacitance (C_{dl}), and boost converter for backward energy transmission from C_{dl} back to the power source. Figure 2(a) portrays a waveform of the voltage at the supply voltage node (V_{SUP} in Fig. 1) and the voltage at the electrode interface (V_{elec} in Fig. 1), when driving 64 electrodes with a pair of cathodic-first biphasic pulses having attributes of 1 ms pulse width and ± 600 μA current amplitude. The target voltage headroom across the current controlling transistors (V_{offset}) was set to 1 V. All the simulations in this paper were performed using the

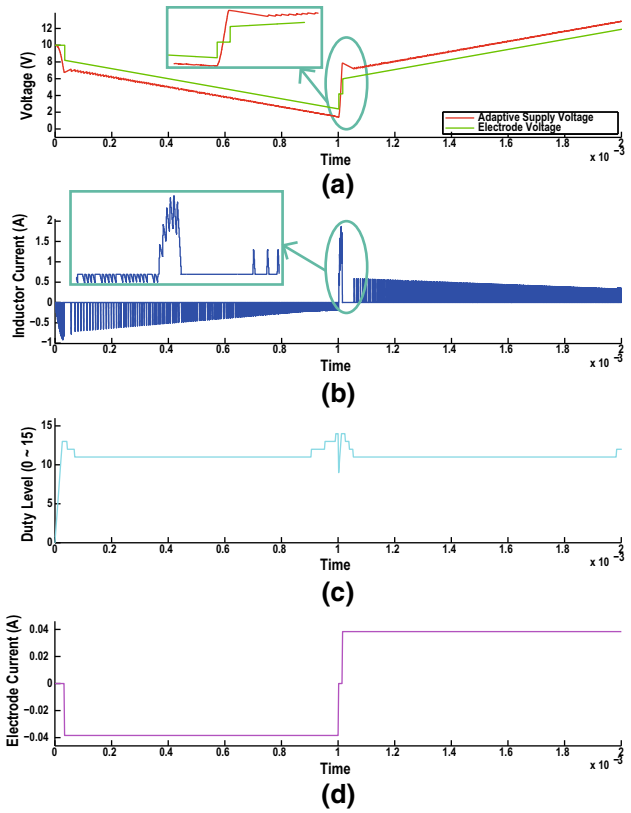

Fig. 2 Waveforms of the proposed stimulation system during a set of cathodic-first bi-phasic stimulation pulses: waveforms of **a** the voltage at the power supply rail (V_{SUP}) and the voltage at the electrode interface (V_{elec}). **b** The current flowing through the inductor (L_1). **c** The duty cycle command. **d** The total current amplitude flowing through the electrodes array

Table 1 Design parameters used for simulations

Item	Value	Item	Value	Item	Value
V_g	20 V	f_s	500 kHz	R^*_{on}	1.6 Ω
C^{P*}_{iss}	1000 pF	C^{P*}_{oss}	500 pF	C^{N*}_{iss}	500 pF
C^{N*}_{oss}	250 pF	I_{RRM}	10 mA	t_{rrb}	10 ns
R_{bond}	200 mΩ	R_{ESR}	50 mΩ	R_{DCR}	50 mΩ
C^*_2	2.2 μF	L	7.2 μH	R_a	3 kΩ
C_{dl}	100 nF	N_{elec}	32	N_{ADC}	8
N_{DPWM}	4	N_{no}	5	N_{cont}	5
V_{offset}	1 V	V_{thres1}	0.5 V	V_{thres2}	0.25 V
A_e	7.2 mm^2	l_e	23.1 mm	μ_e	1120
N_{turn}	4	K_{fe}	16 W/m^3	α	1.26
β	1.46	C_L	3.9 fF	$t_{sw[rf]}$	5 ns

* Indicates the maximum value, when the AICS and the APTS connect the system to full load.

The superscript 'P' indicates parameters of MP_1, and the superscript 'N' indicates the parameters of MN_1.

N_{no} indicates **No_Pulse_Cnt_Max**, N_{cont} indicates **Cont_Pulse_Cnt_Max**

design parameters shown in Table 1, if not otherwise specified. At the onset of a stimulation cycle, both V_{SUP} and V_{elec} are initialized at the bulk tissue potential (V_{mid}), which is defined by a reference electrode exhibiting very fast kinetics to effectively work as a voltage regulator [12]. Then, the stimulator drives V_{SUP} to a voltage level defined as $V_{ref,rev}$, where $V_{ref,rev} = V_{elec} - V_{offset} - I_{DAC} \times R_a$, I_{DAC} is the driving current controlled by the current DAC, and R_a is the electrode access resistance. V_{offset} should be large enough to operate the current controlling transistors into saturation region. The regulated drain-source voltages (V_{offset}) ensures a reasonably high output resistance of the current drivers, which, in turn, attenuates the voltage ripple at the power supply (V_{SUP}). Thus the current flowing through the electrode is kept consistent. To reach the target reference voltage (V_{ref}) as fast as possible, the controller quickly increases the 4-bit duty number, as shown in the Fig. 2(c). The rule for duty update is detailed in Sec. 2.4. Once V_{SUP} reaches V_{ref}, the controller turns on the switches between the electrode and the current driving transistors (S_4 in Fig. 1). Then, cathodic current starts to flow from the electrode to the C_2, discharging the double layer capacitor (C_{dl}), resulting in a downward slope voltage waveform. At the moment that the current starts to flow through the electrode, V_{elec} drops further by $I_{DAC} \times R_a$. The charges collected on C_2 are relayed into the power source through the reverse boost converter operation which will be explained in Sec. 2.2. At $1ms$, the cathodic phase ends, and the anodic phase starts. Responding to the fast transient of V_{elec} at the phase transition boundary, the proposed nonlinear digital controller rapidly ramps up the duty number to accelerate the speed of charge delivery from the power source to C_2, as shown in Fig. 2(c). At this boundary, the converter operates in continuous conduction mode (CCM) as shown in the inset of Fig. 2(b), while the converter operates in discontinuous conduction mode (DCM) during current stimulation. There is a voltage overshoot across C_2 at the beginning of the anodic stimulation. However, the overshoot causes no harmful ramification on tissue such as over-current into the electrode because the current controlling transistors serve as barriers between the power supply and the electrodes. When V_{SUP} crosses over $V_{ref,fwd}$, current starts to flow from C_2 to the electrode array, for the rest of the $1ms$ anodic pulse duration. During the anodic stimulation phase, charges are transferred from the power source to the electrode via C_2, and are accumulated on C_{dl} resulting in an upward slope waveform of V_{elec}.

2.2 Single-cycle operation of the bidirectional converter

Figure 3(a) illustrate DCM operations for the reverse-boost case. During the time period annotated with T_1, the controller turns on the NMOSFET switch (M_{N1}), by raising V_{gsN} to "high". In the beginning of the period, M_{N1} discharges the V_x node to V_{SS}. After that, during the time period annotated with T_2, the controller turns off M_{N1}, pulling down V_{gsN} to "low". In the beginning of the period, energy stored in L_1 sets the voltage at V_x to $V_{DD} + V_F$, closing the conduction path through D_1. When all the energy stored in L_1 is released, L_1 acts as a DC short circuit connecting V_{SUP} and V_x. This period is annotated with T_3, where I_L returns to zero after delivering a short period of the diode reverse recovery current.

Figure 3(c) illustrates the CCM operation for a switching cycle. The system starts to operate in CCM, when the incremental inductor current during a switching cycle – $\Delta I_L = \frac{V_{SUP}-V_{SS}}{L} DT_s$ – is greater than the current flowing into C_2 ($\bar{I}_{transition}$), where D is the duty ratio and T_s is the switching period. The average current required for charging the ascending V_{SUP} during the cathodic-to-anodic phase transition period is $\bar{I}_{transition} = \frac{C_2 \cdot (2 \cdot V_{offset} + 2 \cdot I_{DAC} \cdot R_a)}{\Delta T_{transition}}$, where $\Delta T_{transition}$ is the time to take for the output voltage transition [8]. Thus, the SMPS is more likely to operate in a deeper CCM region, when R_a, V_{offset}, and C_2 are greater, and the fact tells us that, when the number of simultaneously driving electrodes increasingly, C_2 should also be upscaled accordingly, as is done by AICS scheme.

V_{SUP} decreases when the magnitude of I_L is greater than the total sinking current through the electrodes array, $I_{elec,sink}$ (shown in 3(a)), and increases when the magnitude of I_L is smaller than $I_{elec,sink}$. In the forward buck converter operations, illustrated in Fig. 3(b), (d), the energy flow direction is the opposite of that during the reverse boost operation. In the anodic stimulation phase, $I_{elec,src}$ flows from C_2 to the electrodes. The energy consumption at C_2 is recovered from V_g by the forward buck operation of the SMPS.

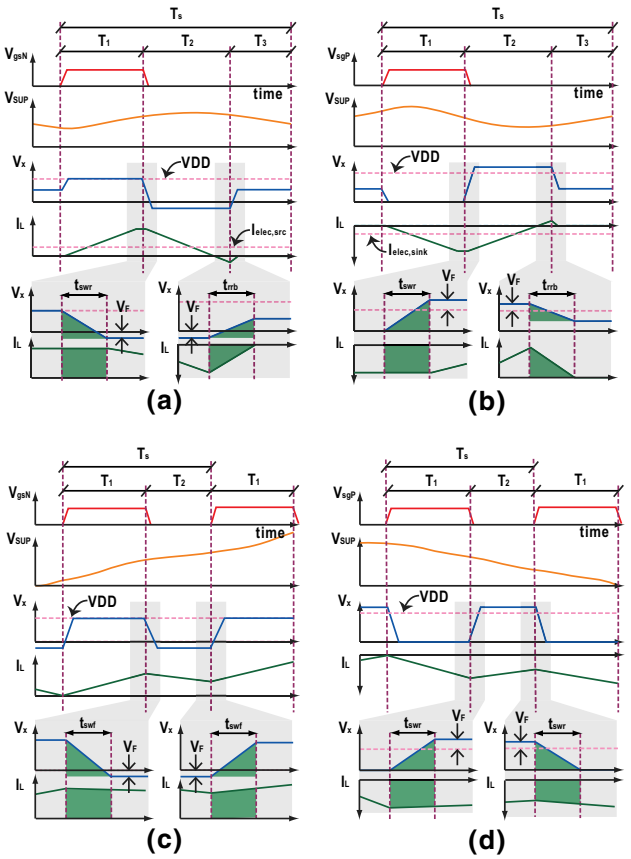

Fig. 3 Key waveforms during a cycle of the forward-buck conversion phase and the reverse-boost conversion phase. Timing diagram for **a** the DCM forward-buck operation, **b** the DCM reverse-boost operation, **c** the CCM forward-buck operation, and **d** the CCM reverse-boost operation

2.3 Existing controllers considered for the PSM stimulator

Although there have been a tremendous amount of the efforts to tackle some of those challenges listed above, to our best knowledge, they could only satisfies part of the requirements among them. Conventional full-fledged DC–DC converters are designed to robustly exhibit a nimble output response with a suppressed output voltage ripple and ringing [13, 14]. However, in the DC–DC converter for stimulator application, some degree of output voltage peaking and ripple is acceptable, only if the output supply voltage can put the current controlling transistors in saturation mode; the influence of the ripple voltage on the current amplitude is attenuated due to high output resistance of the current controlling transistors.

The most viable candidate for the PSM stimulator applications is the SM controllers. The SM controllers continuously monitor all the time-varying state variables such as the output voltage error, its derivative and integral, and the inductor current. The controller commands the power switches to direct the trajectory of the state variables to follow a sliding surface toward a stable operating condition. However, design and implementation of the strict SM controllers incur high cost, since the electronic circuitry involving the switching-inputs should be meticulously designed to satisfy the hitting, existence, and stability conditions [15].

The proposed controller can be described in terms of the SM controllers [16], where the switching manifold is a hyperplane defining the error between V_{SUP} and the target voltage diminishes to zero. In the reaching phase, V_{SUP} will

be driven to a target voltage to prepare for the DAC to steer current trough the transistors, and in the sliding-mode phase, V_{SUP} is induced into the switching manifold.

2.4 Operation of the D-PS-PWM-QPID controller

Shown in the first decision branch of Fig. 4, the D-PS-PWM-QPID controller judges whether it needs to move an electric charge from C_{IESC}, and skips a pulse at the consecutive switching cycle. The controller updates the duty in a manner that is similar to the traditional proportion-integral-differential (PID) controller. The duty is encoded into 4-bit digital codes, thus providing 16 levels of time division of the switching cycle for the digital pulse width modulation (DPWM). The effective resolution of the DPWM is calculated as $R_{DPWM} = \log_2(2^{N_{DPWM}}/D_{max})$, where D_{max} is the maximum duty cycle, N_{DPWM} is the bit-length of the duty value. Here, we can tune R_{DPWM} by adjusting D_{max}, so that the SMPS can adopt to the asymmetric output voltage range depending on the phase. For instance, when the SMPS need to drive the cathodic-first bi-phasic stimuli, as shown in Fig. 2, V_{SUP} spans a range between 2 and 12 V when $V_g = 20$ V. Hence, we adjusted D_{max} of the forward buck operation ($D_{max} \approx 0.7$, $R_{DPWM} \approx 4.51$) to be less than that of the reverse boost operation ($D_{max} \approx 0.3$, $R_{DPWM} \approx 5.74$), to balance the I_L slope by compensating the difference between $V_g - V_{SUP}$ and V_{SUP}.

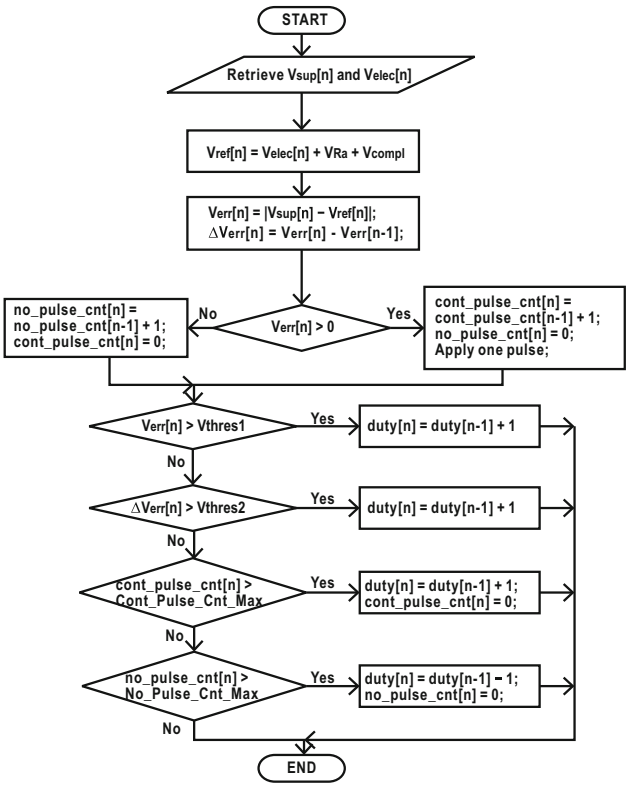

Fig. 4 Flowchart of the digital pulse-skipping PWM controller with quasi-PID duty update. (Adopted from [8])

When the controller determines to turn on the power switch, which shorts the conduction path between the power source (V_g) and the IESC (C_2), it increases the **cont_pulse_cnt** counter value, which stores the history of the number of the consecutive switching cycles without pulse skipping, and resets the **no_pulse_cnt** counter value, which stores the history of the number of the dormant cycles with pulse skipping. When the controller decides to skip a switching cycle, in contrast, it increases the **no_pulse_cnt** value, and reset the **cont_pulse_cnt** value. The two counter values convey 'time integral' information to the controller; when **cont_pulse_cnt** is larger **Cont_Pulse_Cnt_Max**, the controller routine judges that the duty is higher than a desired level and increase the duty by one; while **no_pulse_cnt** is larger than **No_Pulse_Cnt_Max**, the controller judges that the duty is lower than the desired level and decrease the duty by one. In effect, **Cont_Pulse_Cnt_Max** dictates the maximum consecutive active switching cycles, while **No_Pulse_Cnt_Max** puts a lid on the maximum pulse skipping cycles. The 'proportional and derivative' parts of the duty update are quite straight forward; the duty increases by one when V_{errror} is greater than $Vthres1$, and decreases by one when the differential error, $\Delta V_{error}[n] = V_{error}[n] - V_{error}[n-1]$, is greater than $Vthres2$. The duty update logic can be embodied with four 8-bits digital comparators (2 for integral, 1 for proportional, and 1 for derivative control) and one duty counter.

3 System analysis

An ideal adiabatic electrical stimulator system transfers the energy from the source directly into the electrodes array, and then recollects the energy on the double layer capacitance of the electrodes back into the energy source. Thus, without considering energy losses, net total energy consumption of the bidirectional DC–DC converter-powered stimulator during a biphasic pulse cycle is zero. However, energy loss during the charge delivery conducted by the SMPS is inevitable, thus we need to study the energy flow from the power source to the electrodes to figure out how the energy is consumed during the transmission. These loss sources are accounted in the simulator which is based on the state space model, which is also detailed in this section. Using the simulation parameters of the Table 1, the PCE as a function of N_{elec} is plotted in Fig. 5, with the loss equations that will be discussed in this section.

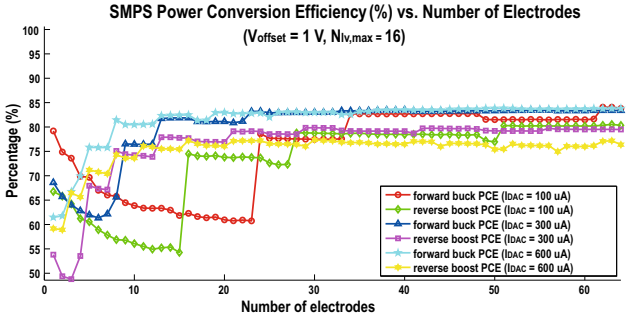

Fig. 5 Simulated power conversion efficiency of the proposed SMPS calculated during a set of the biphasic stimuli, as N_{elec} increases from 0 to 64, when $V_{offset} = 1$ V

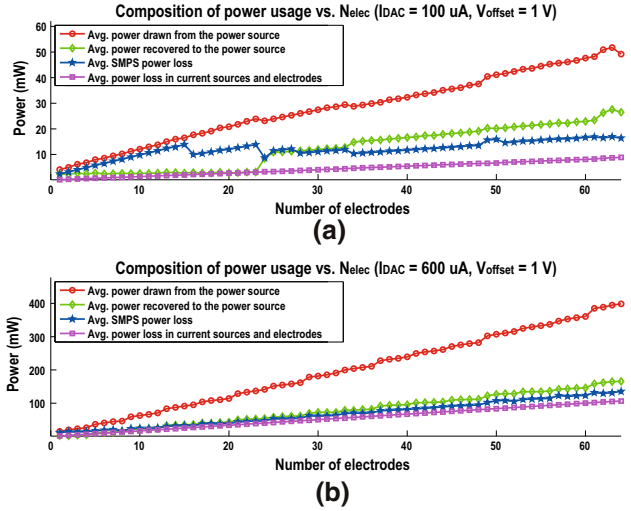

Fig. 6 Average power compositions pertaining to a set of the biphasic stimuli, as N_{elec} increases from 0 to 64, when **a** $I_{DAC} = 100\,\mu$A, and **b** $I_{DAC} = 600\,\mu$A. The power loss in current sources and electrodes is the average of $P_{loss,Ra} + P_{loss,CCT}$ during a pair of biphasic stimuli

3.1 Power consumption

In the proposed system, the energy drawn from the power source is lost as: (1) heat in the current sources and electrodes, and (2) the conduction, switching, and core losses in SMPS. And the remaining energy less the losses is recovered to the power source. In the cathodic stimulation phase, energy is drawn from double layer capacitances of the electrode; then the energy is gradually stored in the inductor as the inductor current (I_L) amplitude rises; and the energy is finally transferred to the power source as I_L amplitude decreases. In the anodic stimulation phase, electric charge is transferred from an energy reservoir (V_g), passes through the IESC, then arrives at the electrodes, ramping up V_{SUP} to track the time-dependent incremental evolution of V_{elec}. The remaining portion of the energy drawn from V_g but not recovered to the source are consumed by the SMPS operations ($P_{loss,SMPS}$) and the current driving operations in the current controlling transistors and the access resistances (R_a) of the electrodes array ($P_{loss,CS}$). This portion of energy which is irrevocably lost during the stimulation is expressed as

$$\begin{aligned} E_{loss,PSM,cyc} &= \int_{t=0}^{T_s} P_{from,src}(t)dt - \int_{t=0}^{T_s} P_{to,src}(t)dt \\ &= \int_{t=0}^{T_s} P_{loss,SMPS}(t)dt + \int_{t=0}^{T_s} P_{loss,CCT}(t)dt \\ &\quad + \int_{t=0}^{T_s} P_{loss,Ra}(t)dt, \end{aligned} \tag{1}$$

where $P_{from,src}(t)$ represents the instantaneous power drawn from the source at the time t, during the forward buck operation, $P_{to,src}(t)$ represents the instantaneous power restored back to the source at the time t, during the reverse boost operation, $P_{loss,Ra}$ is the conduction loss across the access resistance of electrode, and $P_{loss,CCT}$ is the conduction loss across the current controlling transistors. Both $P_{from,src}(t)$ and $P_{to,src}(t)$ can also be expressed in relation to the instantaneous power used for energizing the inductor ($P_{L,stored}$) as

$$P_{from,src}(t) = P_{L,stored}(t) + P_{loss,SPMS}(t) \tag{2}$$

$$P_{to,src}(t) = P_{L,stored}(t) - P_{loss,SMPS}(t), \tag{3}$$

where $P_{loss,SMPS}$ is the cost that we have to pay to reduce $P_{loss,CCT}$, compared to the current-source-based stimulator system. The average power composition during a biphasic stiulation cycle as a function of N_{elec} is shown in Fig. 6, in terms of $P_{from,src}$, $P_{loss,SMPS}$, $P_{loss,Ra}$, $P_{loss,CCT}$, and $P_{to,src}$.

3.1.1 Conduction loss

Conduction loss is caused by the energy which is dissipated across the resistive components, mainly as joule heating. The parasitic resistances that contributes the conduction loss are: (1) the turn-on resistance of power transistors, R_{on}; (2) the inductor equivalent series resistance (DCR, R_{DCR}); (3) the capacitor equivalent series resistance (ESR, R_{ESR}); (4) I-R drop via the current controlling transistors–current sources $I_{elec,src}$ and $I_{elec,elec}$ in Fig. 3; (5) the resistance of bonding wire, denoted as R_{bond} leading toward the electrode; and (6) the access resistance of electrodes formed by both an over-potential at the pad-electrode interface and the voltage drop in tissue.

3.1.2 Switching loss

Switching loss appears at the signal transient triggered by the switching circuit elements such as power transistor and

diode. The main constituent parts of the switching loss are: (1) the V-I crossover loss of the power P/NMOS during turn-off time in DCM mode, and turn-on and -off time in CCM mode; (2) diode reverse recovery loss; (3) the charging and discharging of parasitic capacitors of inductor at the switching node (V_x); and (4) the gate driving loss for charging and discharging input capacitance of the power transistors.

Formally putting all the terms comprising the switching loss,

$$P_{loss,sw}(t) = P_{loss,gate}(t) + P_{loss,cross}(t) + P_{loss,rr}(t). \quad (4)$$

The loss induced by driving the gate is given as:

$$P_{loss,gate}(t) = \frac{1}{2} \cdot f_s \cdot C_{iss} \cdot {V_{DD}}^2 \cdot k_t, \quad (5)$$

where k_t is the buffer multiplication factor that account for the loss due to the gate driving buffer changes. The buffer multiplication factor is given by [17]: $k_t = \frac{k^{m+1}-1}{k^m \cdot (k-1)}$, where m is the number of the cascading inverters in the buffer and k is the scaling factor.

The V-I crossover loss that occurs during the voltage transition at the switching node V_x, induced by the switching of the power transistors, as is depicted in Fig. 3. During the DCM mode operation, shown in Fig. 3(a, b), the crossover loss only appears at the turn-off time of the power transistor, since $I_L = 0A$ at the turn-on instant. In the CCM operation, as shown in Fig. 3(c, d), on the contrary, I_L does not return to zero at the turn-on instant, thus the crossover losses occur at both turn-on and turn-off instant. The V-I overlap during the switching transition occurs because the magnetic energy stored in inductor (L_1) is used to charge and discharge the parasitic capacitors associated with the gate terminals of the power transistors (M_{P1}, M_{N1}). During the time when the gate voltage is stuck at 'Miller Plateau', the displacement current through the reverse transfer capacitance, C_{gd} of MP_1–$C_{gd} \cdot dV_d/dt$ at the drain terminal of M_{P1}–gets diverted through the input resistance of M_{P1}. The crossover loss is formulated as:

$$P_{loss,cross}(t) = \frac{1}{2} \cdot f_s \cdot |I_L| \cdot (V_{DD} + V_F) \cdot t_{sw} \quad (6)$$

In addition to the V-I crossover loss, we have to add the loss for charging and discharging of parasitic capacitance at the switching node (V_x). The parasitic capacitance is given by $C_x = C_{oss} + C_L$, where C_{oss} is the output capacitance of the power transistor between drain and source, and C_L is the parasitic capacitance associated with the inductor (L_1). The effect of the parasitic capacitance is not included in the V-I overlap loss, since it is not connected to the gate, of which voltage dominate the duration of the V-I overlap period. The capacitive loss is described as:

$$P_{loss,cx}(t) = \frac{1}{2} \cdot f_s \cdot C_x \cdot {V_{DD}}^2 \quad (7)$$

The last component of the switching loss is the diode reverse recovery loss, which is illustrated in Fig. 3. During t_a, the reverse diode current discharges the minority carriers inside the p-n junction and forms the concentration gradient in a direction that the forward active current of the diode slides through [18]. The reverse voltage across the diode (D_1) in reverse boost operation is $V_{DD} - V_{SUP}$, thus the power loss is

$$P_{loss,rr,rev}(t) = \frac{1}{6} \cdot (V_{DD} - V_{SUP}) \cdot |I_{RRM}| \cdot t_{rrb} \cdot f_s \quad (8)$$

where I_{RRM} is the peak reverse current of the diode. The reverse voltage across the diode (D_2) in forward buck operation is $V_{DD} - V_{SUP}$, thus the power loss is

$$P_{loss,rr,fwd}(t) = \frac{1}{6} \cdot V_{SUP} \cdot |I_{RRM}| I_{RRM} \cdot t_{rrb} \cdot f_s, \quad (9)$$

3.1.3 Core loss

The core loss is a magnetic loss which is especially significant in DCM operation, in which the proposed system works except the phase boundaries. This loss is induced by the changing magnetic energy in the core during a switching cycle; the magnetic energy drawn into the core when the inductor is getting energized is larger than the magnetic energy recovered from the core when the inductor is releasing the stored energy [19]. In this work, we chose a widely accepted method referred as the 'improved generalized Steinmetz equation' (iGSE), formulated based on the parameters of the Steinmetz equation [20]. The iGSE is given as

$$P_{loss,core} = \frac{1}{T_s} \int_0^{2\pi} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt, \quad (10)$$

where ΔB is peak-to-peak flux density, α, β are Steinmetz parameters, and $k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}$. The Eq. (10) tells that the average power loss per unit volume, $P_{loss,core}$, depends on the time history of the domain wall motion (dB / dt) and the peak-to-peak flux density (ΔB).

3.2 System modelling

Building simulator for the inspection of the system behaviour and power efficiencies over various system parameters involves with the development of the system models describing the SMPS. The SMPS can be expressed in terms of the state space models and transfer functions.

3.2.1 Transfer function

A closed loop system can be written as $G_{closed}(s) = \frac{G_{fwd}(s)}{1+G_{fwd}(s)\cdot G_{fb}(s)}$, where $G_{fwd}(s)$ is the forward gain transfer functions (TF), $G_{fb}(s)$ is the feedback network TF. In the system under analysis, the forward gain TF is composed of the three cascaded TF, $G_{ctl}(s)\cdot G_{dpwm}(s)\cdot G_{vd}(s)$, where $G_{ctl}(s)$ is the TF of the D-PS-PWM-QPID controller, which is described in Sect. 2.4, $G_{dpwm}(s)$ is the continuous time model of the DPWM, which is given as $G_{dpwm}(s) = \left(\frac{1}{2^{N_{dpwm}}-1}\right)\cdot e^{-sT_{dpwm}}$, where N_{pwm} is the DPWM resolution and T_{dpwm} is the delay caused by the DPWM circuit. $G_{vd}(s)$ the continuous time model of SMPS of which the input is $V_{err}(t)$ and the output $d(t)$. The feedback part consists of $H(s)$ and the $G_{adc}(s)$. $H(s)$ represents the output voltage sensor gain which is given as $H(s) = \frac{V_{ref}(s)}{V_o(s)}$, and $G_{adc}(s)$ is the continuous time model of the ADC which is given as $G_{adc}(s) = \left(\frac{2^{N_{adc}}-1}{V_{max,adc}}\right)\cdot e^{-sT_{adc}}$, where $V_{max,adc}$ is the maximum voltage of ADC input, N_{adc} is the ADC resolution, and T_{ADC} is the conversion delay. The TF of the D-PS-PWM-QPID controller can be calculated from the input-output relationship, $G_{ctl}(s) = \frac{\mathcal{L}(d(t))}{\mathcal{L}(V_{err}(t))}$, where $\mathcal{L}(\cdot)$ denotes the laplace transform of a continuous time function. The duty function $d(t)$ is given as a function of $f_+(t)$ and $f_-(t)$, where $f_+(t)$ indicates the increment of the duty by 1, and $f_-(t)$ is the decrement of the duty by 1: $\frac{d}{dt}d(t) = \frac{f_+(t)-f_-(t)}{T_s}$.

We can express $f_+(t)$ and $f_-(t)$ based on the flowchart depicted in Fig. 4 as below:

$$\begin{aligned} f_+(t) = H\Bigg(H\Bigg(\sum_{i=0}^{N_{cont}-1} V_{err}(t-iT_s) - N_{cont}\Bigg) \\ + H(V_{err}(t) - V_{thres1}) \\ + H(V_{err}(t) - V_{err}(t-T_s) - V_{thres2})\Bigg) \end{aligned} \tag{11}$$

$$f_-(t) = H\left(\sum_{i=0}^{N_{no}-1} V_{err}(t-iT_s) - N_{no}\right), \tag{12}$$

where $H(\cdot)$ is the Heavyside step function, N_{cont} and N_{no} are **Cont_Pulse_Cnt_Max** and **No_Pulse_Cnt_Max** of the D-PS-PWM-QPID controller, respectively. The continuous time model of the reverse boost and the forward buck converters can be described as an one pole TF:

$$G_{vd,[rev,fwd]}(s) = \frac{G_{d0,[rev,fwd]}}{1+\frac{s}{\omega_{p,[rev,fwd]}/2\pi}} \tag{13}$$

The charge delivered from the energy source V_g into C_2 in the forward boost case, and the charge delivered from C_2 into the energy source V_g are formulated as $Q_{delivered} = 0.5\cdot((D_1+D_2)\cdot T_s)\cdot I_{pk}$, where D_1 is the duty ratio of energizing period, D_2 is the duty ratio of the period when the energy stored in the inductor is released, and I_{pk} is the peak current flowing through the inductor. Peak inductor current in the reverse boost and the forward buck operation are formulated as $I_{pk,rev} = D_1\cdot T_s\cdot V_{sup}/L$, and $I_{pk,fwd} = D_1\cdot T_s\cdot(V_g - V_{sup})/L$, respectively. We can relate D_2 with D_1 as $D_{2,rev} = \left(V_{sup}/(V_g - V_{sup})\right)D_{1,rev}$ for the reverse boost operation, and $D_{2,fwd} = \left((V_g - V_{sup})/V_{sup}\right)D_{1,fwd}$, for the forward buck operation. From the average output current flowing into C_2, the effective resistances across the power source network are expressed as:

$$R_{eff,rev}(D_1) = \frac{10^6\cdot L\cdot {V_g}^2}{D_1\cdot {V_{sup}}^2\cdot\left(D_1+\frac{D_1\cdot V_{sup}}{V_g-V_{sup}}\right)} \tag{14}$$

$$R_{eff,fwd}(D_1) = \frac{10^6\cdot L\cdot V_g}{{D_1}^2(V_g - V_{sup})}, \tag{15}$$

where $R_{eff,rev}(D_1)$ and $R_{eff,fwd}(D_1)$ are the effective resistances in the reverse boost operation, and the forward buck operation, respectively. Now, we can use the small signal linearization technique for deriving the duty to voltage transfer function ($G_{vd,[rev,fwd]}(s)$).

The resulting gain and the pole frequency in the reverse boost operation can be written as:

$$G_{d0,rev} = \frac{-2\cdot D_{rev}\cdot M_{rev}R\cdot V_{SUP}}{10^6\cdot L(1-M_{rev}) - {D_{rev}}^2\cdot M_{rev}\cdot R} \tag{16}$$

$$\omega_{p,rev} = \frac{L(1-M_{rev}) - 10^{-6}{D_{rev}}^2\cdot M_{rev}\cdot R}{R\cdot L\cdot C(1-M_{rev})}, \tag{17}$$

where the duty (D_{rev}) and the conversion ratio (M_{rev}) are given as:

$$D_{rev} = \frac{1.414\sqrt{-I_{elec}\cdot L + I_{elec}\cdot L\cdot M}}{\sqrt{T_s\cdot V_g}} \tag{18}$$

$$M_{rev} = 1 + \frac{0.5\cdot {D_{rev}}^2 T_s\cdot V_g}{I_{elec}\cdot L} \tag{19}$$

3.2.2 State space model

We can express the proposed system with a set of linear, finite state, dynamic equations. We have three state variables of interest: inductor current (I_L), the voltage on C_2 (V_C), and the voltage on the electrode interface (V_{elec}). The equations that express the dynamic evolutions of V_C, V_{elec}, and V_{SUP} are as follows:

$$\frac{dV_{C,rev}}{dt} = \left(\frac{1}{\alpha R_{DCR} C_2}\right) V_C + \left(\frac{1}{\alpha C_2}\right) I_L + \left(\frac{1}{\alpha C_2}\right) I_{elec,sink} \tag{20}$$

$$\frac{dV_{C,fwd}}{dt} = \left(\frac{1}{\alpha R_{DCR} C_2}\right) V_C + \left(\frac{1}{\alpha C_2}\right) I_L + \left(-\frac{1}{\alpha C_2}\right) I_{elec,src} \tag{21}$$

$$\frac{dV_{elec,rev}}{dt} = -\frac{I_{elec,sink}}{C_{dl}} \tag{22}$$

$$\frac{dV_{elec,fwd}}{dt} = \frac{I_{elec,src}}{C_{dl}} \tag{23}$$

$$V_{SUP,rev} = \left(\frac{1}{\alpha}\right) V_C + \left(\frac{R_{ESR}}{\alpha}\right) I_L + \left(\frac{R_{ESR}}{\alpha}\right) I_{elec,sink} \tag{24}$$

$$V_{SUP,fwd} = \left(\frac{1}{\alpha}\right) V_C + \left(\frac{R_{ESR}}{\alpha}\right) I_L - \left(\frac{R_{ESR}}{\alpha}\right) I_{elec,src} \tag{25}$$

where the subscript 'rev' marks for the variables in the reverse boost operation and the subscript 'fwd' marks for the variables in the forward buck operation, and $\alpha = 1 + \frac{R_{ESR}}{R_{DCR}}$.

And the equations that express the dynamic evolutions of I_L in the period marked as T_1 in Fig. 3 are as follows:

$$\frac{dI_{L,rev}}{dt} = \left(-\frac{1}{\alpha L}\right) V_C + \left(-\frac{R_{ESR}}{\alpha L}\right) I_{elec,sink} + \left(\frac{-R_{ESR} - \alpha\left(R_{on,MP1} + R_{DCR}\right)}{\alpha L}\right) I_L \tag{26}$$

$$\frac{dI_{L,fwd}}{dt} = \left(-\frac{1}{\alpha L}\right) V_C + \left(\frac{R_{ESR}}{\alpha L}\right) I_{elec,src} + \left(\frac{1}{L}\right) V_{DD} + \left(\frac{-R_{ESR} - \alpha\left(R_{on,MN1} + R_{DCR}\right)}{\alpha L}\right) I_L \tag{27}$$

The equations for I_L in the period marked as T_2 are as follows:

$$\frac{dI_{L,rev}}{dt} = \left(-\frac{1}{\alpha L}\right) V_C + \left(\frac{-R_{ESR} - \alpha R_{DCR}}{\alpha L}\right) I_L + \left(-\frac{R_{ESR}}{\alpha L}\right) I_{elec,sink} + \left(\frac{1}{L}\right) V_{DD} - \frac{V_F}{L} \tag{28}$$

$$\frac{dI_{L,fwd}}{dt} = \left(-\frac{1}{\alpha L}\right) V_C + \left(\frac{-R_{ESR} - \alpha R_{DCR}}{\alpha L}\right) I_L + \left(\frac{R_{ESR}}{\alpha L}\right) I_{elec,src} - \frac{V_F}{L} \tag{29}$$

The equation for I_L in the period marked as T_3 is $\frac{dI_{L,[rev,fwd]}}{dt} = 0$.

3.2.3 Limit cycle oscillation

Digital controllers can incur the limit cycle oscillation problem, if the resolution of DPWM is not high enough to provide stead-state output that they are controlled by a traditional linear controller [21]. However, in the D-PS-PWM-QPID controller, the DPWM resolution no longer restricts the resolution of the quantized output voltage at which a power system is allowed to settle on; the controller modulates the amount of the energy to transfer into the load, delivering the energy necessary for the reference tracking. In effect, the pulse skipping logic dithers the average amount of the transferred energy to the load throughout the long time frame, by preventing V_{SUP} to periodically fluctuate.

3.3 Discussion

Now, we are ready to answer to the question of how many scaling levels we need to achieve a reasonable amount of power saving over a wide operating range, while paying the smallest possible implementation cost for additional control and switching circuitry. To answer the question, we performed simulations calculating the energy saving percentage, sweeping N_{elec} from 0 to 64, for $I_{DAC} = 100, 300, 600\,\mu A$, of which results are shown in Fig. 7. The energy saving percentage is an indicator of performance, that evinces how much wasted energy is reduced in the proposed system compared to the current source stimulator, given that both have the same power source. In mathematical term, the energy saving percentage is found as $\eta_{waste} = 1 - \frac{E_{waste,PM}}{E_{waste,CS}}$, where $E_{waste,PM}$ is the wasted energy in the proposed stimulator, and $E_{waste,CS}$ is the wasted energy in the conventional current-source-based stimulator without power supply modulation. The energy saving percentage approaches to 50% in all three cases of $I_{DAC} = 100, 300, 600\,\mu A$, as the number of the electrode approaches to 64. As is predicted from the theory, as the loading gets lighter η_{waste} gets smaller, and even reaches to -100%, which means that twice more energy is burnt in the proposed one, compared to the current-source-based stimulator. This is because the DC–DC converter overhead dominates the energy waste when driving a light load; thus APTS and AICS play more significant roles when the load is light. From the results shown in Fig. 7, we judged that $N_{lv,max} = 16$ could be chosen as a possible spot that can have reasonably high η_{waste} values throughout all the loading conditions, with a tractable number of the control lines connected to M_{P1}, M_{N1}, and C_2.

To confirm that the system dynamics described by the state space model and the transfer functions coincide each

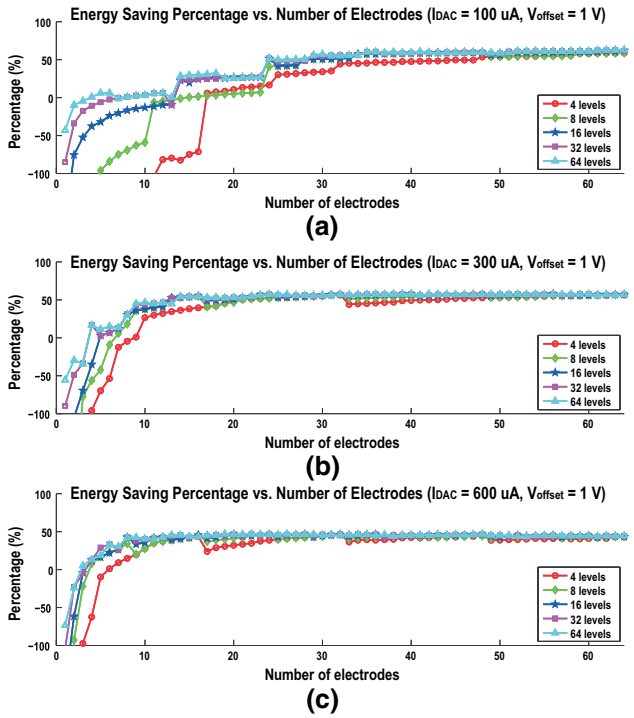

Fig. 7 Wasted energy saving percentage vs. number of stimulating electrodes for various PT and IESC scaling levels, when **a** $I_{DAC} = 100\,\mu A$, **b** $I_{DAC} = 300\,\mu A$, and **c** $I_{DAC} = 600\,\mu A$

other, we will analyze the system under a typical operating point driving the load of $N_{elec} = 32$ and $I_{DAC} = 600\,\mu A$. In this case, the TF of the D-PS-PWM-QPID controller $G_{ctl}(s)$ is calculated to be a constant (≈ 9.2), with the duty function that is updated at the beginning of the switching cycle. Here, we need to take care of the input sinusoidal injection function ($V_{err}(t) = sin(\omega t)$), of which the frequency is less the switching frequency (f_s).

The system parameters involved to calculate the TF (G_{vd}) from the duty ratio to V_{SUP} are $V_{SUP} = 10$ V, $C_2 = 1.1\,\mu F$, $M_{rev} = 2$, $D_{rev} = 0.083$, $G_{d0,rev} = 92.17$, $\omega_{p,rev} = 278$, $M_{fwd} = 0.5$, $D_{fwd} = 0.083$, $G_{d0,fwd} = 92.17$, and $\omega_{p,fwd} = 278$. The DPWM block typically has a negligible delay compared to the switching frequency, which leads to $N_{DPWM} = 4.58$, $T_{DPWM} = 0$, thus $G_{DPWM} = 1/24$. As for the ADC block which lies on the feedback path, the conversion time can be assumed to be negligible compared to a switching period, which leads to the assumptions that $T_{adc} = 0$ and $H_s = 1$. Finally, we have all the TF components, which are necessary for depicting the TF of the closed-loop reference input tracking system of interest, thus we are ready to analyze the frequency response of the closed loop reference input tracking using the equation below:

$$G_{closed}(s) = \frac{G_{ctl}(s) \cdot G_{dpwm}(s) \cdot G_{vd}(s)}{1 + G_{ctl}(s) \cdot G_{dpwm}(s) \cdot G_{vd}(s) \cdot G_{adc}(s) \cdot H(s)} \quad (30)$$

The resulting bode plot is shown in Fig. 8, from which we can compare the spectral performances calculated from the state space model simulations and from the transfer function analysis.

4 Experimental results

In this section, we assess the stability and performance of the PSM stimulator system using the simulator described in the previous section. Then, the proposed topology with the

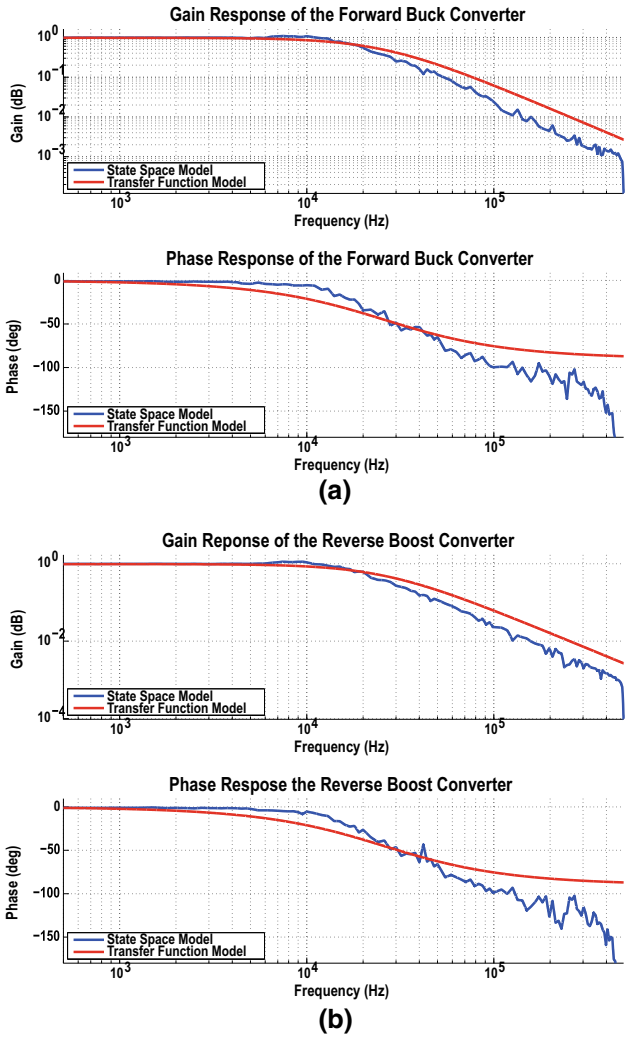

Fig. 8 Bode plots calculated by state space model and transfer function analysis, for **a** forward buck operation, and **b** reverse boost operation

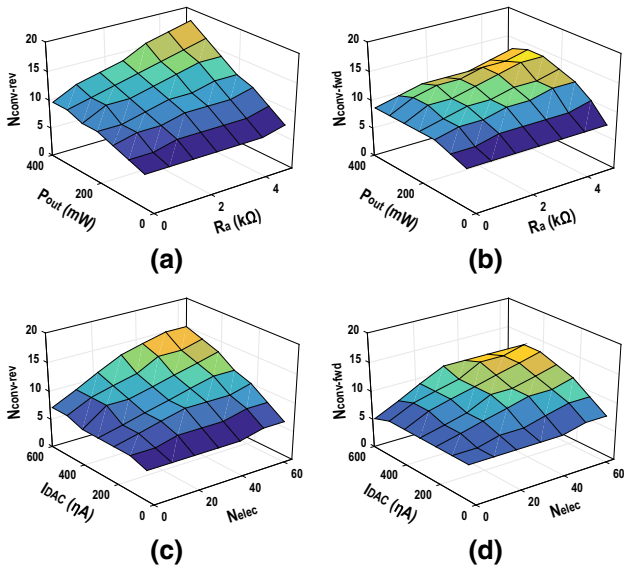

Fig. 9 Convergence speed of the bidirectional SMPS for microstimulator when driving a biphasic pulse. (*Upper row*) Number of switching cycles (N_{conv}) taken for V_{sup} to reach the switching manifold over various load resistances (R_a) and output power (P_{out}) **a** in the reverse boost mode, and **b** in the forward buck mode. (*Lower row*) N_{conv} taken for V_{sup} to reach the switching manifold over various stimulation current amplitudes (I_{DAC}) and number of electrodes (N_{elec}) **c** in the reverse boost mode, and **d** in the forward buck mode

D-PS-PWM-QPID controller is shown to be feasible for realization on a verification platform, which consists of off-the-shelf components and a FPGA board communicating with PC using an USB interface.

4.1 Numerical assessment

We first undertook extensive validation of the PSM stimulator system over a wide range of loading configurations using a simulation code based on the state-space model with power losses being accounted. Here, we evaluate whether or not the D-PS-QPID-PWM controller can stably drive the power supply by quickly converging into the switching manifold at the phase transition boundaries.

To measure converging performance of the SMPS, the number of switching cycles for the stimulator to settle on the switching manifold from initial phase changing event (N_{conv}) was used. N_{conv} is extracted from the time-domain simulation waveform at the beginning of the cathodic pulse, and at the cathodic-to-anodic inter-phasic boundary. Figure 9 reveals that N_{conv} is bounded less than 18 switching cycles ($\sim 36\,\mu s$ or 3.6% of a pulse duration) for wide range of the loading configurations spanning over $I_{DAC} = 0 \sim 600\,\mu A$, $P_{out} = 0 \sim 400$ mW, and $N_{elec} = 0 \sim 64$. Table 2 compares the converging speed of the D-PS-PWM-QPID controlled bidirectional converter with some state-of-the-art converters designed for DVS power supply. In absolute time scale, converters in some works [24, 25] exhibit steady-state operating points faster than this work. However, after normalizing the converging speed in terms of the number of switching cycles required to settle at initial target operating point (N_{conv}), the proposed SMPS consumes significantly less cycles than others, including a bidirectional converter employed for a PSM stimulator [7].

Next, we also confirmed that the SMPS with the D-PS-PWM-QPID controller is stable for over the wide range of the loading configurations of concern. The phase plot, displayed in Fig. 10, validates that the system error function (V_{err}) and its derivative vanish toward the origin; thus the stability of the system can be ensured over a wide range of the loading.

4.2 Verification platform

The D-PS-PWM-QPID controller is programmed in the FPGA, according to the flowchart of Fig. 4; it retrieves the ADC output values of V_{elec} and V_{SUP}, and determines a 4-bit duty level and the **Pulse_Enable** signal which indicates whether to apply a set of pulses or not for the upcoming switching cycle. for DPWM block. The DPWM block drives the gates of the power switches. The DPWM block modulates the duration of the gate driving

Table 2 Converging speed at the discontinuous boundary of the phase transitions

Refs.	[7][b]	[22]	[23]	[24]	This Work
Topology	Bidirectional buck–boost	Buck–boost	Buck–boost	Buck	Bidirectional buck–boost
Control scheme	Current mode	Hysteresis	Current mode	Voltage mode	Digital voltage mode
Switching frequency (MHz)	0.25	10	5	10	0.5
Up-tracking time (μs/V)	208	93	20	1.7	5
Down-tracking time (μs/V)	208	27	15	4.4	6.4
Up-tracking N_{conv}[a]	292	5208	560	93	14
Down-tracking N_{conv}[a]	292	1512	420	248	18

[a] The values are normalized for a voltage transition of 5.6 V, which was derived in the time-domain scenario shown in Fig. 2.

[b] Estimated from the corresponding literature

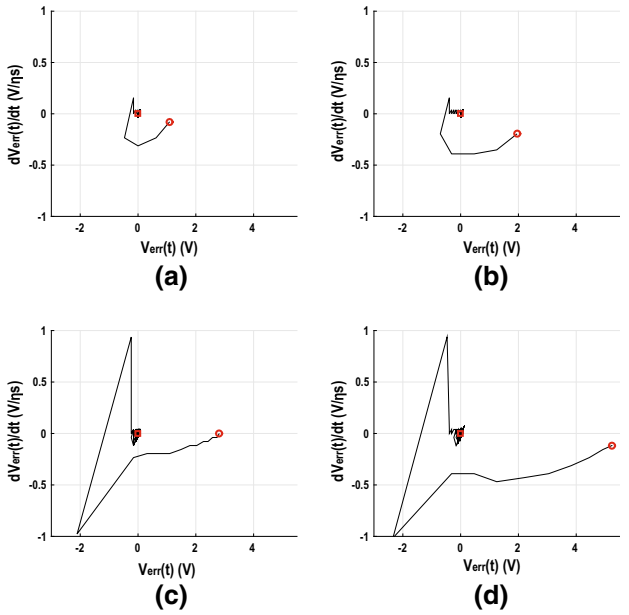

Fig. 10 Phase portrait plot of the bidirectional SMPS for microstimulator when driving cathodic-first biphasic pulses of **a** $I_{DAC} = 100\,\mu A$ to an electrode during the reverse boost phase, and **b** during the forward buck phase, and when driving **c** $I_{DAC} = 600\,\mu A$ to 64 electrodes during the reverse boost phase, and **d** during the forward buck phase

pulses for MP_1 and MN_1 that close the conduction path between **VDD** (or **VSS**) and the inductor (L_1) of the LC filter. The body diodes of the power switches are used as a pair of anti-parallel diodes of Fig. 1, when both power switches are open, and the inductor has the energy to be released on to the IESC. At the end of a pair of stimuli, the FIFO DAQ I/F report the voltage waveforms during the stimulation to the PC, and the D-PS-PWM-QPID controller report the dynamics of **Pulse_Enable** signal and **duty level** signal during the preceding pair of stimuli to the PC.

4.3 Observation

The dynamics of the internal state variables of the blocks programmed on the FPGA can be stored and transferred to the PC, so that we can observe how the blocks under test behave, according to the block attributes. Figure 11 shows the timing diagrams of the important internal signals of the D-PS-PWM-QPID controller, when $V_{offset} = 1$ V, $I_{DAC} = 300\,\mu A$, and $N_{elec} = 16$. Figure 11(a) shows the input signals of the D-PS-PWM-QPID, which are the 8-bit ADC codes of the voltages at the model electrode and the modulated power supply. Figure 11(b) shows the Pulse Enable signal which indicates whether an energy packet is processed during the time slot, or not. The **Cont_Pulse_Cnt_Max** attribute determines the maximum number of consecutive pulses, while the

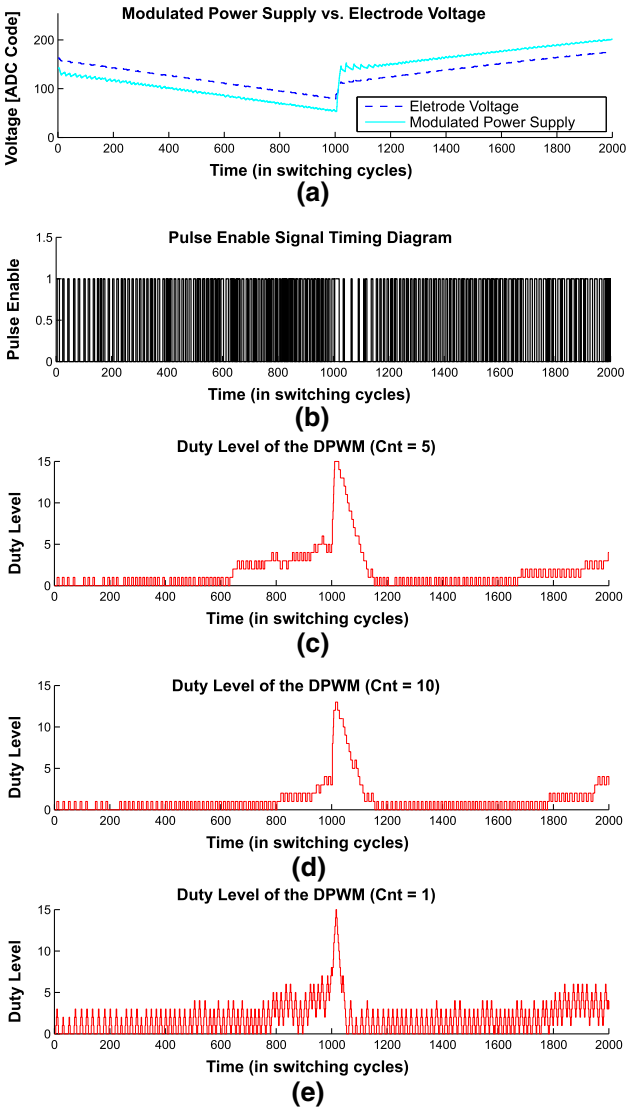

Fig. 11 Measured duty level dynamics pertaining to various **Cont_Pulse_Cnt_Max** and **No_Pulse_Cnt_Max** values, when $V_{offset} = 1$ V, $I_{DAC} = 300\,\mu A$, and $N_{elec} = 16$. **a** V_{elec} and V_{sup} voltage waveforms during a set of biphasic stimulus. **b** Pulse enable signal. **c** Duty level when **Cnt** (= **Cont_Pulse_Cnt_Max** = **No_Pulse_Cnt_Max**) = 5. **d** Duty level when **Cnt** = 1. **e** Duty level when **Cnt** = 10

No_Pulse_Cnt_Max attribute determines the maximum number of cycles that are skipped without a pulse. These two attributes, together, set boundaries where duty level is adjusted for adapting the load power. We performed experiments under the conditions that **Cont_Pulse_Cnt_Max** = **No_Pulse_Cnt_Max** = **Cnt** = 5, for the timing diagrams shown in Fig. 11(a–c); **Cnt** = 10, for the result shown in Fig. 11(d); and **Cnt** = 1, for the result shown in Fig. 11(e). The number of consecutive pulses, **Cont_Pulse_Cnt**, which is indicated by the duration that the **Pulse Enable** signal is raised, is the number of switching cycles taken for V_{SUP} to cross over the target reference voltage to track. The number of switching cycles

without a pulse, **No_Pulse_Cnt**, is an indicator that V_{SUP} needs to be adjusted to track the target reference voltage. If **Cnt** is set to be too small, as shown in Fig. 11(e), the duty level responds too sensitively to the transient SMPS output voltage, resulting in oscillatory behavior. On the other hand, if **Cnt** is set to be too large, as shown in Fig. 11(e), the duty level is too inertly adjusted, resulting in long time periods of the consecutive pulses or idle state.

5 Conclusion

The PSM stimulator with the-D-PS-PWM-QPID controller can accommodate a broad dynamic range of the output loading conditions, while supporting fast transient tracking capability with robustness notwithstanding the power stage transfer function. Spots of energy losses are identified in the light of energy flow of the stimulator, traversing from the source power reservoir, via SMPS converter and current drivers connected to electrodes, and back to the source power reservoir. Analysis on the scaling PT and IESC for preventing the power consumption overhead for the power supply modulation from increasing beyond the amount of power saving from the power supply modulation is given. A set of state-space model is derived for behavior simulation of the stimulator design. And transfer functions describing the frequency response of the design are derived for understanding reference tracking capability of the design in spectral domain. The converging speed and stability of the system were assessed using the simulations which implements the state-space model incorporating the energy losses. Finally, a proof-of-concept experimental platform was presented to observe internal state dynamics of the D-PS-PWM-QPID controller with varying values of the attributes.

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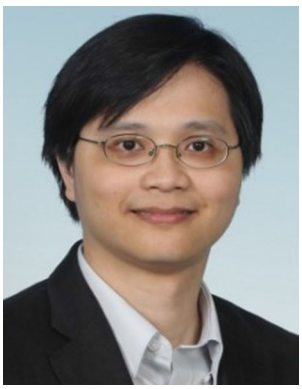

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