A 4-μm Diameter SPAD Using Less-Doped N-Well Guard Ring in Baseline 65-nm CMOS

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***Abstract*— This brief reports a small size single-photon avalanche diode (SPAD) in baseline 65-nm CMOS suitable for low-cost time-of-flight application with high spatial resolution. By exploiting the less-doped n-well region to surround the vertical p-well/deep-n-well multiplication region, the electric field at the SPAD periphery can be reduced without process modifications while avoiding premature lateral breakdown. Validated using TCAD simulations, the fabricated 4-μm diameter SPAD device exhibits a compact device size with a low dark count (73 cps/μm^2 at 20 °C) and a high fill factor (17.7%) using 65-nm baseline CMOS, while demonstrating competitive performance when compared with the state of the art.**

***Index Terms*— Baseline CMOS, premature lateral breakdown, single-photon avalanche diode (SPAD), small pitch.**

I. Introduction

WITH the continuous development of advanced applications such as 3-D-imaging and object ranging, reducing the pixel pitch and increasing the fill factor of single-photon avalanche diode (SPAD)-based imager are becoming a major trend. Implementing compact SPAD devices with reduced junction area exhibits various advantages, including low dark count, reduced after-pulsing probability [1], and improved timing accuracy [2]. Moreover, advanced CMOS technologies also offer the possibility of reducing the footprint of in-pixel electronics. However, the requirement of an explicit guard ring for preventing premature lateral breakdown is still one of the major hurdles for the downsizing of SPAD pixels. Even though the introduction of the retrograde deep n-well as a virtual guard ring can effectively reduce the SPAD size with an active area diameter down to 1–2 μm [3], [4], the requirement for the p-well block fabrication step may not be well supported in baseline CMOS processes.

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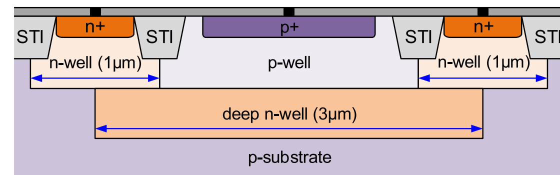

Fig. 1. Cross section of the proposed 4-μm-diameter SPAD device in baseline 65-nm CMOS, with the blue arrows indicating the design rule limited dimensions.

In this brief, we report a compact SPAD implemented in a baseline 65-nm triple-well CMOS technology. We study the feasibility of using the less-doped n-well region to confine the electric field gradients at the SPAD periphery to suppress premature lateral breakdown. The corresponding electric field distribution, together with that of the retrograde deep n-well approach, is also investigated using TCAD simulation. The fabricated SPAD prototype with 4-μm diameter demonstrates robust operation while achieving competitive performance when compared with the state of the art without using customized CMOS image sensor (CIS) processes.

II. Device Construction

The cross section of the SPAD device is shown in Fig. 1. The p-well region is surrounded by the n-well ring and the deep n-well layer, with the breakdown events happening between the p-well and deep n-well interface. The device size is limited by the design rule of the chosen process. The minimum width of the deep n-well is 3 μm. An n-well width of 1 μm results in a 4-μm SPAD device with a 2-μm diameter active area. Due to the lack of process options in the chosen process with respect to [3] and [4], we exploit the less-doped n-well (i.e., lower-doping level relative to that of deep n-well [5]) as the guard ring instead of using the retrograde deep n-well or p-epitaxial layer. The exact doping concentration is defined by the chosen process. The reduced electric field at the p-well/n-well junction can enforce the SPAD breakdown at the deep n-well/p-well interface where a higher electric field exists, resulting in a compact SPAD structure compatible with baseline CMOS.

To study the internal built-in electric fields for the proposed SPAD structure, we model the proposed SPAD device in COMSOL Multiphysics for studying the relationship between the p-well/deep n-well junction with reference to the

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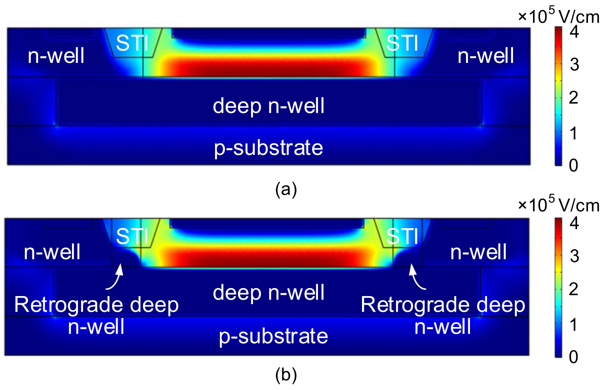

Fig. 2. TCAD simulation illustrating the electric field profile of (a) the proposed SPAD and (b) the SPAD with retrograde deep n-well in [3] and [4].

process parameters in [6]. As shown in Fig. 2(a), the electric field is $\sim 2 \times 10^5$ V/cm in guard-ring region which is $\sim 2\times$ lower than that at the avalanche junction. Due to the highly doped deep n-well region, the high electric field (red) can be restricted at the vertical p-well/deep n-well interface, achieving robust SPAD operation without premature lateral breakdown at a moderate excess bias voltage (V_{EB}). The shallow trench isolation (STI) exhibits a negligible effect on the device operation [4].

The simulated electric field distribution of the retrograde deep n-well structure in [3] and [4] is also shown in Fig. 2(b). It can be observed that both techniques can restrict the high electric field in the center of the active area where the p-well overlaps with the deep n-well region, with the electric field gradually reduced toward the lateral edge. Notice that the average electric field of the lateral p-well/n-well junction in the proposed structure is larger than that of the p-well/retrograde deep n-well one, mainly attributed by the receding doping profile of the retrograde deep n-well near the surface. However, the improved electrical isolation is at an expense of increased device area (design rule limited) and process incompatibility.

III. Experimental Results and Discussion

The proposed 4-μm SPAD device is fabricated in a baseline 65-nm CMOS process. We evaluate the validity of the proposed structure for preventing the premature lateral breakdown using the light emission test at varying V_{EB}, as shown in Fig. 3. When biased at $V_{EB} = 1$ V, the emitted light disappears gradually toward the edge, and no premature edge breakdown is observed as shown in Fig. 3(b). However, as in Fig. 3(c), a bright ring around the active region, which indicates breakdown activities at the edge, exists when $V_{EB} = 2.8$ V. Fig. 3(d) shows the measured dark count rate (DCR) with varying V_{EB}. As observed, the DCR drastically increases with $V_{EB} > 2.2$ V due to the second breakdown at the edge, indicating the maximum V_{EB} to achieve safe operation of the proposed SPAD.

We further study the avalanche behavior of the proposed SPAD using a passive quenching circuit with an external 30-kΩ resistor. The breakdown voltage (V_{bd}) is measured to be about 9.6 V at room temperature. Fig. 4 shows the measured DCR as a function of V_{EB} inside the temperature chamber SH-261. The DCR at $V_{EB} < 0.8$ V is dominated by the tunneling, while that at $V_{EB} > 1.6$ V is mainly determined by thermal generation–recombination. It can be observed that the normalized DCR ($V_{EB} = 2.2$ V at 20 °C) is about 1 kcps, which is better than [7] and [8] due to the reduced tunneling noise from increased depletion region formed by the p-well/deep n-well junction.

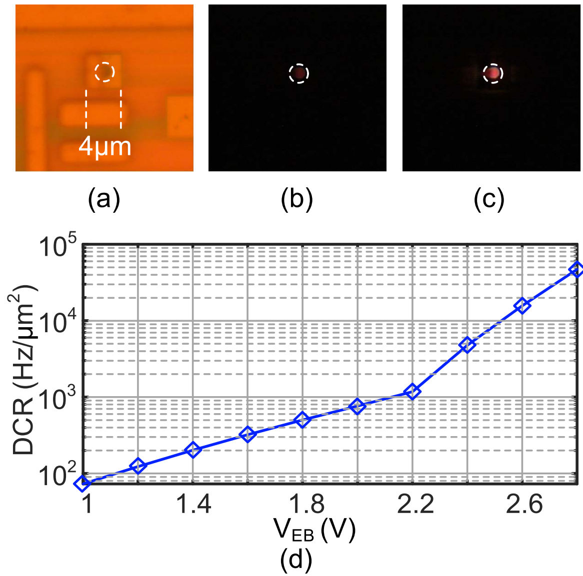

Fig. 3. (a) Chip micrograph of the proposed SPAD in 65-nm baseline CMOS, and light emission test results at (b) $V_{EB} = 1$ V; (c) $V_{EB} = 2.8$ V; and (d) measured DCR at varying V_{EB}.

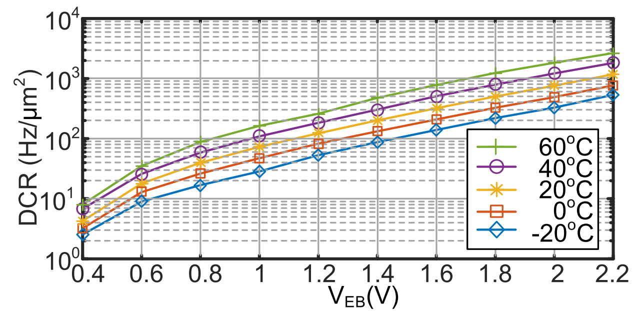

Fig. 4. Measured DCR against V_{EB} at different temperatures.

Fig. 5 shows the photon detection efficiency (PDE) with an incident wavelength from 300 to 900 nm, defined as

$$\mathrm{PDE} = \frac{N_{\mathrm{Counts}} - N_{\mathrm{DCR}}}{N_M} \quad (1)$$

where N_{Counts} is the number of recorded avalanche events, N_{DCR} is the measured dark counts, and N_M is the measured number of photons radiated from the monochromator (Newport 74100) using the optical power meter (Newport 2936-C).

The PDE is the combination of electron and hole avalanche triggering probabilities. At ultraviolet (UV) wavelength, the avalanche events are mainly contributed by electrons while they are dominant by holes in the infrared region. The electron-induced avalanche dominates over the hole-induced one due to its higher ionization coefficient. It can be observed that the PDE decreases as wavelength increases due to the higher penetration depth (i.e., deeper into the n-side) at a longer wavelength, contributing to more hole-induced avalanche. The PDE enhances when V_{EB} increases from

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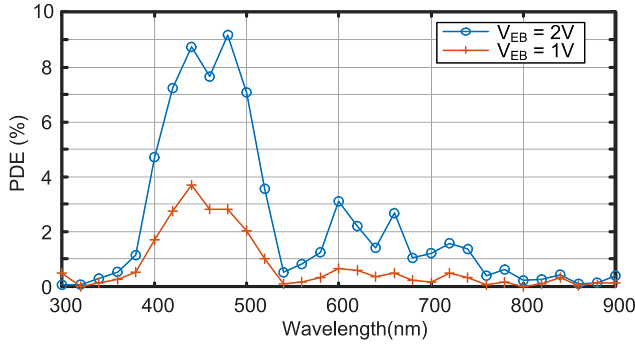

Fig. 5. Measured PDE with respect to the wavelength at different V_{EB}.

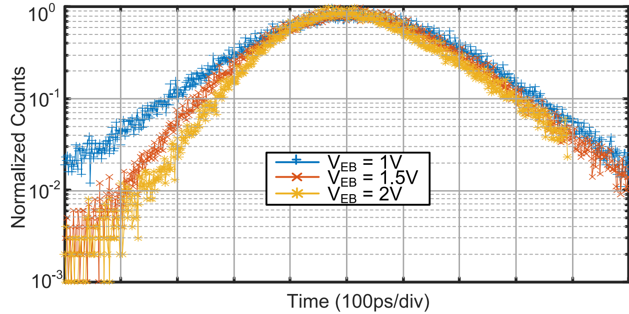

Fig. 6. Measured time jitter with respect to the wavelength at different V_{EB}.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[4]	[7]	[8]	This work
Technology	130nm CIS	65nm CMOS	130nm BSI CMOS	65nm CMOS
PN Junction	P-well /Deep N-well	N-plus /P-well	NLDD /P-well	P-well /Deep N-well
Guard Ring (GR) type	Retrograde Deep N-well virtual GR	Modified N-well GR	N-well GR	Less-doped N-well GR
Active area	3.14μm²	64μm²	28μm²	2.8μm²
Device area	50.2μm²	Not Reported	121μm²	16μm²
Fill Factor#	6.25%	Not Reported	23.3%	17.7%
DCR (V_{EB}=1V)	2.9cps /um²@25°C V_{EB}=1.2V	6.25kcps /um²@20°C V_{EB}=0.2V	1.25kcps /um²@25°C	73cps /um²@20°C
PDE	14% @500nm V_{EB} = 1.2V	5.5% @420nm V_{EB} = 0.25V	12.2% @700nm V_{EB}=1.5V	9.2% @480nm V_{EB} = 2V
Jitter†	66ps @470nm	155ps @637nm	260ps @750nm	158ps @485nm

† Laser jitter excluded
# Fill Factor = Active area/Device area

1 to 2 V as a result of a larger avalanche triggering probability. The increased wavelength at maximum PDE when compared with [7] is due to the deeper multiplication region from the surface. The peak PDE is 9.2% at 480 nm with $V_{EB} = 2$ V which is competitive when compared with [7]. The oscillations in the PDE curve are mainly due to the dielectric layers on top of the SPAD [9], [10].

We characterize the timing jitter by illuminating the sensor with a pulsed laser and measuring the timing interval between the trigger signal and SPAD pulse. The laser source (Advanced Laser Diode Systems, GmbH, Germany) operates at 40 MHz at 485 nm. During the measurement, one photon is detected at every one hundred laser pulses on average to avoid the pile-up effect [11]. Fig. 6 shows the measured normalized timing jitter with different V_{EB}. With a laser jitter of 80 ps, the full-width half maximum (FWHM) responses are 343, 286, 238 ps at $V_{EB} = 1$, 1.5, and 2 V, respectively.

Table I summarizes the proposed SPAD with the state of the art. When compared with the existing SPADs in baseline CMOS technology [7], [8], this brief demonstrates a compact SPAD with a small device size and a low DCR in 65-nm baseline CMOS. We can achieve a $\sim$2.8$\times$ improvement in higher fill factor with a comparable device active area when compared with the CIS implementation in [4].

IV. CONCLUSION

This brief reports a compact SPAD structure by exploiting the less-doped n-well region to surround the vertical p-well/deep n-well multiplication region. The reduced electric field at the SPAD periphery without process modifications can prevent premature lateral breakdown. TCAD simulations and measurement results from the fabricated prototype in baseline 65-nm CMOS demonstrate the validity of the proposed SPAD for compact time-of-flight applications.

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