A 6.5 × 7 μm^2 0.98-to-1.5 mW Nonself-Oscillation-Mode Frequency Divider-by-2 Achieving a Single-Band Untuned Locking Range of 166.6% (4–44 GHz)

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***Abstract*—The common self-oscillation-mode (SOM) frequency dividers have a high-Q sensitivity curve limiting the locking range (LR). This letter reports a non-SOM (NSOM) frequency divider-by-2. Fabricated in 65-nm CMOS, it occupies a die area of 6.5 × 7 μm^2, and measures a single-band untuned LR of 166.6% (4–44 GHz), over a small input range <0.15 V_{pp}. The key technique is a load-modulated dynamic latch aided by a current-reuse cross-coupled pMOS pair. The achieved figure-of-merit of 26.6 GHz/mW compares favorably with the state-of-the-art.**

***Index Terms*—5G bands, current-mode-logic (CML), figure-of-merit (FOM), frequency divider, locking range (LR), non-self-oscillation-mode (NSOM), phasor, self-oscillation-mode (SOM).**

I. Introduction

Self-oscillation-mode (SOM) frequency dividers (Fig. 1) are widespread in mm-wave local oscillator (LO) generators. The injection-locked frequency divider (ILFD) [1], [2] supports high-frequency operation at low power, but its high-Q sensitivity curve (SC) narrows the locking range (LR), complicating the design of its driving oscillator that has to deliver a wide output swing. The inductive load of ILFD also penalizes the area efficiency. The current-mode-logic (CML) [3] divider enjoys a wider LR, but at the cost of static power and smaller output swing. An inductance load is also essential to extend the operating frequency. To surmount those tradeoffs, recent efforts have been focused on the inductorless dynamic-latch dividers [4]–[8]. With a tunable load, the SC can be shifted via V_{tune}, resulting in a broader LR made by multiple sub-bands. Regrettably, dynamic-latch-based dividers suffer from several shortcomings: 1) the LR is very sensitive to the parasitic effects; 2) both the LR and center frequency of each sub-band is susceptible to the noise of V_{tune}; and 3) only the manual control of V_{tune} was achieved in [4]–[7], while a closed-loop control [8] comes at the cost of extra circuitry and area to secure a clean V_{tune}. Also, the topologies in [4]–[8] only support division-by-4, which restricts the I/Q generation frequency to be 4× lower than that of the oscillator.

This letter proposes a non-SOM (NSOM) frequency divider-by-2. It offers a very wide single-band LR and relaxes the input power range. The key technique is a load-modulated dynamic latch assisted by a current-reuse cross-coupled pMOS pair (XCPP). Prototyped in 65-nm CMOS, our divider-by-2 occupies only 6.5 × 7 μm^2 core area. Without any tuning, the single-band LR covers from 4 GHz to at least 44 GHz, with a power consumption up to 1.5 mW. The achieved figure-of-merit (FOM) of 26.6 GHz/mW compares favorably with the recent art.

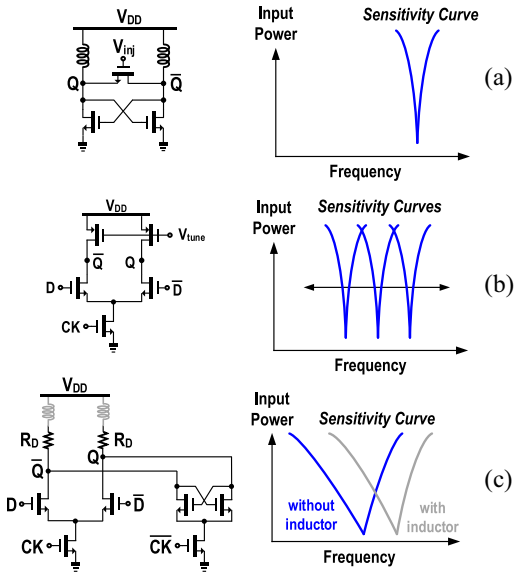

Fig. 1. (a) ILFD and its SC. (b) Dynamic latch (to build a divider) and its SC. (c) CML latch with the resistive load R_D (to build a divider) and its SC.

II. Proposed Divider-by-2

As shown in Fig. 2(a), our divider-by-2 generates the I/Q outputs (V_{OI} and V_{OQ}) by incorporating two dynamic latches ($L_{1,2}$). They are driven by two complementary clock phases (CK and $\overline{\text{CK}}$) at the frequency f_{CK}. The RF input (RF_{IN}) along with its common-mode level ($V_{\text{CK,CM}}$) is provided via an off-chip broadband isolation balun (BAL-0067). It has an amplitude imbalance of 0 ± 0.5 dB and phase imbalance of 180 ± 5° across the frequency range from 300 kHz to 67 GHz. Fig. 2(b) depicts the schematic of the proposed dynamic latch, in which its input signal directly drives the load-modulated pMOS, and the injection nMOS, to realize a rail-to-rail output swing in a pull–push manner. During the sensing phase (CK is high), the differential pair ($M_{1,2}$) steers the tail current to charge the outputs with a first-order time constant $R_O C_L$, where R_O and C_L are the output resistance and parasitic load capacitance, respectively. V_{sw} is the differential output voltage necessary to switch the succeeding latch. To reach V_{sw}, the sensing time (t_1–t_2) of our topology can be much shorter than that (t_1–t_3) of the CML counterpart under the

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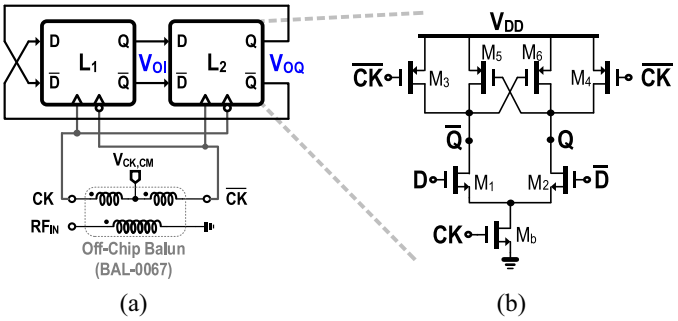

Fig. 2. (a) Complete divider-by-2. (b) Proposed dynamic latch with XCPP.

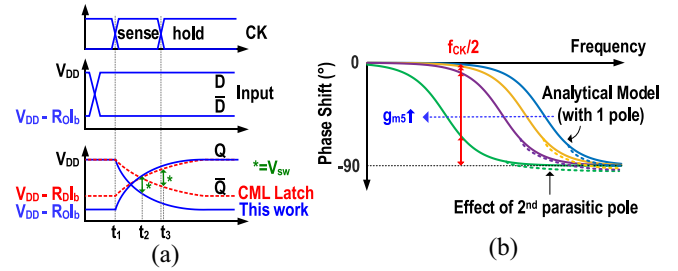

Fig. 3. (a) Proposed latch operation comparing with its CML counterpart. (b) Phase responses of our latch with respect to g_{m5} and the second parasitic pole.

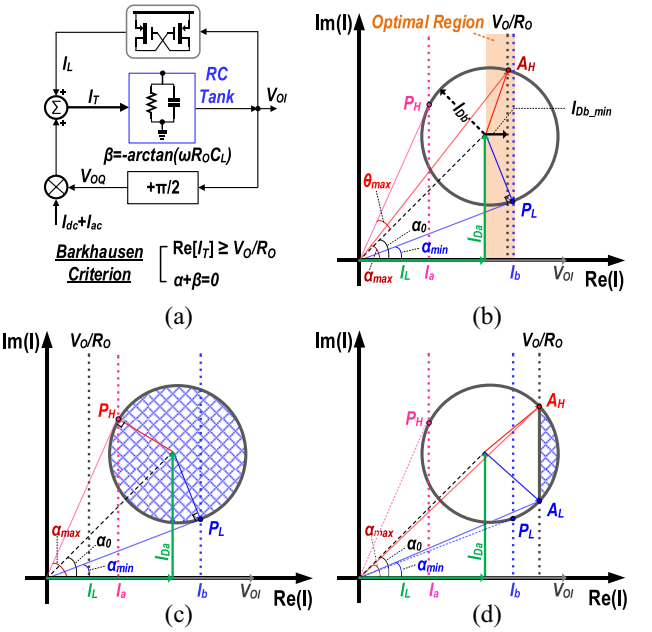

Fig. 4. (a) Behavior model of the proposed divider-by-2. Phasor diagrams of (b) hybrid $[f_{\rm PL}, f_{\rm AH}]$ operating in the NSOM, (c) $[f_{\rm PL}, f_{\rm PH}]$ operating in the SOM and (d) $[f_{\rm AL}, f_{\rm AH}]$ operating in the NSOM. Note that $\alpha_{\rm min} = \alpha_0 - \theta_{\rm max}$ for (b) and (c).

same total power budget. Also, by increasing the transconductance (g_{m5}) of the XCPP, additional phase shift can be generated by a latch [Fig. 3(b)]. These properties allow our latch to support division-by-2 easier than [5]–[8]. Hence, the Barkhausen criterion can be satisfied by applying a proper input swing as $V_{\rm CK}$. For a given $f_{\rm CK}$, a larger g_{m5} yields a higher sensitivity (i.e., smaller $V_{\rm CK}$). The extra phase shift due to the high-frequency parasitic pole forces our divider-by-2 to operate alike a two-stage differential ring oscillator. During the holding phase (CK is low), the cut-off tail transistor (M_b) prevents the dropdown of the high-level output. Note that there is no dc current path in our latch, differing from its CML counterpart that consumes dc power. Meanwhile, the low-level output is sustained by the modulated load ($M_{3,4}$) that has a large off-resistance. Thus, our divider favors low-frequency operation, and we can allocate more dc current to the sensing-phase operation, resulting in a larger output swing close to rail-to-rail [see Fig. 5(b) later].

III. Phasor-Based LR Analysis

In the behavior model of our divider-by-2 [Fig. 4(a)], $M_{1,2}$ in L_1 behaves as a single-balanced mixer. It helps to mix the dc current ($I_{\rm dc}$) + injected ac current ($I_{\rm ac}$) at $f_{\rm CK}$, with the $V_{\rm OQ}$ at $f_{\rm out}$. The total current (I_T) flowing through the RC tank is the combination of the current (I_L) generated by the XCPP, and the output current ($I_{\rm Da} + I_{\rm Db}$) of $M_{1,2}$, where $I_{\rm Da}$ and $I_{\rm Db}$ are denoted by mixing $V_{\rm OQ}$ with $I_{\rm dc}$ and $I_{\rm ac}$, respectively. The injection ratio (η) is given by $I_{\rm ac}/I_{\rm dc}$ that is determined by $V_{\rm CK}$. The phase difference (α) between I_T and $V_{\rm OI}$ should be compensated by the RC tank's phase (β), under proper injection-locked operation. The theoretical background is the following: let us consider the phasor $V_{\rm OI}$ as a reference in the phasor diagram [Fig. 4(b)]. I_L is in phase and $I_{\rm Da}$ is in quadrature, while the phase difference assigned between $I_{\rm Db}$ and $V_{\rm OI}$ is arbitrary. By calculating α, the four limiting conditions of the upper and lower operating frequencies can be derived: ($f_{\rm AL}$, $f_{\rm AH}$) in (1) for amplitude-limited (gain condition) and ($f_{\rm PL}$, $f_{\rm PH}$) in (2) for phase-limited (phase condition)

$$\begin{cases} f_{\rm AL} = \left(-\sqrt{\left(\frac{1}{4}g_{m1}\eta\right)^2 - \left(g_{m5} - \frac{1}{R_O}\right)^2} + g_{m1}\right)/(2\pi C_L) \\ f_{\rm AH} = \left(\sqrt{\left(\frac{1}{4}g_{m1}\eta\right)^2 - \left(g_{m5} - \frac{1}{R_O}\right)^2} + g_{m1}\right)/(2\pi C_L) \end{cases} \tag{1}$$

$$f_{\rm PL} = \frac{\tan(-\theta_{\rm max} + \alpha_0)}{2\pi R_O C_L}, \quad f_{\rm PH} = \frac{\tan(\theta_{\rm max} + \alpha_0)}{2\pi R_O C_L}. \tag{2}$$

Here, we obtain the phase shift α_0 without $V_{\rm CK}$ injection and the maximum additional phase shift $\theta_{\rm max}$ as

$$\alpha_0 = \arctan\left(\frac{g_{m1}}{g_{m5}}\right) \text{ and } \theta_{\rm max} = \arcsin\left(\frac{\frac{1}{4}g_{m1}\eta}{\sqrt{g_{m5}^2 + g_{m1}^2}}\right).$$

We observe that possible solutions only exist on the right side of V_O/R_O due to the Barkhausen criterion [$\mathrm{Re}(I_T) \geq V_O/R_O$]. Depending on the relative position between V_O/R_O and $[I_a, I_b]$, our divider has three possible cases to define its LR: 1) $V_O/R_O < I_a$ leads to $[f_{\rm PL}, f_{\rm PH}]$ in Fig. 4(c); 2) when V_O/R_O falls into $[I_a, I_b]$, the LR is dominated by $[f_{\rm PL}, f_{\rm AH}]$, shown in Fig. 4(b) and it corresponds to the SC in Fig. 5(a); and 3) when $V_O/R_O > I_b$, the operating frequency range is $[f_{\rm AL}, f_{\rm AH}]$ as shown in Fig. 4(d). Here, P_L and P_H are the lower and upper tangency points from the origin to the circle, respectively, indicating the phase condition. Accordingly, I_a and I_b are defined as the projections of P_H and P_L on the real axis, respectively. A_H and A_L intersect the vertical line of V_O/R_O with the circle providing the gain condition.

If $V_{\rm CK,CM}$ is large enough to have $g_{m5}R_O > 1$, the divider enters into SOM operation at the free-running frequency $f_{\rm OSC} = g_{m1}/(2\pi g_{m5} R_O C_L)$. An increase of $V_{\rm CK,CM}$ results in larger $g_{m1,5}$ and R_O. Adjusting $V_{\rm CK,CM}$ can effectively tune $f_{\rm OSC}$ but the reduced open-loop gain in the large-signal behavior of our divider at high frequency limits the upper operating frequency and shrinks LR equivalently. Therefore, a lower $V_{\rm CK,CM}$ allows the divider to stay

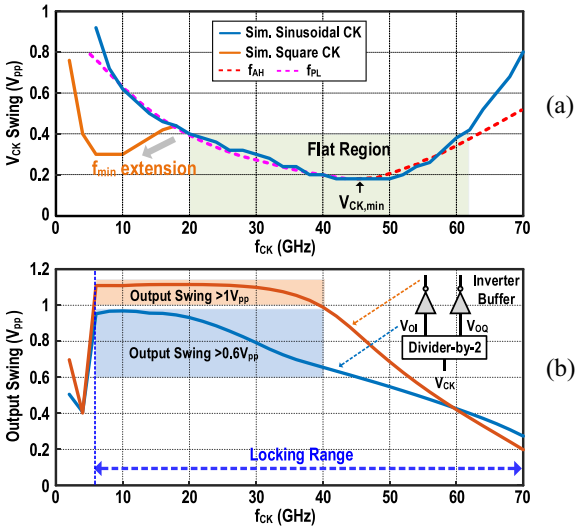

Fig. 5. (a) Simulated and calculated SCs under the NSOM ($g_{m1} = 1.97$ mS, $g_{m5} = 78.18$ μS, $g_{mb} = 3.21$ mS, $I_{dc} = 356.9$ μA, $R_O = 2.09$ kΩ, and $C_L = 13.95$ fF). (b) Corresponding output swings of the divider-by-2 and inverter buffer.

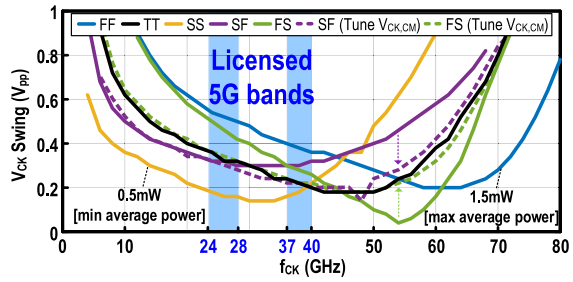

Fig. 6. Simulated SCs under the key process corners: fast-fast (FF), slow-slow (SS), typical-typical (TT), fast-nMOS-slow-pMOS (FS), and slow-nMOS-fast-pMOS (SF).

operating in the NSOM (boundary), due to the pull–push topology formed by the load-modulated pMOS and XCPP, and the injection nMOS. When $V_{CK,CM}$ is small enough to obtain $g_{m5}R_O < 1$, it secures the NSOM and the divider consumes less power. The gain crossover point shifts toward the high frequency, raising the upper limit of the operating frequency. To operate in the flat region of the SC, the minimum I_{Db} ($I_{Db,min}$) is $V_O/R_O - |I_L|$, and the minimum V_{CK} ($V_{CK,min}$) is $8I_{dc}(1-g_{m5}R_O)/(g_{m1}g_{mb}R_O)$. If $V_{CK,CM}$ is further reduced, $V_{CK,min}$ will rise, and finally the divider will be unlocked.

The proposed divider can be biased to operate in the SOM as well. From simulations, with $V_{CK,CM} = 0.6$ V yields $f_{OSC} = 13$ GHz. The corresponding LR ranges from 6 to 42 GHz under $V_{CK} = 0.8$ V_{pp}. When we set $V_{CK,CM} = 0.45$ V, our divider enters the NSOM since the end of I_L is $< V_O/R_O$ [Fig. 4(b)]. The upper limit is extended to 70 GHz at $V_{CK} = 0.8$ V_{pp}. A flat SC across ~40 GHz is attained with an input-swing variation of 0.22 V_{pp} ($V_{CK,min} = 0.18$ V_{pp}). The hybrid criterion [f_{PL}, f_{AH}] dominates the upper and lower limits of the operating frequency. The consistency of the calculated and simulated results validates our analysis [Fig. 5(a)]. Particularly, when compared with the sinusoidal input, the square-wave input, exhibiting a steeper rising/falling edge, aids extending the lower limit of the operation frequency with no extra power, especially at ~10 GHz when $V_{CK,CM}$ is small. As shown in Fig. 5(b), our divider has a simulated output swing close to rail-to-rail between 5 and 30 GHz, and still >0.6 V_{pp} up to 40 GHz it is adequate to drive up an inverter buffer (0.67 mW) to recover a rail-to-rail output swing up to 40 GHz, which is suitable for a recent oscillator-bufferless wireline circuit [9].

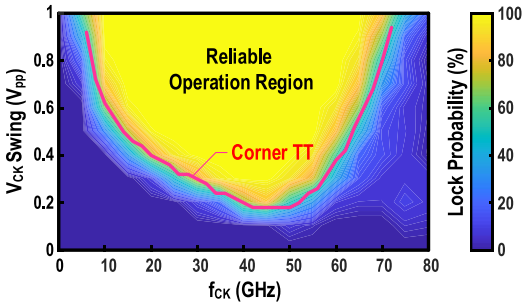

Fig. 7. Monte-Carlo simulation of lock probability in the contour around the TT-corner SC as reference (100× Monte-Carlo simulation result).

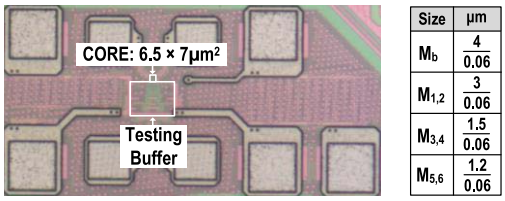

Fig. 8. Die photograph (left) and fabricated size (right) of our latch in Fig. 2(b).

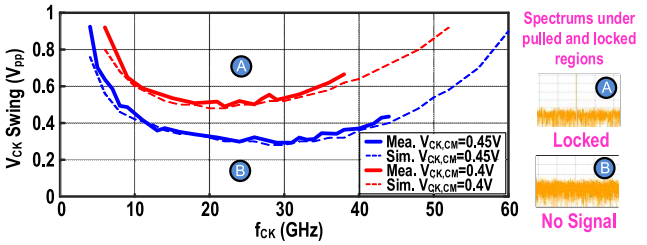

Fig. 9. Measured (solid) and post-extraction (PEX) simulated (dashed) SCs of our divider-by-2 in NSOM.

Under the key process corners, all the simulated SCs (Fig. 6) cover the licensed 5G bands [10], consuming an average power from 0.5 mW (leftmost SC) to 1.5 mW (rightmost SC). Tuning $V_{CK,CM}$ help us securing NSOM operation, namely, that both undershoot SC (SF) and overshoot SC (FS) can be adjusted to the expected SC (TT) in Fig. 6. Also, we perform 100× Monte-Carlo simulations to observe the reliable operation region (Fig. 7) around the TT-corner SC, it covers ~60 GHz in the NSOM when $V_{CK,CM} = 0.45$ V.

IV. Measurement Results

The proposed divider-by-2 prototyped in 65-nm CMOS is followed by an on-chip test buffer to drive the 50-Ω instrument. Fig. 8 shows the core area of 6.5 × 7 μm^2 and sizing parameters of each latch. Our divider-by-2 dissipates up to 1.5 mW, excluding the inverter and test buffers. Fig. 9 shows the measured and simulated SCs. At the designed $V_{CK,CM} = 0.45$ V, the input-frequency range is maximized from 4 to 44 GHz (i.e., LR of 40 GHz), with an input-swing variation as low as 0.15 V_{pp} from 44 GHz down to 10 GHz. Based on our analysis, pushing V_O/R_O to the right of the two tangent points [see Fig. 4(b)] will limit the LR. This happens as expected if $V_{CK,CM} = 0.4$ V, yielding a narrower [f_{AL}, f_{AH}] of 6–38 GHz, and the input swing has to be enlarged by 1.67× ($V_{CK,min} = 0.5$ V_{pp}). Thus, V_O/R_O should be sized in the optimal region [Fig. 4(b)] to maximize the LR. The required V_{CK} can be easily supplied with the large oscillator's swing [11] (e.g., >1 V). If the low-frequency phase and high-frequency amplitude conditions are unsatisfied (i.e., below the SC in Fig. 9), no signal appears. The input and output of our divider-by-2 show the expected 6-dB difference of phase noise

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameters	This Work	JSSC'13 [9]	CICC'08 [3]	JSSC'17 [1]	JSSC'18 [2]	ISSCC'11 [4]	JSSC'13 [6]	JSSC'17 [8]
Technology	65nm CMOS	65nm CMOS	65nm CMOS	0.13μm BiCMOS	65nm CMOS	65nm CMOS	32nm CMOS	65nm CMOS
Key Technique	Dynamic Latch + Load Modulation + XCPP	Forward Source Follower Injection	CML	Distributed IL	4th-order Transformer-Based	Dynamic Latch + Tunable Voltage Bias	Dynamic Latch + Load Modulation + Tunable Voltage Bias	Dynamic Latch + Current Bleeding + Source Coupling
Generation Style	Dynamic	Dynamic	Static	Static	Static	Dynamic	Dynamic	Dynamic
Operation Mode	**NSOM**	SOM	SOM	SOM	SOM	SOM	SOM	SOM
Need Tunability?	**No**	No	No	No	No	Yes	Yes	Yes
Single-ended Output Swing Capability	**Rail-to-Rail**	Rail-to-Rail	Small	Small	Small	Small	Small	Small
f_{CK}/f_{out} Ratio	2	2	2	2	2	4	4	4
f_{min} to f_{max} (GHz)	**4 to 44**	0.4 to 14.5 *	64.7 to 82.3	35 to 59.5	32.3 to 61.9	20 to 70	14 to 70	16 to 67
f_{max} (GHz)	**44** #	14.5 *	82.3	59.5	61.9	70 #	70 #	67 #
L.R. in Total-Band	**166.6%**	189.3% *	24%	53%	62.8%	111.1%	133.3%	122%
L.R./No. in Sub-Band	**166.6% / 1**	189.3% * / 1	24%	22-37% / 2	62.8% /1	10-17% / 9	60-90% / 4	47.1-70% / 3
Power P_{dc} (mW)	**0.98 to 1.5**	0.2 to 0.55 *	15.8	3.8	1.2	1.7 to 6.5	1.3 to 4.8	6.2-8.7
Die Area (μm²)	**6.5 x 7**	~8 x 6	40 x 40	90 x 630	280 x 250	15 x 30	18 x 55	52 x 60
FOM (GHz/mW)	**26.6**	25.6	1.11	6.45	24.7	1.03 to 1.76	6.67 to 17.5	5.87
FOM_H (GHz^2/mW)	**1173**	371.7	92	383.6	1526.9	40.9 to 72.2	481.3 to 654.6	393.3

FOM = $(f_{max} - f_{min}) / P_{dc}$ [6] $FOM_H = [(f_{max} - f_{min}) * f_{max}] / P_{dc}$ [12] * From simulations # Maximum frequency is limited by the available instrument.

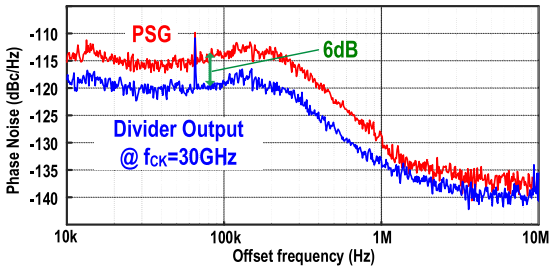

Fig. 10. Measured phase noise at the divider's input and output.

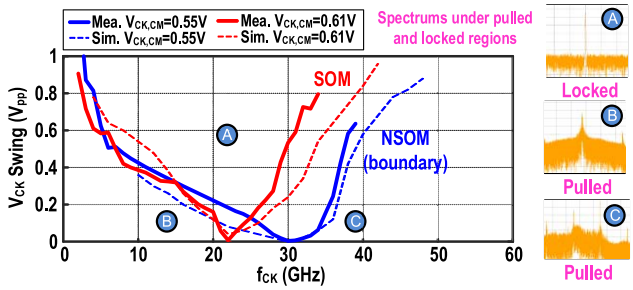

Fig. 11. Measured (solid) and PEX simulated (dashed) SCs in both SOM and NSOM (boundary).

(Fig. 10). Referring to the measured SC in the SOM (Fig. 11), the NSOM (boundary) shows a similar $V_{CK,min}$ of ~5 mV_{pp}, but extends the LR from 20 to 26 GHz under a V_{CK} of 0.4 V. Thus, the NSOM is favored for our divider that can maximize the LR by using an ac-coupled $V_{CK,CM}$. Table I compares the measured performance of our proposed divider with the prior art. Without any tuning, our divider-by-2 locks a wider LR of 166% in a single band, while achieving a higher FOM [6] of 26.6 GHz/mW, and an FOM_H [12] of 1173 GHz^2/mW.

V. CONCLUSION

This letter has reported a frequency divider-by-2 based on a new load-modulated dynamic latch assisted by a current-reuse XCPP. The potential maximum lock range is developed by means of a new NSOM design approach. The proposed divider prototyped in 65-nm CMOS shows a wide LR of both NSOM with larger LR and NSOM (boundary) with minimum input swing, while occupying an ultracompact core area of $6.5 \times 7\ \mu m^2$. Our divider-by-2 is a promising candidate to replace the typical static CML-based divider-by-2 for five features: 1) small input swing requirement; 2) low power; 3) very wide LR; 4) inductorless; and 5) scalability with the advanced processes to extend the upper operating frequency.

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