A Low-Power Compression-Based CMOS Image Sensor With Microshift-Guided SAR ADC

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***Abstract*—This brief presents a low-power compression-based CMOS image sensor for wireless vision applications. The sensor implements low-bit-depth imaging with planned sensor distortion (PSD) to effectively compress both data bandwidth and processing power while maintaining high reconstruction image quality. Accordingly, a column-parallel microshift-guided successive-approximation-register (SAR) ADC is proposed to enable 3-bit PSD imaging based on a 3 × 3 pattern. To support normal imaging with low area overhead, the circuit is reconfigurable as an 8-bit SAR/single-slope ADC. The data bandwidth is further compressed by a customized lossless encoder based on predictive coding and run length coding. A 256 × 216 prototype imaging system composed of the compression-based image sensor and the lossless encoder is fabricated in a 0.18-μm standard CMOS process. Measurement results show that the image sensor achieves 3 bit/pixel (bpp) with 34.9-dB reconstruction peak signal-to-noise ratio (PSNR) and 0.91 structural similarity index (SSIM). With 1/4 spatial downsampling and lossless encoding, 0.31 bpp is obtained with 29.2-dB PSNR and 0.83 SSIM. The sensor consumes 14.8 μW (full resolution) and 4.3 μW (downsampling) at 15 fps, achieving state-of-the-art FoMs of 17.8 and 5.2 pJ/pixel·frame, respectively. Including the encoder, the overall system dissipates as low as 1.2 μJ/frame, making it an attractive solution for wireless sensor networks.**

***Index Terms*—CMOS image sensor, focal-plane compression, planned sensor distortion (PSD), low bit depth, microshift, SAR ADC, wireless sensor networks.**

I. Introduction

CMOS image sensors have seen rapid growth in recent years. In the era of Internet-of-Things (IoT), they play an important role as eyes to enable smart devices see their environment. Targeting emerging wireless vision applications such as implantable bio-sensing, building automation or remote agricultural monitoring, new requirements are imposed on power consumption, data bandwidth, processing and cost of the whole imaging systems due to constrained energy, bandwidth and maintenance. Although the power of image sensors has been pushed to a very low level [1], [2], much higher power is consumed during transfer, processing and transmission of the large-bandwidth image data. The problem is even getting worse when multiple sensors are employed.

The image data bandwidth can be effectively reduced by implementing a digital signal processor (DSP) based on standard compression algorithms such as JPEG/JPEG2000 [3]. However, these methods suffer from complex computation, leading to large power, area and thermal overhead. On the contrary, integrating image compression on the sensor focal plane offers an effective solution to the above problems [4]–[10]. Compared with the digital counterparts [4], the analog compression architectures achieve higher speed, smaller area and lower power [5]–[10]. Nevertheless, previous compression-based image sensors usually provide images with low peak signal-to-noise ratio (PSNR) and small structural similarity index (SSIM), which can hardly be used for computer vision analysis [11]. Furthermore, they still consume too large power, stopping them from practical employment in energy-constrained wireless sensor networks.

Prior works have focused on compressing spatial redundancy while high bit depth is redundant for smart sensing [2]. In contrast, planned sensor distortion (PSD) algorithms have been proposed to suppress image bit depth by exploiting spatial correlation [12], [13]. Different from traditional compression algorithms, PSD not only avoids complex processing but also simplifies frontend image capture. High image quality is still maintained through advanced reconstruction algorithms in the backend. Consequently, PSD promises low complexity, power and bandwidth for the sensor implementation.

In this brief, we propose a first PSD-based CMOS image sensor to improve both data rate and energy efficiency. Column-parallel microshift-guided successive-approximation-register (SAR) ADCs are implemented for PSD imaging with minimum overhead. Using a 3 × 3 microshift pattern, the image bite depth is suppressed to 3 bits, providing the best tradeoff between image quality and bandwidth/power. Further compression is conducted by downsampling and lossless encoding. Reconstructed images demonstrate high PSNR and SSIM. As a result, state-of-the-art energy efficiency and low bandwidth are achieved with high reconstruction image quality.

The remainder of this brief is organized as follows. Section II will describe the PSD-based framework and

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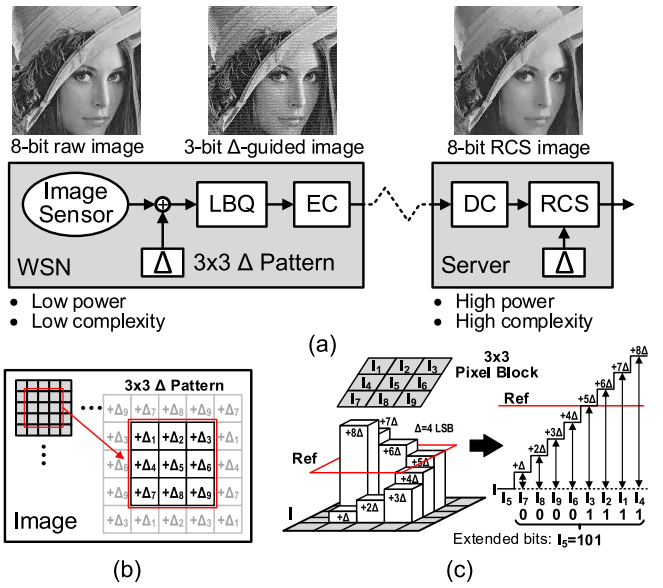

Fig. 1. (a) Proposed PSD-based 3-bit imaging framework; (b) Microshift-guided imaging (3×3 Δ pattern); (c) Reconstruction principle.

microshift-guided ADC. System architecture and circuit implementation will be presented in Section III. Experimental results are shown in Section IV followed by conclusions in Section V.

II. Planned Sensor Distortion Framework

A. PSD-Based Framework

Generally, reducing image bit depth is a direct and simple approach to compress data bandwidth and save processing power. However, aggressive bit depth reduction can cause great image quality loss even though high compression ratio is obtained. Such deteriorated images will severely degrade the accuracy of detection or recognition algorithms [11]. In order to effectively compress bit depth redundancy while maintaining satisfactory image quality, the PSD algorithm is employed to reconstruct high-bit-depth images from low-bit-depth microshift-guided images [12], [13].

A PSD-based 3-bit imaging framework is proposed as shown in Fig. 1(a). It is similar but different to dithering [12]. A predefined microshift (Δ) is added to the image signal before a low-bit-depth quantizer (LBQ). The 3-bit microshift-guided image is further compressed by a lossless encoder (EC) before transmitted wirelessly to the server. The server will first conduct lossless decoding (DC) and then reconstruct (RCS) the image based on the predefined Δ pattern. The framework brings the advantages of low power and low complexity for the wireless sensor node (WSN), even though higher power and complexity are required for high-quality reconstruction on the server, which accord with wireless application requirements.

Fig. 1(b) shows the microshift-guided imaging using a 3×3 Δ pattern. The pattern contains 9 different microshifts, each of which represents a 3-bit sub-quantization level. For the 3-bit imaging, all the 9 sub-quantization levels are $\{0, 4, \ldots, 32\}$ LSB, in terms of 8-bit resolution. The pattern is repeatedly applied all over the image plane so that within a 3×3 pixel block, all sub-quantization levels are included.

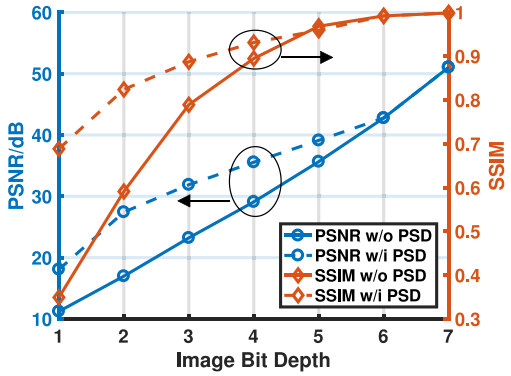

Fig. 2. Image quality (PSNR and SSIM) improvement by planned sensor distortion (PSD) using 3×3 Δ pattern.

The reconstruction principle [12], [13] is illustrated intuitively in Fig. 1(c). Similar to the pseudo multiple sampling (PMS) method [14], [15], PSD increases the image bit precision using multiple neighbouring samples. Each pixel within the 3×3 pixel block defines a unique sub-quantization comparison with the reference for the central pixel (I_5). All the comparison results can be utilized as a spatial 3-bit quantizer according to the pre-defined Δ pattern. Consequently, the I_5 bit depth is extended by 3 bits. More advanced reconstruction algorithms based on Markov random field (MRF) optimization have been used for higher image quality in this brief [13].

In Fig. 2, image quality improvement by 3×3 PSD is verified through simulation on 8-bit test images. Both PSNR and SSIM degrade as the bit depth is reduced. At 3-bit depth, PSD boosts PSNR and SSIM to be more than 32 dB and around 0.9 respectively. It provides sufficient image quality (PSNR>30 dB & SSIM>0.8) for computer vision analysis [11] with the lowest data rate. So 3-bit PSD is chosen for the sensor implementation. Noise will degrade the image quality. To ensure PSNR>30 dB and SSIM>0.8, the overall root mean square noise should be lower than 6 LSB for the 3-bit PSD.

B. Microshift-Guided ADC

The microshift-guided quantization can be implemented either in the digital or analog domain. Applying the microshift before ADC brings the benefits of lower power and smaller area as the ADC quantization levels and readout bandwidth are reduced. Furthermore, employing column-parallel ADCs can achieve higher speed, lower power and larger pixel fill factor. In such case, column fixed-pattern noise (FPN) minimization is required to fulfill the overall noise requirement.

In terms of ADC architectures, single slope (SS) ADC and SAR ADC are two major options due to high energy efficiency and natural compatibility with microshifting [14], [15]. Microshift-guided SAR ADC is adopted for the advantages of lower power and higher speed than the SS type. Although 3-bit ADC is implemented, 8-bit accuracy is designed for high reconstruction performance. To avoid calibration between the microshift and the quantization step as well as power-hungry global voltage buffers, the SAR ADC is extended to 6 bits for 3-bit quantization with 3-bit microshifting. Besides, a 2-bit SS ADC is introduced to form an 8-bit SAR/SS ADC to support normal imaging with low area overhead.

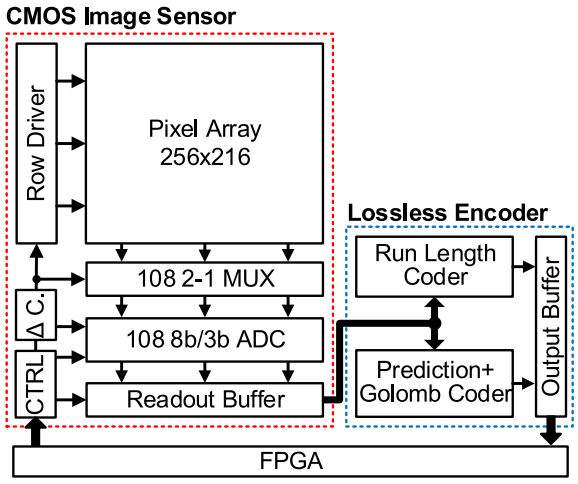

Fig. 3. System block diagram: CMOS image sensor and lossless encoder.

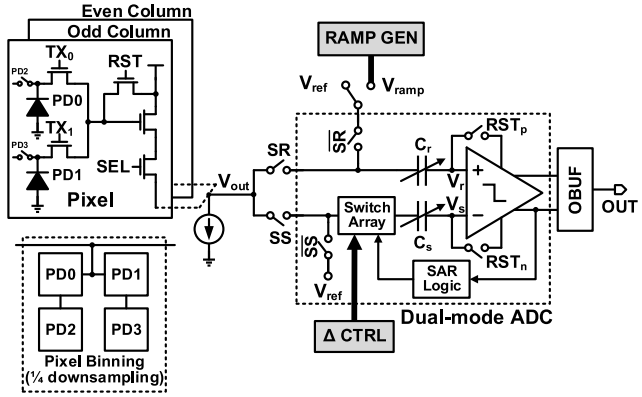

Fig. 4. Pixel architecture and column-parallel circuit.

III. System Architecture and Circuit Implementation

A. System Architecture

An imaging system is designed based on the proposed PSD compression framework in Fig. 1. As shown in Fig. 3, the system consists of a PSD-based CMOS image sensor and a lossless encoder. The image sensor has a 256×216 pixel array, which are quantized by 108 column-parallel dual-mode ADCs through column multiplexors (MUX). The dual-mode ADC can be configured as an 8-bit SAR/SS ADC for normal imaging or a 3-bit microshift-guided SAR ADC for PSD imaging. A global microshift controller (Δ *CTRL*) is introduced to control the local Δ generation on a row-by-row basis. After the microshift-guided quantization, the 3-bit image data are readout to the lossless encoder for further compression based on predictive coding or run length coding. An FPGA controls the whole system and reads back the data for analysis.

B. Circuit Implementation

The pixel architecture and the column-parallel circuit are shown in Fig. 4. Two pixel columns share a dual-mode ADC. A two-pixel shared architecture is employed to increase pixel fill factor. To enable 1/4 spatial downsampling for 4X lower data rate and power consumption, 4-pixel binning is employed using 2 inter-pixel switches, which provides

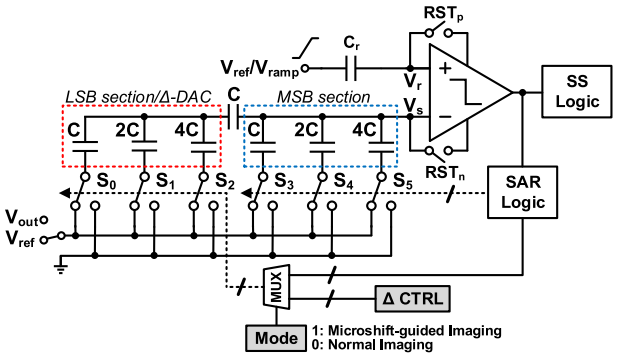

Fig. 5. Dual-mode ADC for 8-bit normal imaging (SAR/SS) and 3-bit microshift-guided imaging (SAR).

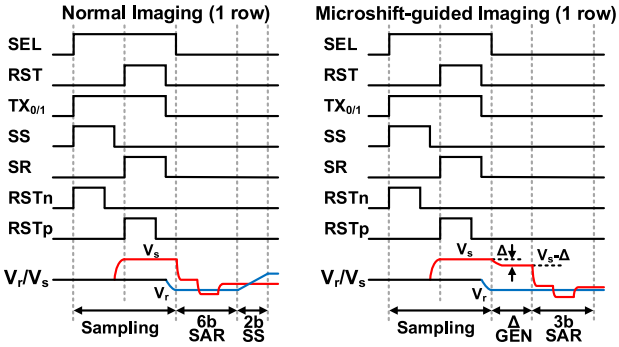

Fig. 6. Timing diagrams for normal imaging and microshift-guided imaging.

higher interpolation image quality than the skipping method. Spatial correlation is guaranteed by minimizing FPN from two aspects. Firstly, reset and signal voltages are double sampled using the same capacitance ($C_s = C_r$) to minimize the pixel mismatch. Secondly, the comparator offset is cancelled during bottom-plate sampling to minimize the ADC mismatch. A two-stage dynamic comparator with input offset cancellation is employed to achieve sub-mV offset with high energy efficiency [16].

The architecture of the dual-mode ADC is shown in Fig. 5. A 6-bit capacitive DAC split by a unit capacitor is implemented for the SAR operation, considering smaller area and higher linearity. The differential non-linearity (DNL) and integral non-linearity (INL) have been designed to be less than 0.5 LSB of 8-bit resolution. During microshift-guided imaging, the MSB section is used for 3-bit quantization while the LSB DAC is controlled by 3-bit global signals $S_{2:0}$ from Δ *CTRL* to generate Δ. Due to the optimized matching of the two sections, no calibration is needed between the Δ and the quantization step. For normal imaging, 6-bit SAR is conducted on the capacitive DAC while 2-bit SS ramp is applied globally through C_r. The hybrid architecture has been proven to have both low power and compact area [9].

C. Operation

The timing diagrams of two imaging modes are shown in Fig. 6. Because neither pinned photodiode nor high supply voltage is employed, charge-shared double sampling [2] is implemented instead of charge-transferred correlated double sampling for both modes. Different from [16], RST_p and RST_n are asynchronous to cater for sequential readout of V_r and V_s.

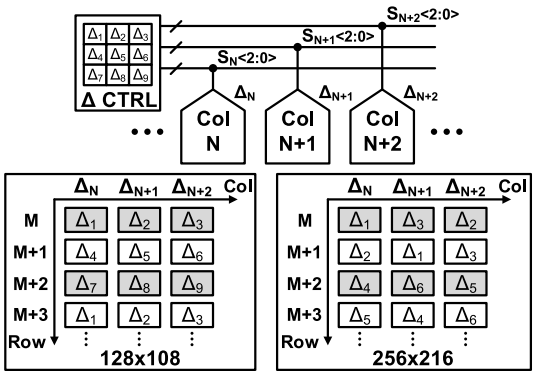

Fig. 7. 3×3 microshift (Δ) pattern generation at 2 imaging resolutions.

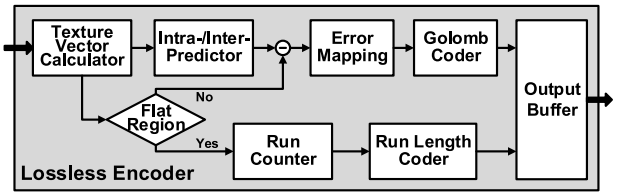

Fig. 8. Lossless encoder block diagram.

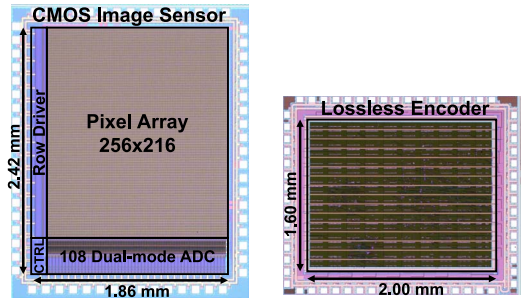

Fig. 9. Chip microphotographs of the prototype CMOS image sensor and lossless encoder.

For normal imaging, 6-bit SAR quantization is processed on V_s followed by 2-bit ramping on V_r. For microshift-guided imaging, Δ is generated before the 3-bit SAR operation. The 3×3 Δ pattern is generated as shown in Fig. 7. The pattern is applied row by row. In each row, 3 adjacent columns are controlled individually through $S_N/S_{N+1}/S_{N+2}$ by Δ *CTRL* to locally generate the planned Δ. As two imaging resolutions are available through column circuit sharing, the Δ sequences are rearranged to meet the locations of corresponding pixels at 256×216 resolution. In our design, the 3-bit pattern is {0, 4, 8; 12, 16, 20; 24, 28, 20} LSB, where a redundant 20 LSB replaces the unavailable 32 LSB with negligible influence.

D. Lossless Encoder

The block diagram of the lossless encoder is shown in Fig. 8. A flat region is judged based on the texture calculation. If a flat region is detected, run length coding is employed. Otherwise, predictive+Golomb coding is used. The selective use of two coding methods allows a higher compression ratio to be 2.4. Thanks to the 3-bit data width, both the processing power and area have been greatly improved for the encoder.

TABLE I
CHIP PERFORMANCE SUMMARY

CMOS Image Sensor				
Supply (V)	1.2 (analog) /0.8 (digital)			
Chip dimension (mm²)	2.42x1.86			
Pixel size (μm²)	7.9x7.9 (46% fill factor)			
Pixel Array	256x216			
Frame rate (fps)	15 (max. 436)			
Conversion gain (μV/e⁻)	7.0			
Sensitivity (V/lux·s)	1.7			
FPN (Dark)	0.87%			
Random noise	0.65%			
Operation mode	Normal		Compression	
ADC architecture	8b SAR/SS		3b Δ-Guided SAR	
Data rate (bpp)	8		3	
Resolution	256x216	128x108	256x216	128x108
PSNR (dB)	43.7	43.6	34.9	33.2
SSIM	0.95	0.97	0.91	0.92
Power (μW@15 fps)	23.5	6.6	14.8	4.3
Energy (pJ/pixel·frame)	28.3	31.8	17.8	20.7
Lossless Encoder				
Supply (V)	1.8 (limited by IO devices)			
Chip dimension (mm²)	1.60x2.00			
Throughput (pixel/s)	100M			
Compression ratio	2.4			
Energy (pJ/pixel)	63.7			
Overall System (compression mode only)				
Date rate (bpp)	1.25			
PSNR (dB)/SSIM	34.9/0.91 (256x216)		33.2/0.92 (128x108)	
Energy (pJ/pixel)	81.5 (256x216)		84.4 (128x108)	

IV. EXPERIMENTAL RESULTS

A prototype system including the CMOS image sensor and the lossless encoder is fabricated in a 0.18-μm standard CMOS process. The microphotographs of two chips are shown in Fig. 9. They are integrated on a printed circuit board (PCB) controlled by an FPGA. The image sensor has dimensions of 2.42×1.86 mm^2, where each column circuit only occupies 370×15.8 μm^2. The area of the encoder is 1.60×2.00 mm^2.

The chip performance is summarized in Table I. The pixel size is 7.9×7.9 μm^2 with a 46% fill factor. The sensor consumes 23.5 μW and 6.6 μW at 15 fps for 256×216 and 128×108 normal imaging respectively. The powers are effectively reduced to 14.8 μW and 4.3 μW respectively by the compression. The reconstruction takes about 0.2 s (256×216) and 0.05 s (128×108) on a typical desktop. With 3 bpp, the reconstructed PSNRs and SSIMs are maintained higher than 33 dB and 0.9 respectively at both resolutions. More than 35% sensor power has been saved by the 62.5% data rate compression. Lower bit depth will save more power but also degrade the image quality. With the lossless encoder, the overall system will maintain the same sensor PSNR/SSIM but further suppress the data rate to be 1.25 bpp at an additional energy cost of 63.7 pJ/pixel (1.8 V). The energy is improvable to 12.6 pJ/pixel (estimation) by scaling 1.8 V down to 0.8 V.

Sample images (256×216) are shown in Fig. 10. The raw microshift-guided image (c) has lower PSNR/SSIM due to the added Δ pattern. However, the reconstructed 8-bit image (d) demonstrates much higher PSNR/SSIM than the 3-bit image without microshifts (b). Performance comparisons with prior compression-based and low-power image sensors are listed in Table II. The proposed sensor accomplishes the best image quality with the highest energy efficiency among all the compression-based image sensors. It can also attain the lowest data rate (0.75 bpp) with 1/4 downsampling. With the encoder, the overall system can achieve 0.31 bpp. Compared with ultra-low-power image sensors, the compression-based sensor achieves the state-of-the-art FoM

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART COMPRESSION-BASED/LOW-POWER IMAGE SENSORS

Reference^	This work		JSSC'14 [9]	JSSC'13 [8]		TCAS-I'16 [10]	JSSC'09 [6]	TCAS-I'13 [7]	JSSC'15 [1]	JSSC'16 [2]
Algorithm	PSD		VPIC	CS		CS+AER	DWT	DPCM+VQ	-	-
Process	0.18 µm		0.18 µm	0.15 µm		0.18 µm	0.35 µm	0.35 µm	65 nm	0.11 µm
Processing level	Column		Column	Column		Pixel	Column	Pixel	-	-
Supply (V)	1.2/0.8		3.3/1.8	3.3/2.0/1.8		3.3/1.8	3.3	3.3	0.5	0.9
Area (mm^2)	2.42x1.86		2.16x1.36	2.9x3.5		1.13x0.85	4.4x2.9	1.61x1.28	0.73x0.95	4.04x4.53
Pixel architecture	4T APS		3T APS	4T APS		22T AER	7T APS	I-APS+PE	5T DPS	4T APS
Pixel pitch (µm) & FF	7.9 (46%)		1.85 (13%)	5.5 (-)		15 (32%)	15.4 (28%)	37.5 (7%)	4 (57%)	5 (-)
Resolution	256x216		816x640	256x256		48x72	128x128	32x32	128x128	340x260
Frame rate (fps)	15 (max.436)		111	480	1920	23	30	125	32	15
Compression ratio	2.7	10.7*	8	4	16	5.35	8	8.5	1	1
Data rate (bpp)	3	0.75*	1	3	0.75	2.24	1	0.94	10	8
PSNR (dB)	**34.9**	**29.2***	20	35.7	32.5	23	15	18	27	50
SSIM	**0.91**	**0.83***	-	0.87	0.80	0.84	-	-	-	-
Power (µW)	14.8	4.3*	690	93600	96200	1560	26200	37000	8.8	45.5
FoM# (pJ/pixel·frame)	**17.8**	**5.2***	12	2975	765	19625	53304	289062	17	34.3

^ The lossless encoder is not included as other designs do not implement entropy encoders. # FoM=Power/(Resolution · Frame rate).
* For PSD+¼ downsampling (256x216→128x108), the performance is measured against 256x216 imaging through 4X cubic interpolation.

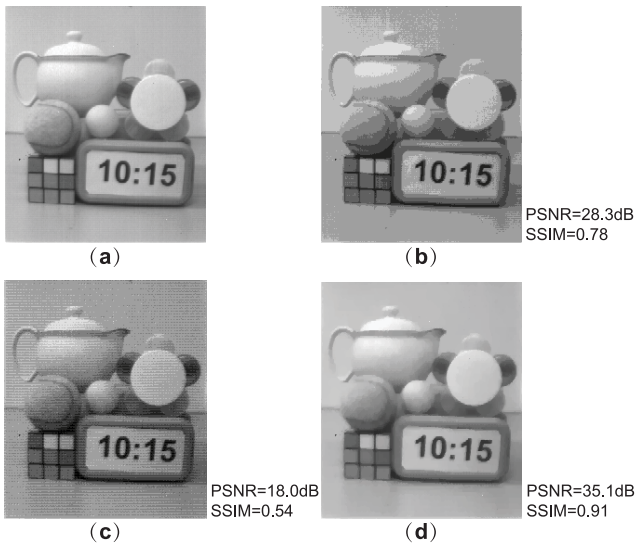

Fig. 10. Sample images (256×216): (a) 8-bit normal image; (b) 3-bit image without microshifts; (c) 3-bit microshift-guided image; (d) Reconstructed 8-bit image from (c).

with the lowest data rate while maintaining sufficient image quality for vision analysis. The greatly reduced bandwidth could benefit much more for data transfer, processing and transmission.

V. CONCLUSION

A CMOS image sensor with PSD-based compression is proposed for low-power wireless imaging applications. It features low data rate and high energy efficiency with satisfactory image quality. A microshift-guided SAR ADC based on a 3×3 PSD Δ pattern is designed to suppress the image bit depth down to 3 bits while ensuring high reconstruction image quality (PSNR>33 dB and SSIM>0.9). With 1/4 downsampling and lossless encoding, the overall data rate can be compressed by more than 96%. State-of-the-art energy efficiency has also been accomplished by the proposed compression-based image sensor. Integrated with a lossless encoder, the overall imaging system only consumes a few μJ/frame, providing a practical solution for energy-constrained wireless sensor networks.

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