A 3.15-mW +16.0-dBm IIP3 22-dB CG Inductively Source Degenerated Balun-LNA Mixer With Integrated Transformer-Based Gate Inductor and IM2 Injection Technique

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***Abstract*— This article proposes two linearization techniques in improving the third-order input intercept point (IIP3) of a balun-low-noise amplifier (LNA) mixer. First, the intrinsic third-order intermodulation (IM3) product of the inductively source degenerated (ISD) transconductor from the second-order derivative transconductance component (g_m'') is reduced by tailoring toward the optimum biasing point at the moderate-inversion region. Second, the generated IM3 current by the first-order derivative transconductance (g_m') due to the interaction with the feedback component in the ISD transconductor is attenuated by second-harmonic injection via the bulk of the ISD transconductor. Furthermore, a transformer-based gate inductor and a transformer-based balun are applied to improve the input impedance matching and produce a balanced differential input signal. Measured results in 0.13-μm CMOS show a high IIP3 of +16 dBm and a conversion gain (CG) of 22 dB at 2.4 GHz. The double-sideband (DSB) noise figure (NF) is 7.2 dB, and the power consumption is 3.15 mW at 1.2 V.**

***Index Terms*— Balun-low-noise amplifier (LNA) mixer, CMOS, high linearity, inductively source degeneration transconductor, low-power, second-order intermodulation (IM2) injection, third-order input intercept point (IIP3), Volterra series.**

I. Introduction

HIGHLY linear front-end circuits are greatly desired for wireless receivers to improve the dynamic range. Yet, intermodulation distortions caused by the nonlinear transconductor current limit the linearity of the front-end circuit in CMOS technologies. In addition to the inherent nonlinear effect, the downscaling of CMOS further exacerbates the linearity of the circuit due to lower voltage headroom and high-field mobility. Thus, it is essential to develop effective circuit techniques that aid linearity enhancement without jeopardizing other preferred performances, such as low noise, high conversion gain (CG), and low power consumption [1].

An inductively source degenerated (ISD) transconductor, as shown in Fig. 1(a), is commonly used in both low-noise amplifier (LNA) and mixer design [2], [3]. However, the linearity performance is unsatisfactory as the intrinsic second-order distortion current at the transistor's source is mixed with the fundamental input signal by the feedback mechanism through the degeneration source inductor, thereby generating third-order intermodulation (IM3) distortion.

In fact, there are more than one feedback path existing in an ISD transconductor (i.e., gate–drain feedback through gate–drain capacitance and gate-input feedback through input impedance matching network), as shown in Fig. 1(b). The overall linearity can be improved by terminating the second-order nonlinearity in the feedback loop to suppress the generated IM3 component. Harmonic termination [4], [5] was proposed in realizing it, where the integrated *LC* network creates a low impedance path to the supply/ground for the

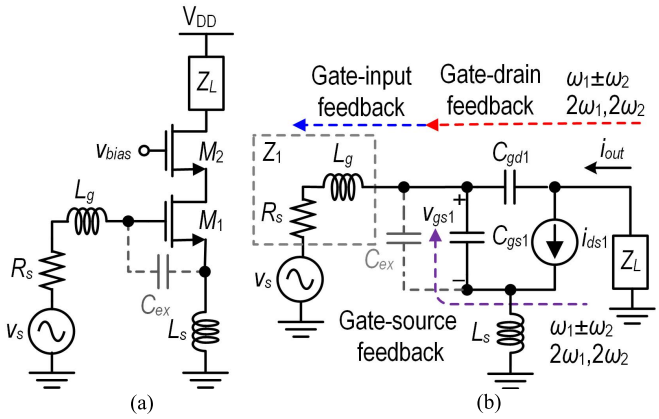

Fig. 1. (a) Schematic and (b) small-signal equivalent circuit of the ISD common-source transconductor with feedback path.

Manuscript received June 3, 2019; revised September 5, 2019; accepted October 18, 2019. Date of publication November 22, 2019; date of current version February 25, 2020. This work was supported in part by the Macao Science and Technology Development Fund through the SKL Fund, in part by the University of Macau under Grant MYRG2017-00185-AMSV, and in part by the Motorola Solution Foundation under Grant IF017-2016. *(Corresponding author: Harikrishnan Ramiah.)*

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Digital Object Identifier 10.1109/TVLSI.2019.2950961

second-order frequencies ($\Delta\omega$, 2ω). Despite the suppression in second-order distortion interaction, the required passive *LC* components are bulky, which incur noise and restrict improvements in linearity, due to the limited *Q*-factor of the on-chip inductors.

Another technique is the modified derivative superposition [6] that uses two transistors operating in different regions to relax the source–gate feedback effect. This involves a main transistor M_{main} operating in the saturation region and an auxiliary transistor M_{aux} operating in the subthreshold region to create a second-order derivative transconductance $g''_{m,\text{aux}}$ to cancel the resultant vectors g''_m and g'_m of M_{main}. When M_{aux} is biased in the subthreshold region, additional noise is induced and the input impedance matching is degraded as both transistor gates are shorted together at the input. Similarly, in the predistortion technique [7], nonlinearity improvement is achieved at the input of the common gate transistor with an auxiliary transistor operating in the weak inversion region. Postdistortion technique has been implemented in [8]–[10] where the auxiliary transistor is connected at the drain of the main transistor instead of directly connecting to the gate. However, this technique improves the nonlinearity with the penalty of gain reduction.

An IM2 injection technique has been proposed in recent years, attenuating the total IM3 current by injecting a phase-inverted IM2 signal into the differential transconductor and producing an interaction term in the IM3 current. References [11]–[15] adopted a squaring circuit to generate the IM2 signal. In [13], the IM2 signal is injected at the gate of the mixer's input transistor; thus, the second-order component potentially leaks through the gate-input feedback to the former block such as the LNA, resulting in performance degradation for the entire receiver. This problem can be mitigated by injecting the IM2 signal into bulk of the input transistor [11] or tail transistor of the differential amplifier [15] with commendable output third-order input intercept point (IIP3) improvement. In [15], the conventional capacitor in IM2 circuit was replaced with a large varactor to increase the two-tone spacing at the cost of an increase in active chip area consumption. However, the discussion in both works is limited to the linearity improvement of the circuit only. On the other hand, the cascaded LNA and mixer configuration in [14] achieves an IIP3 of +10.6 dBm at the penalty of higher power consumption. In contrary to the cascaded architecture, the merging of the LNA and mixer through the current reuse structure is preferred to reduce total power consumption [16].

In this article, we introduce the IM2 injection and optimum bias voltage technique into the ISD transconductance-based LNA mixer to improve the linearity and to maintain the CG at low power consumption. Also, a passive balun and transformer-based gate inductor are adopted at the input of the transconductor to aid input impedance matching and to create high fundamental rejection signal for the IM2 injection circuit via its balanced feature. This architecture also achieves a solution to the gate-input feedback through the transformer-based input impedance matching network.

This article is organized as follows. In Section II, we investigate the ISD transconductor and discuss the existing linearization technique. Section III presents the proposed linearity enhancement techniques that effectively improve the IIP3 of the ISD transconductor. The measurement results are presented in Section IV. Finally, Section V concludes this article.

II. Conventional ISD Transconductor Linearity Optimization

The simplified equivalent circuit of the conventional ISD transconductor is shown in Fig. 1(b) and is used to calculate the IIP3. The output current of the input transistor, M_1, can be expressed as a harmonic function of the input voltage v_s using the following Volterra series expression:

$$i_{out} = G_1(\omega) \circ v_s + G_2(\omega_1, \omega_2) \circ v_s^2 + G_3(\omega_1, \omega_2, \omega_3) \circ v_s^3 \tag{1}$$

where $\circ$ is the Volterra series operator. $G_1(\omega)$, $G_2(\omega_1, \omega_2)$, and $G_3(\omega_1, \omega_2, \omega_3)$ are models representing the first-, second-, and third-order transconductance of M_1, respectively. Similar to the expansion presented in [17] with the inclusion of linear conductance, g_{ds1} while neglecting distortion contribution from the cascode transistor M_2, the IIP3 expression of the ISD common-source stage by using the Volterra series can be expressed as follows:

$$\text{IIP3}(\pm\omega_1, \pm\omega_1, \pm\omega_2) = \frac{1}{6R_s}\left|\frac{G_1(\omega_1)}{G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2)}\right|. \tag{2}$$

The first- and third-order Volterra kernels are given, respectively, by

$$\begin{aligned} &G_1(\omega) \\ &= T_1(\omega) \\ &\quad \times \left\{\frac{g_{m1}(1 - Y_{\text{gd1}}(\omega)Z_s(\omega)) - g_{\text{ds1}}c(\omega)Z_s(\omega) - b(\omega)Y_{\text{gd1}}(\omega)}{g_{\text{ds1}}(Z_s(\omega) + Z_L(\omega)) + a(\omega)}\right\} \end{aligned} \tag{3}$$

$$\begin{aligned} &G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2) \\ &= T_1^2(\pm\omega_1) \cdot T_1(\mp\omega_2) \\ &\quad \times \left\{\frac{1}{g_{m1} + g(\pm 2\omega_1 \mp \omega_2)} \cdot \frac{\alpha(\pm 2\omega_1 \mp \omega_2)}{Z_x(\pm 2\omega_1 \mp \omega_2)} \right. \\ &\qquad \left. \cdot \varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1)\right\} \end{aligned} \tag{4}$$

in which

$$T_1(\omega) = \frac{1}{g_{m1} + g(\omega)} \times \frac{g_{\text{ds1}}(Z_s(\omega) + Z_L(\omega)) + a(\omega)}{Z_x(\omega)} \tag{5}$$

$$\begin{aligned} &\varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1) \\ &\quad = g''_{m1} - \frac{2}{3}\left(g'_{m1}\right)^2 \\ &\qquad \cdot \left(\frac{1}{g_{m1} + g(\pm\omega_1 \mp \omega_2)} + \frac{1}{g_{m1} + g(\pm 2\omega_1)}\right) \end{aligned} \tag{6}$$

$$g(\omega) = \frac{1}{Z_x(\omega)} \times \left\{\begin{matrix} g_{\text{ds1}}(Z_x(\omega) + Z_y(\omega)) + Y_{\text{gs1}}(\omega)Z_x(\omega) \\ + a(\omega) + c(\omega)Z_1(\omega) \end{matrix}\right\} \tag{7}$$

$$\alpha(\omega) = b(\omega) + c(\omega)Z_1(\omega) \tag{8}$$

$$Z_x(\omega) = Z_s(\omega) + Y_{\text{gd1}}(\omega)Z_T(\omega) \tag{9}$$

$$Z_y(\omega) = Z_L(\omega) + Y_{\text{gs1}}(\omega)Z_T(\omega) \tag{10}$$

$$Z_T(\omega) = Z_1(\omega)Z_L(\omega) + Z_1(\omega)Z_s(\omega) + Z_L(\omega)Z_s(\omega). \tag{11}$$

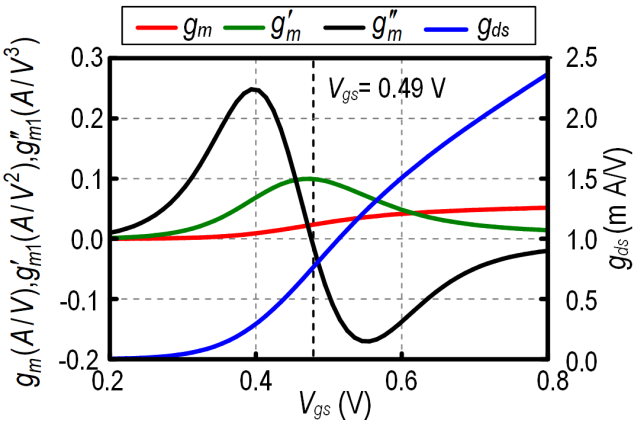

Fig. 2. g_m, g_{ds}, g'_m, and g''_m common-source 80/0.13-μm nMOS transistor. Threshold voltage is about 0.40 V for this device.

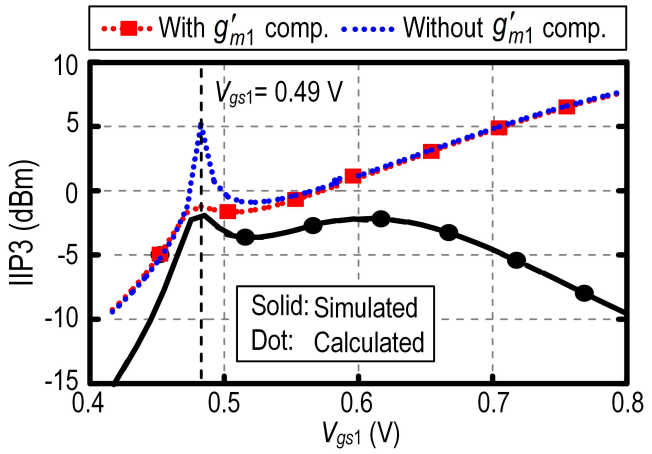

Fig. 3. Simulated and calculated of IIP3 for different values of $V_{\rm gs1}$.

$a = (1 + Y_{\rm gd1}Z_L)$, $b = (1 + Y_{\rm gs1}Z_s)$, and $c = (Y_{\rm gs1} + Y_{\rm gd1})$. $Y_{\rm gs1}$ and $Y_{\rm gd1}$ are the parasitic admittances at the gate–source and gate–drain of M_1, respectively. Z_s is the source node impedance of M_1 which is denoted as $j\omega L_s$. $T_1(j\omega)$ is the linear transfer function of gate–source voltage, $v_{\rm gs1}$ over v_s.

$\varepsilon(\pm\omega_1 \mp \omega_2, \pm 2\omega_1)$ shows the effect of the output current nonlinearities on IM3 distortion. The second term in (6) describes the second-order nonlinearity of the input transistor, g'_{m1} contributing IMD3 due to the multiple harmonic feedback interaction triggered in the circuit mainly by degenerated source inductor and gate–drain capacitances. This causes a degradation in IIP3 even at the optimum gate biasing point, where the third-order nonlinear coefficient g''_{m1} of the input transistor is zero. As can be inferred from Fig. 2, when g''_{m1} is minimized to 0 at $V_{\rm gs} = 0.49$ V, g'_{m1} shows a peak value, and thus, the second term in (6) dominates the nonlinearity of the circuit at this bias point. Fig. 3 explains this phenomenon, where the analytical IIP3 plot shows a high peak without the g'_{m1} component.

However, the possibility in improving linearity of the ISD transconductor without degrading the noise figure (NF) performance is established if a small device of input transistor is selected at a relatively high overdrive voltage $V_{\rm gsT}(\approx V_{\rm gs} - V_{\rm th})$. As discussed in [18], the capacitor $C_{\rm ex}$ integrated in reducing the input transistor size in minimizing the feedback effect caused by $C_{\rm gd}$ and $C_{\rm ds}$, also reducing the transconductance distortions due to large $V_{\rm gsT}$. This is shown in Fig. 3, where the analytical IIP3 plot of the ISD transconductor improves when $V_{\rm gsT}$ increases at the cost of increased power consumption. However, note that the simulated IIP3 plot of the cascoded ISD transconductor is limited and degraded drastically when $V_{\rm gsT}(>200$ mV). This is because when the input cascoded ISD transistor biased in strong inversion region, the drain voltage plays a significant role due to the higher gain of the transconductor compared to the one biased in the moderate-inversion region. Despite the reduction in transconductance distortion as $V_{\rm gsT}$ is increased, the transistor M_1 tends to be pushed into the linear region of operation at high $V_{\rm gsT}$ at low supply voltage resulting in a high output conductance nonlinearity ($g'_{\rm ds1}$, $g''_{\rm ds1}$) and cross-modulation nonlinearity, and hence, (4) becomes invalid. Besides that, the distortion contribution from the cascoded transistor M_2 becomes dominant, as the output resistance of M_1 is low in advanced CMOS process [18].

In this article, to effectively enhance the linearity of the ISD transconductor at low power consumption, the input transistor is biased at the moderate-inversion region by setting g''_{m1} to zero, while the third-order nonlinearity distortion current that arises by the feedback effect is suppressed by injecting an opposite sign of the second-order intermodulation (IM2) current into the bulk of the input transistor. In addition, the second-order injection technique is plausible because it does not degrade the gain and contribute noise as it works in common-mode frequencies and consumes a negligible amount of current.

III. Proposed High Linearity ISD Balun-LNA Mixer

Fig. 4 shows the proposed balun-LNA mixer, where the transistors M_1 and M_2 act as the ISD transconductor with a source inductor L_s, while the transistors M_5 and M_8 form the switching pair for the differential double-balanced mixer. An IM2 injection circuit that consists of $M_{3,4}$, R_l, and C_1, is introduced into the ISD transconductor to improve the linearity by injecting the IM2 at the bulk of $M_{1,2}$ through the ac-coupling capacitor $C_{\rm ac3}$. Resistor R_B bias the bulk terminal of $M_{1,2}$ with zero potential as it is shorted to ground. The current-bleeding transistor $M_{9,10}$ enhances the CG of the LNA mixer by splitting the current flow into the load, R_L. A simple 1:1 transformer-based balun $T_{\rm TB1,2}$ in an unbalance-to-balanced configuration with a center tap is used at the input of RF and LO ports for input impedance matching and single ended to differential conversion. Additionally, transformer $T_{\rm TI}$ is added between $T_{\rm TB1}$ and transistor $M_{1,2}$ to provide the necessary series gate inductance for the input impedance matching and high common-mode rejection for the IM2 circuit with reduced physical area consumption compared to the conventional practice in integrating an individual gate inductor. The design parameters of the proposed balun-LNA mixer are summarized in Table I.

Sections III-A–III-C present a detailed analysis of the input impedance matching, CG, and noise on the proposed ISD

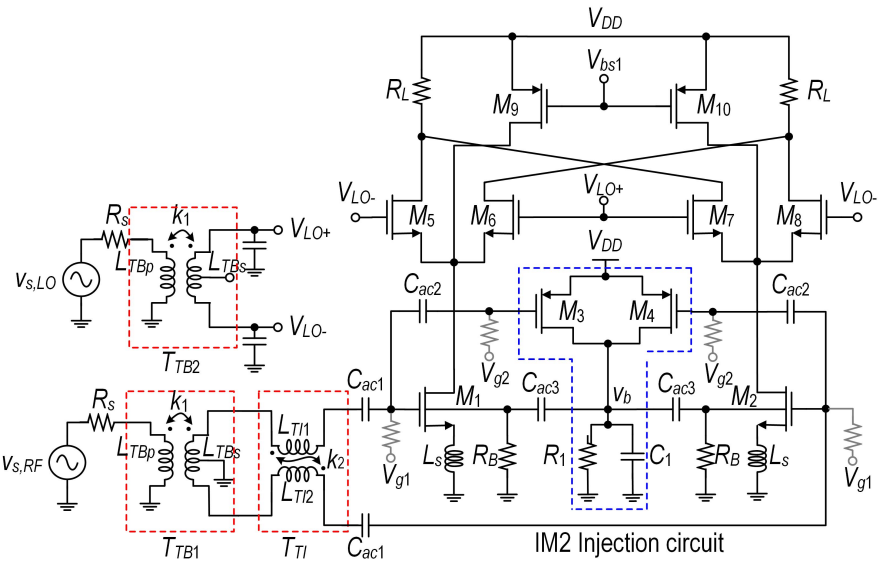

Fig. 4. Circuit schematic of the proposed modified ISD balun-LNA mixer, including an on-chip transformer-based balun and a transformer-based inductor at the input transconductance stage without the output IF buffer and biasing circuits. The three transformers' impedance ratio from the primary to the secondary winding is unity.

TABLE I
CIRCUIT PARAMETERS OF THE PROPOSED BALUN-LNA MIXER

Parameter	T_{TB}+T_{TI}+IM2 Injection Circuit
$(W/L)_{1,2}$ (μm/μm)	60/0.13
$(W/L)_{3,4}$ (μm/μm)	60/0.13
$(W/L)_{5\text{-}8}$ (μm/μm)	40/0.13
$(W/L)_{9,10}$ (μm/μm)	70/0.13
k_1	0.78
k_2	0.76
Q_{TBp}/Q_{TBs}	11.0/9.8
Q_{TI}	10.3
R_L (Ω)	500
L_s (nH)	0.7
R_1 (Ω)	1850
C_1 (pF)	2.5
C_L (pF)	1.5
L_{TBp}/L_{TBs} (nH)	3.26/3.28
L_{TI1}/L_{TI2} (nH)	4.22/4.22
P_{DC} (mW)	1.2V@3.15 mW

topology by considering the transformer losses due to magnetic flux leakage. From Sections III-A–III-C, the bulk effect of the input transistor is neglected as the output of the squaring circuit contains only even-order components and the fundamental signal is canceled at V_b. On the contrary, the linearity computation in Section III-D incorporates this bulk effect to obtain a comprehensive analysis into the nonlinearity of the proposed transconductor.

A. Input Impedance Matching

Fig. 5(a) shows the small-signal equivalent circuit of the input differential transconductance stage, which consists of two transformers $T_{\rm TB1}$ and $T_{\rm TI}$ where the transformer models are adopted from [19] and [20], respectively. The parasitic resistance of $T_{\rm TB1}$ and $T_{\rm TI}$ is neglected to simplify the analysis. $L_{\rm TBp}$ and $L_{\rm TBs}$ are the primary and secondary inductances of $T_{\rm TB1}$, respectively, and $n_1 = (L_{\rm TBs}/L_{\rm TBp})^{1/2}$ represents the

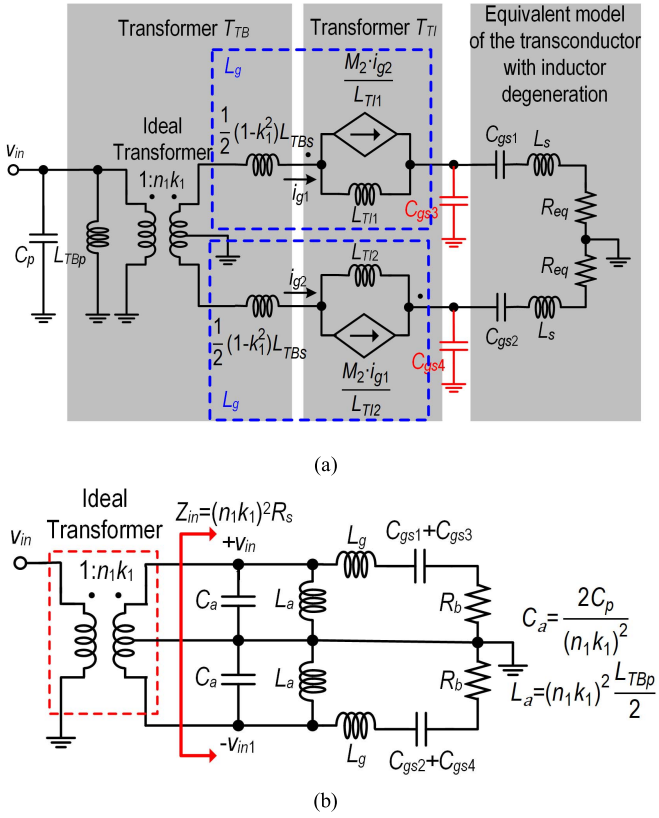

Fig. 5. Schematic showing the proposed differential ISD transconductor with (a) transformer equivalent model of transformer-based balun $T_{\rm TB1}$ and transformer-based gate inductor $T_{\rm TI}$ while including input parasitic capacitance. (b) More compact equivalent circuit model of input network for calculating the input impedance by series of parallel–series conversion.

turn ratio. $L_{\rm TI1}$ and $L_{\rm TI2}$ are the primary and secondary winding inductances of $T_{\rm TI}$, respectively, with a mutual inductance, M_2. The parameter k_1 represents the coupling coefficient of $T_{\rm TB1}$. The capacitance C_p represents both parasitic capacitance of the primary side of $T_{\rm TB1}$ and bondpads. The parasitic gate–

source capacitance $C_{\mathrm{gs3,4}}$ of the squaring device is accounted in as it is directly connected to the input transistor.

T_{TI} is a 1:1 transformer, and hence, it could be related as $L_{\mathrm{TI1}} = L_{\mathrm{TI2}}$ and $i_{g1} = i_{g2}$. In the differential mode, the effective inductance of the primary and secondary coils of T_{TI} can be represented as $L_{\mathrm{eff}} = L_{\mathrm{TI}}(1 + k_2)$, where $k_2 = M_2/(L_{\mathrm{TI1}}L_{\mathrm{TI2}})^{1/2}$ is the coupling coefficient of T_{TI}. The input network is simplified further as shown in Fig. 5(b) by transferring the primary impedance of T_{TB1} referred to the secondary of an ideal transformer. The variable L_g is used to represent the total series inductance of $0.5(1 - k_1^2)L_{\mathrm{TBs}} + L_{\mathrm{eff}}$. At the resonant frequency, the parallel capacitor $C_{\mathrm{gs3,4}}$ in Fig. 5(a) is transformed into a series representation by applying a parallel-to-series impedance transformation [21]. Then, the resulting real impedance of the ISD amplifier is reduced to $R_b \approx \eta^2 R_{eq}$, where $\eta = C_{\mathrm{gs1}}/(C_{\mathrm{gs1}} + C_{\mathrm{gs3}})$ and $R_{eq} = \omega_T L_s + R_g$. R_{g} is the gate resistance of the input transistor M_1. Interestingly, the circuit transformation forms a parallel-to-series input network.

At resonant frequencies

$$\omega_{o1} L_a = \frac{1}{\omega_{o1} C_a} \tag{12}$$

$$\omega_{o2} L_g = \frac{1}{\omega_{o2} C_t} \tag{13}$$

where ω_{o1} and ω_{o2} are parallel and series LC resonant frequencies and $C_t = C_{\mathrm{gs1}} + C_{\mathrm{gs3}}$. The ideal input impedance matching condition is achieved by selecting proper inductor and capacitor values to ensure the parallel and series LC networks resonate at the same frequency ($\omega_{o1} = \omega_{o2} = \omega_o$), i.e., $L_a C_a = L_g C_t$, and the real impedance of $Z_{\mathrm{in}} \approx n_1^2 k_1^2 R_s$. Subsequently, the real input differential impedance looking into the secondary winding becomes

$$\begin{aligned} Z_{\mathrm{in}}(\omega_o) &= n_1^2 k_1^2 R_s \\ &= 2\eta^2 R_{eq} = 2\eta^2(\omega_T L_s + R_g) \end{aligned} \tag{14}$$

where $\omega_T = g_{m1}/C_{\mathrm{gs1}}$. If the parasitic resistance is neglected, the real part of Z_{in} is reduced by the term η in comparison to the typical power-constrained ISD amplifier for a given value of L_s, g_{m1}, and transistor size. This means that the ratio of T_{TB1} is limited by C_{gs3}. An additional inductance is adopted via the transformer-based gate inductor, as the inductance T_{TB1} is insufficient to resonate at 2.4 GHz.

In reference to (13), a smaller gate inductance L_{g} is required for series resonance at a given input device size and operating frequency due to C_{gs3}. Also, the transformer coupling effect increases the effective inductance of each side of T_{TI} by a factor of $(1+k_2)$ in a differential input network. This suggests that the physical area can be reduced further while retaining the desired inductance for input impedance matching. As a result, the parasitic capacitance that is dependent on the length and size of the winding metal trace is reduced, consequently improving the circuit performance compared to the individual inductors. Similarly, higher quality factor and self-resonant frequency can be achieved compared to individual inductors [20].

Note that the parallel-to-series transformation of $C_{\mathrm{gs3,4}}$ in Fig. 5(b) is only valid at the resonant frequency. Since both the parallel and series tank resonates at the same frequency of ω_o, the equivalent circuit transformation is valid.

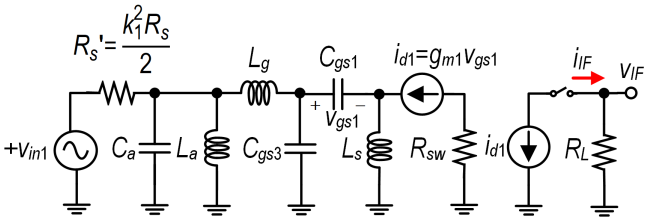

Fig. 6. Half-circuit small-signal representation of the proposed balun-LNA mixer.

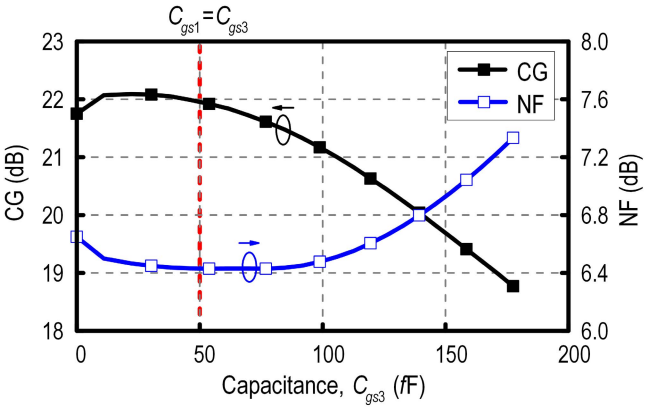

Fig. 7. Simulated CG and NF of the proposed balun-LNA mixer with different transistor size of $M_{3,4}$, to demonstrate its effects when $C_{\mathrm{gs1}} \approx 50$ fF.

B. Conversion Gain and Balanced Input Signal Analysis

Fig. 6 shows the half-circuit small-signal model of the transconductance stage where R_{sw} represents the resistance at the switching transistor's source. At input impedance matching condition, neglecting the parasitic resistance and adopting $(\omega_T/\omega_o) \gg 1$, the voltage CG of the LNA mixer, A_v, can be expressed as

$$A_v = \frac{2}{\pi}\frac{R_L}{\omega_o L_s} \cdot \left| \frac{1}{1 - \omega_o^2 C_{\mathrm{gs3}} L_g + j\omega_o C_{\mathrm{gs3}} R_s'} \right|. \tag{15}$$

The CG of the LNA mixer at the resonant frequency is relatively independent of the transconductance $g_{m1,2}$. Thus, the CG performance of the proposed circuit is relaxed by the optimum biasing point technique.

The injected IM2 would cause gain degradation through the interaction with the fundamental signal in the main path; however, the generated IM3 is at the same order of the intrinsic IM3 at the main path [14]. Thus, the CG is effectively unchanged by the proposed linearization techniques. Alternately, the parasitic capacitance from the transistor $M_{3,4}$ would not deteriorate the CG performance of the circuit. For a 1:1 impedance transformer, C_{gs3} is designed to be equal or smaller than C_{gs1} for the purpose of input impedance matching in (14), thus conserving the CG of the LNA mixer, evidently observed in Fig. 7. In conclusion, a lower impedance transformation and an optimum device dimension of $M_{3,4}$ are required to maintain the CG.

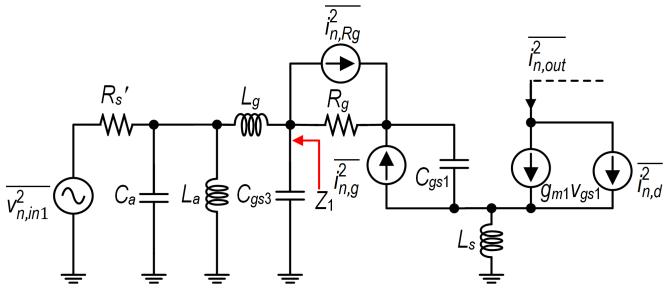

Fig. 8. Noise equivalent half circuit of the input transconductance stage.

Some gain and phase imbalances of an on-chip or off-chip transformer-balun are unavoidable due to its imperfection and asymmetric parasitic capacitance interaction with the internal circuit elements. The integration of inductor-based transformer between the output differential terminals of the balun creates a mutual inductance between the differential terminals so that a well-balanced input signal is generated and to ensure that the squaring circuit has high common-mode rejection [22]. This high common-mode rejection allows the NF of the main transconductance stage to be well isolated from the noise generated from the squaring circuit.

C. Noise Figure Analysis

Fig. 8 shows the half circuit of the transconductance stage with the transformer input network to compute the NF. The noise contribution from IM2 injection circuit is neglected as the injected signal only contains common-mode components, and the capacitance $C_{\mathrm{gs3,4}}$ is included as it is directly connected to the gate of the input transistor $M_{1,2}$. The parallel LC network, i.e., $(1/sC_a)//sL_a$ is an open circuit at the desired operating frequency for maximum power transfer, and hence, it contributes minimum noise to the circuitry.

When $C_{\mathrm{gs3}} = 0$, the noise factor (F) of the single transconductance stage at ω_{o} is given as [23]

$$F = 1 + \frac{R_g}{R_{eq}} + \frac{\delta\alpha}{5}\frac{1}{g_{m1}R_{eq}} + \frac{\gamma}{\alpha}g_{m1}R_{eq}\left(\frac{\omega_T}{\omega_o}\right)^2 \cdot\left(1 + \frac{\delta\alpha^2}{5\gamma} - 2\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \quad (16)$$

where α is the ratio of device transconductance to zero-bias drain-to-source conductance, δ is the coefficient of drain noise, γ is the coefficient of gate noise, and c is a correlation coefficient of the gate-induced noise current and the drain noise current. In the presence of C_{gs3}, the noise factor in (16) can be rewritten by simply substituting the resistance R_{eq} with $R_s/2\eta^2$ [21] and assuming k_1 is equal to 1, that is,

$$F = 1 + 2\frac{R_g\eta^2}{R_s} + \frac{\delta\alpha}{5}\frac{2\eta^2}{g_{m1}R_s} + \frac{\gamma}{\alpha}\frac{g_{m1}R_s}{2\eta^2}\left(\frac{\omega_o}{\omega_T}\right)^2 \cdot\left(1 + \frac{\delta\alpha^2}{5\gamma} - 2\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right). \quad (17)$$

As shown in Fig. 7, the NF increases when the device size of M_3 is increased, where the last term in (17) becomes dominant as the factor η is inversely proportional. This term

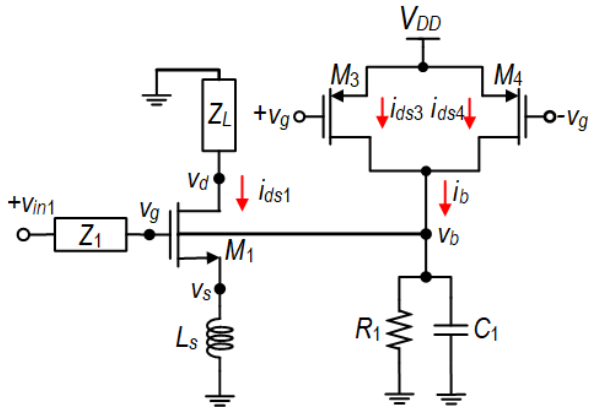

Fig. 9. Thevenin's equivalent half circuit of a combined inductively degenerated common-source transconductance stage and IM2 injection.

can be reduced by increasing ω_T through either increasing the aspect ratio or the gate biasing of the input transistor $M_{1,2}$. Unfortunately, a large aspect ratio leads to large C_{gs1}, alternately an increase in the gate biasing effects the sweet spot-induced linearity. However, the drop in the fourth term is partially relaxed by a lower turn ratio of the transformer T_{TB}, which is reflected by the factor of 1/2. Furthermore, in this design, C_{gs3} is approximated to be equal to the parasitic capacitance C_{gs1}, and thus, the second and third terms can be reduced by half compared to the conventional notation described in (16).

D. Linearity Analysis

As discussed earlier, the linearity performance of the ISD transconductance stage is limited by two mechanisms: the intrinsic third-order nonlinearity term, g''_{m1} in the main path, and the second-order nonlinear component, g'_{m1} interaction in a feedback. If the second-order nonlinear signal IM2 is injected into the bulk terminal of the input transistors, additional IM3 components will appear at the output of the ISD transconductor. This additional IM3 term originating from g'_{mb1} and g'_{m3} by the interaction created between the bulk and source terminals, with an opposite sign and the same magnitude, cancels the indirectly generated IM3 signal in the main path due to the second-order interaction.

The IM2 injection signal is externally generated based on a simple squaring circuit M_3 and M_4, as shown in Fig. 9. Z_1 is the source impedance looking into the left side of gate terminal M_1. To understand the proposed linearization technique in ISD transconductor, a two-tone input signal with equal amplitude is injected for the linearity verification. As both drains of M_3 and M_4 are shorted, the fundamental and odd-order distortion components are canceled with only even-order components present at node v_{b}. The injected IM2 voltage is mixed with the fundamental input signal to generate new third-order intermodulation, IM3 term at $2\omega_1 - \omega_2$ that cancels out the generated IM3 distortion component due to the gate–source and gate–drain feedbacks.

As the signal is applied at the bulk terminal of the transistor $M_{1,2}$, the body effect is taken into consideration, while the nonlinear output conductance and cross-modulation terms

among the nonlinearity components are neglected. Additionally, the back bias of M_3 and M_4 is ignored as both bulk terminals are tied to the source. Thus, the small-signal drain current of the transistors can be expressed by a Taylor series expansion as follows:

$$\begin{aligned} & i_{\mathrm{ds1}}(v_{\mathrm{gs1}}, v_{\mathrm{ds1}}, v_{bs1}) \\ &= g_{m1}v_{\mathrm{gs1}} + g_{\mathrm{ds1}}v_{\mathrm{ds1}} + g_{m\mathrm{b1}}v_{bs1} + g'_{m1}v_{\mathrm{gs1}}^2 - g'_{m\mathrm{b1}}v_{bs1}^2 \\ &\quad + g''_{m1}v_{\mathrm{gs1}}^3 + g''_{m\mathrm{b1}}v_{bs1}^3 + \cdots \\ &= g_{m1}(v_g - v_s) + g_{\mathrm{ds1}}(v_d - v_s) + g_{m\mathrm{b1}}(v_b - v_s) \\ &\quad + g'_{m1}(v_g - v_s)^2 - g'_{m\mathrm{b1}}(v_b - v_s)^2 + g''_{m1}(v_g - v_s)^3 \\ &\quad + g''_{m\mathrm{b1}}(v_b - v_s)^3 \end{aligned} \tag{18}$$

$$\begin{aligned} & i_{\mathrm{ds3}}(v_{sg3}) \\ &= g_{m3}v_{sg3} + g'_{m3}v_{sg3}^2 + g''_{m3}v_{sg3}^3 \\ &= -g_{m3}v_g + g'_{m3}v_g^2 - g''_{m3}v_g^3 \end{aligned} \tag{19}$$

$$\begin{aligned} & i_{\mathrm{ds4}}(v_{sg4}) \\ &= g_{m4}v_{sg4} + g'_{m4}v_{sg4}^2 + g''_{m4}v_{sg4}^3 \\ &= g_{m4}v_g + g'_{m4}v_g^2 + g''_{m4}v_g^3 \end{aligned} \tag{20}$$

where $v_{\mathrm{gs}n}$ and $v_{\mathrm{bs}n}$ are the voltages applied to the gate-to-source and bulk–source of nth transistor, respectively. $g_{m\mathrm{b1}}$ is the first-order coefficient of the bulk-transconductance of the transistor M_1. $g'_{m\mathrm{b1}}$ and $g''_{m\mathrm{b1}}$ denote the first- and second-order derivatives of bulk transconductance, respectively.

The ultimate goal is to derive the relationship between the input voltage and the output current by using the Volterra series expansion in the frequency domain so that the third-order nonlinearity coefficient can be identified. Hence, the gate–source and bulk voltages of M_1 can be modeled by the following truncated Volterra series with respect to the input voltage v_{in1} as:

$$\begin{aligned} v_g &= A_1(\omega) \circ v_{\mathrm{in1}} + A_2(\omega_1, \omega_2) \circ v_{\mathrm{in1}}^2 \\ &\quad + A_3(\omega_1, \omega_2, \omega_3) \circ v_{\mathrm{in1}}^3 \end{aligned} \tag{21}$$

$$\begin{aligned} v_s &= B_1(\omega) \circ v_{\mathrm{in1}} + B_2(\omega_1, \omega_2) \circ v_{\mathrm{in1}}^2 \\ &\quad + B_3(\omega_1, \omega_2, \omega_3) \circ v_{\mathrm{in1}}^3 \end{aligned} \tag{22}$$

$$\begin{aligned} v_d &= C_1(\omega) \circ v_{\mathrm{in1}} + C_2(\omega_1, \omega_2) \circ v_{\mathrm{in1}}^2 \\ &\quad + C_3(\omega_1, \omega_2, \omega_3) \circ v_{\mathrm{in1}}^3 \end{aligned} \tag{23}$$

$$v_b = D_2(\omega_1, \omega_2) \circ v_{\mathrm{in1}}^3. \tag{24}$$

Similarly, A_n's, B_n's, C_n's, and D_n's values model the nth-order nonlinear responses. First, we can develop Kirchhoff's current law (KCL) equations at each node to derive the A_n, B_n, C_n, and D_n kernels as follows:

$$\begin{aligned} \frac{v_{\mathrm{in1}} - v_g}{Z_1(\omega)} &= Y_{\mathrm{gs1}}(\omega)(v_g - v_s) \\ &\quad + Y_{\mathrm{gd1}}(\omega)(v_g - v_d) \end{aligned} \tag{25}$$

$$i_{\mathrm{ds1}} + Y_{\mathrm{gs1}}(\omega)\left(v_g - v_s\right) = \frac{1}{Z_s(\omega)}v_s \tag{26}$$

$$Y_{\mathrm{gd1}}(\omega)(v_g - v_d) = i_{\mathrm{ds1}} + \frac{v_d}{Z_L(\omega)} \tag{27}$$

$$\begin{aligned} i_b &= i_{\mathrm{ds3}} + i_{\mathrm{ds4}} \\ &= Y_b(\pm\omega_1 \pm \omega_2)v_b \end{aligned} \tag{28}$$

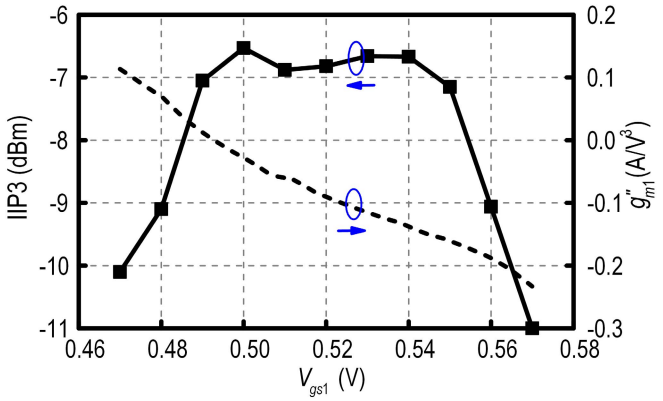

Fig. 10. Simulated IIP3 and g''_{m1} of the input transistor $M_{1,2}$ without integrating IM2 circuit relating to its gate–source voltage V_{gs1}.

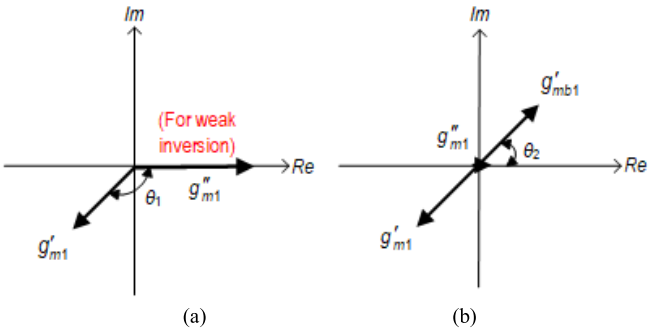

Fig. 11. Vector diagram for the components of $G_3(\pm\omega_1, \pm\omega_1, \omega_2)$ for (a) conventional ISD transconductor and (b) proposed ISD transconductor.

where $Y_b = 1/R_1 + j\omega C_1$ is the output drain admittance of transistor $M_{3,4}$. Here, Z_L represents impedance at the drain node of transistor $M_{1,2}$, which includes R_{sw} and the parasitic capacitance at this drain node. Taking M_3 and M_4 to be identical and substituting (19) and (20) into (28), the output voltage of the squaring circuit can be expressed as

$$v_b = 2\frac{1}{Y_b(\pm\omega_1 \mp \omega_2)}g'_{m3}v_g^2. \tag{29}$$

From (24) and (29), the second-order Volterra kernel of $D_2(\omega_1, \omega_2)$ can be derived as

$$D_2(\pm\omega_1, \mp\omega_2) = \frac{2g'_{m3}}{Y_b(\pm\omega_1 \mp \omega_2)}A_1(\omega_1)A_1(\omega_2). \tag{30}$$

In reference to Fig. 9, a nodal equation at the drain node of transistor M_1 can be obtained as

$$i_{\mathrm{ds1}} = i_{out} = -v_d/Z_L(\omega). \tag{31}$$

Hence, the nth-order Volterra operator $G_{n,p}$ that describes the output current nonlinearity of the proposed transconductor is given as

$$G_{n,p} = -C_n/Z_L\left(\sum_{i=1}^{\{2,3\}}\omega_i\right). \tag{32}$$

Therefore, $C_n(\omega_1, \omega_2, \ldots, \omega_n)$ has to be derived to obtain $G_{n,p}$ of the Volterra operators. Equations (25)–(27) are solved

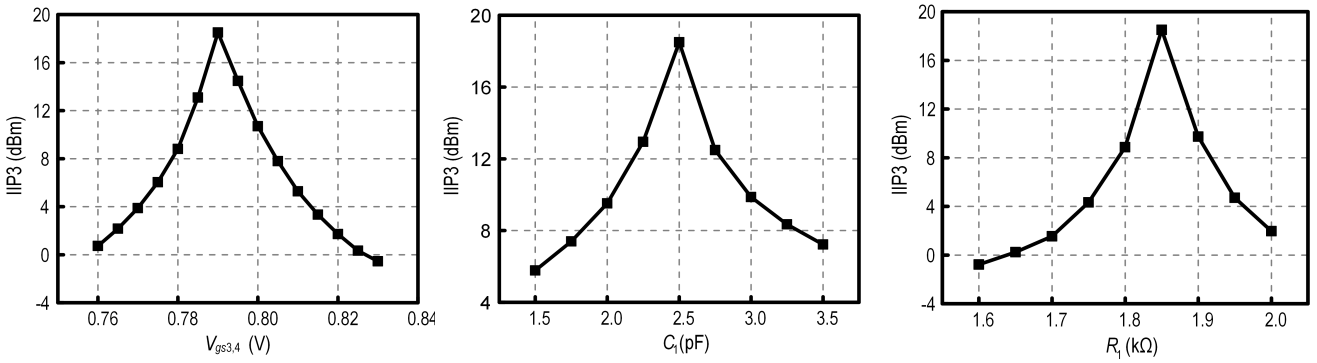

Fig. 12. Simulated plots of (a) IIP3 versus $V_{\mathrm{gs3,4}}$ at constant $C_1 = 2.5$ pF and $R_1 = 1.85$ kΩ, (b) IIP3 versus capacitor C_1 at constant $V_{\mathrm{gs3,4}} = 0.79$ V and $R_1 = 1.85$ kΩ, and (c) IIP3 versus resistor R_1 at constant $V_{\mathrm{gs3,4}} = 0.79$ V and $C_1 = 2.5$ pF.

recursively to obtain the kernels in (21)–(23). The detailed derivation of the Volterra kernels is given in the Appendix. By using Volterra kernels $A_n(\omega_1, \omega_2, \ldots, \omega_n)$, $B_n(\omega_1, \omega_2, \ldots, \omega_n)$, and $C_n(\omega_1, \omega_2, \ldots, \omega_n)$, $G_{n,p}(\omega_1, \omega_2, \ldots, \omega_n)$ of the Volterra operators are described in (33)–(35), shown at the bottom of the page.

Hence, by substituting (33) and (35) into (2), it is observed that IIP3 of the transconductor can be improved substantially by reducing the magnitude of the third-order harmonic Volterra operator $G_{3,p}(\pm\omega_1, \pm\omega_1, \pm\omega_2)$. Clearly, (35) shows that the linearity performance of the transconductor is limited by the first term in the numerator bracket, that is, the direct distortion from the composite g''_{m1} and the second term is the feedback interact distortion component by the first- and second-order products with the intrinsic second-order nonlinear term g'_{m1} of the input transistors. The third term is an additional bulk interaction distortion that is formed by the proposed IM2 injection technique. The third-order bulk-transconductance nonlinearity distortion g''_{mb1} in (35) is negligible as it contributes a relatively low effect compared to the other distortion components.

By solving the third-order $G_{3,p}(\pm\omega_1, \pm\omega_1, \pm\omega_2)$ kernel using mathematic tools such as Mathematica or Maple, the closed-form expressions can be obtained, where this mathematical relation is inscrutable as it is lengthy. Thus, the characteristic of this circuit is best described graphically by the vector diagram obtained through this expression using the mathematical tool.

In this article, the intrinsic third-order nonlinearity is eliminated by nullifying the composite g''_{m1}, which is achieved by setting the gate bias of input transistors at g''_{m1} equal to zero. Fig. 10 shows the IIP3 behavior of the ISD transconductor for an aspect ratio of 60/0.13 μm with stacked switching and IF stages. However, the IIP3 does not exhibit significant improvement at the sweet spot of $V_{\mathrm{gs1}} = 0.49$ V due to the second-order nonlinearity of the input transistor, g'_{m1}, which contributes IMD3 as explained in Section II. Therefore, an IM2 injection technique is also implemented to suppress the third-order nonlinearity distortion current that arises due to the feedback effect.

The generated g'_{m1} nonlinear distortion is mainly caused by the gate–drain capacitance and degenerated inductance. Hence,

$$G_{1,p}(\omega) = -\frac{1}{Z_x(\omega)} \cdot \frac{1}{g_{m1} + g_p(\omega)} \{ g_{m1}(Y_{\mathrm{gd1}}(\omega) Z_s(\omega) - 1) + g_{\mathrm{mb1}} c(\omega) Z_s(\omega) + b(\omega) Y_{\mathrm{gd1}}(\omega) \} \tag{33}$$

$$G_{2,p}(\pm\omega_1, \mp\omega_2) = \frac{\alpha(\pm\omega_1 \mp \omega_2)}{Z_x(\pm\omega_1 \mp \omega_2)} \left\{ \begin{array}{l} g'_{m1}(A_1(\pm\omega_1)A_1(\mp\omega_2) - A_1(\pm\omega_1)B_1(\mp\omega_2) - B_1(\pm\omega_1)A_1(\mp\omega_2)) \\ +(g'_{m1} - g'_{\mathrm{mb1}})B_1(\pm\omega_1)B_1(\mp\omega_2) + g_{\mathrm{mb1}} D_2(\pm\omega_1, \mp\omega_2) \end{array} \right\} \tag{34}$$

$$G_{3,p}(\pm\omega_1, \pm\omega_1, \mp\omega_2) = \frac{\alpha(\pm 2\omega_1 \mp \omega_2)}{Z_x(\pm 2\omega_1 \mp \omega_2)} \left\{ \begin{array}{l} g''_{m1} \left[\begin{array}{l} A_1^2(\pm\omega_1)A_1(\mp\omega_2) - B_1^2(\pm\omega_1)B_1(\mp\omega_2) \\ -3(2A_1^2(\pm\omega_1)B_1(\mp\omega_2) + A_1(\pm\omega_1)A_1(\mp\omega_2)B_1(\pm\omega_1)) \\ +3(2B_1^2(\pm\omega_1)A_1(\mp\omega_2) + B_1(\pm\omega_1)B_1(\mp\omega_2)A_1(\pm\omega_1)) \end{array} \right] \\ +\frac{2}{3} g'_{m1} \left[\begin{array}{l} 2A_1(\pm\omega_1)A_2(\pm\omega_1, \mp\omega_2) + A_1(\mp\omega_2)A_2(\pm\omega_1, \pm\omega_1) \\ -2A_1(\pm\omega_1)B_2(\pm\omega_1, \mp\omega_2) - A_1(\mp\omega_2)B_2(\pm\omega_1, \pm\omega_1) \\ -2B_1(\pm\omega_1)A_2(\pm\omega_1, \mp\omega_2) - B_1(\mp\omega_2)A_2(\pm\omega_1, \pm\omega_1) \\ +2B_1(\pm\omega_1)B_2(\pm\omega_1, \mp\omega_2) + B_1(\mp\omega_2)B_2(\pm\omega_1, \pm\omega_1) \end{array} \right] \\ -\frac{2}{3} g'_{\mathrm{mb1}} \left[\begin{array}{l} 2B_1(\pm\omega_1)B_2(\pm\omega_1, \mp\omega_2) + B_1(\mp\omega_2)B_2(\pm\omega_1, \pm\omega_1) \\ -2B_1(\pm\omega_1)D_2(\pm\omega_1, \mp\omega_2) - B_1(\mp\omega_2)D_2(\pm\omega_1, \pm\omega_1) \end{array} \right] \\ -g''_{\mathrm{mb1}} B_1^2(\pm\omega_1)B_1(\mp\omega_2) \end{array} \right\}. \tag{35}$$

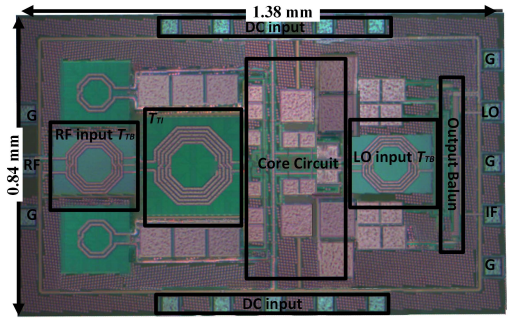

Fig. 13. Microphotograph of the proposed LNA mixer.

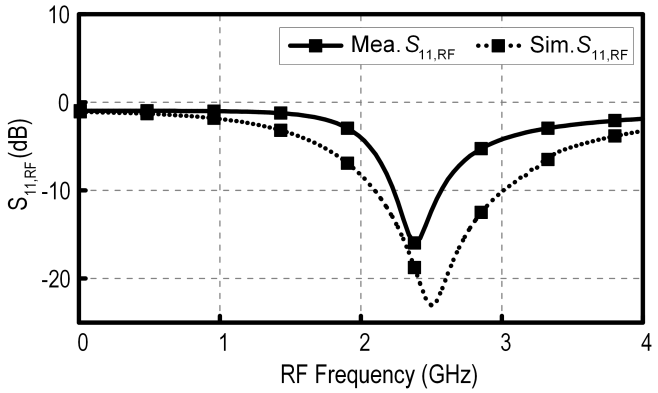

Fig. 14. Measured and simulated of input return loss (S_{11}) of the RF port.

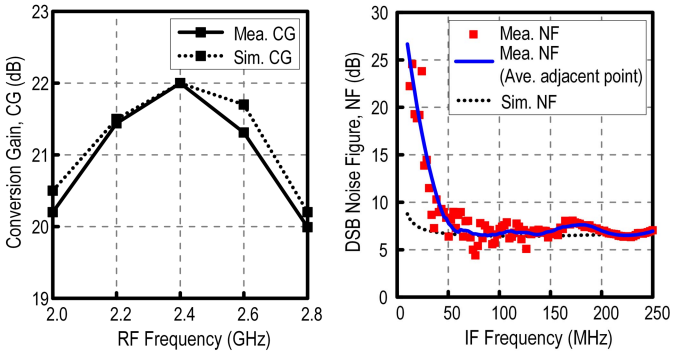

Fig. 15. Measured and simulated (a) CG versus RF frequency and (b) DSB NF versus IF frequency.

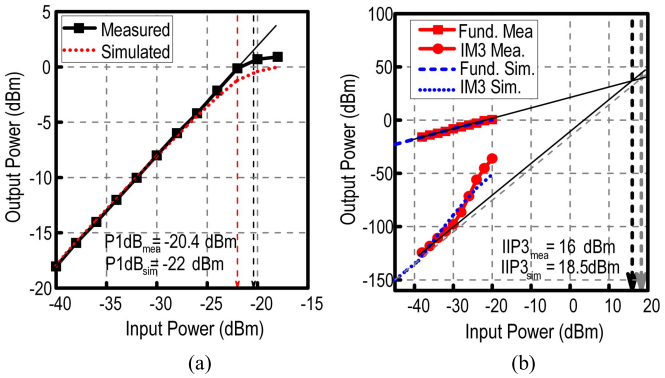

Fig. 16. Measured and simulated (a) $P_{1\,\mathrm{dB}}$ and (b) two-tone IIP3 results.

the angle of θ_1 in Fig. 11(a) is relaxed from the parametric variation of R_1 and C_1. By adjusting R_1 and C_1 defined through the term g'_{mb1}, a collinear relationship is established with the vector of the second-order distortion produced by g'_{m1} with a fixed value of the input device size and L_s. As shown in Fig. 11(b), the imaginary and real parts of g'_{mb1} contribution is adjusted such that it is out-of-phase with the second-order contribution of g'_{m1}.

Initially, the aspect ratio of $M_{3,4}$ is set to achieve an accurate input impedance matching by setting its gate capacitance equal to that of $M_{1,2}$. Thus, the dc bias of $M_{3,4}$, R_1, and C_1 is chosen appropriately to give the desired IM2 amplitude and phase while setting the gate bias of M_1 ($V_{gs1} = 0.49$ V) to the sweet spot point. To validate the Volterra analysis, an extensive set of simulation is done using the Cadence SpectreRF simulator. The graph in Fig. 12 shows that the maximum IIP3 appears at a gate-bias voltage $V_{gs3,4}$ of 0.79 V with capacitance $C_1 = 2.5$ pF and resistance $R_1 = 1.85$ kΩ. However, this technique is frequency-dependent and the phase shift of IM2 injection would limit the linearity improvement. Therefore, it is more suitable for a narrowband circuit with small two-tone spacing.

The gate-input feedback effect can also be eliminated due to the differential nature of the transformer balun, which cancels out the even-order distortion current at the gate of the transistor $M_{1,2}$ by transforming it back to the input in antiphase.

IV. Experimental Results

Based on the extensive analysis, a highly linear balun-LNA mixer is implemented with a 0.13-μm CMOS technology by Global Foundries. The microphotograph of the proposed architecture is shown in Fig. 13, with a total area of 1.16 mm^2, which includes the pad and the output active balun. We measured the chip through on-chip wafer probing. In this characterization, an active balun (not shown for conciseness) is integrated at the output of the LNA mixer to convert the differential IF signals into a single-ended output with a 50-Ω matching. The input port is single-ended and matched to the 50-Ω characteristic impedance of the system and enabled the integration of single-ended front-end antenna to the balun-LNA mixer circuit.

The core balun-LNA mixer and the squaring circuit consumes 3.15 mW of power at 1.2 V. Fig. 14 shows the input reflection coefficient at the RF port, which is less than −10 dB at the desired frequency. The measurement and a comparative simulation of CG versus RF frequency are performed for a fixed IF of 100 MHz at an LO power of 0 dBm. As presented in Fig. 15(a), the simulated and measured power CG is 22 dB. Fig. 15(b) shows the simulated and measured double-sideband (DSB) NF as a function of IF frequency. The NF is 7.2 dB at the output IF frequency of 100 MHz.

Fig. 16(a) shows that the measured and simulated $P_{1\,\mathrm{dB}}$ of −22 and −20.4 dBm, respectively, at the input RF frequency of 2.4 GHz. We applied a two-tone RF signal at

TABLE II
CIRCUIT PARAMETER OF THE PROPOSED BALUN-LNA+MIXER

Reference	Process (μm)	RF (GHz)	CG (dB)	NF (dB)	P1dB (dBm)	IIP3 (dBm)	V_{DD} (V)	P_{DC} (mW)	FOM (dB)	Topology	Circuit
[11]** VLSI'16	0.09	2.4	9.8	15.0	N/A	+15.7	1.2	5.8	-15.7	Fully-differential	Mixer
[13]** VLSI'16	0.18	2.4	6.7	17.0	N/A	+9.0	1.6	4.6	-22.8	Fully-differential	Mixer
[24]** EL'14	0.09	2.4	22.1	13.2	N/A	+17.1	1.0	4.0	-4.6	Fully-differential	Mixer
[25]** ISCAS'14	0.18	2.4	5.0	27.0*	N/A	+9.0	1.8	23.76	-41.3	Fully-differential	Mixer
[26] EL'16	0.18	0.1-2.5	8.9	9.6	-4	+5.8	1.8	3.74	-15.5	Fully-differential	Mixer
[27]** AEU'14	0.13	2.4	22.3	7.2	-22.3	-10.8	0.5	0.91	-3.0	Fully-differential	LNA+Mixer
[28] TCAS-I'18	0.18	0.4	11.6	14.7	N/A	+3.6	1.2	1.1	-13.3	Single-ended RF input	Passive front-end RX
[29] VLSI'19	0.13	0.9	40	14	N/A	-6	1.2	1.16	-3.4	Fully-differential	RX
[30] TMTT'19	0.13	2.4	42	7.2	N/A	-17	1.2	1.7	-2.8	Single-ended RF input	RX
[31] TCAS-I'13	0.18	2.4	31	3	N/A	-10	1.8	9	-9.6	Single-ended RF input	Subharmonic front-end RX
This work	**0.13**	**2.4**	**22.0**	**7.2***	**-20.4**	**+16.0**	**1.2**	**3.15**	**1.03**	**Single-ended RF input**	**Balun+LNA +Mixer**

*DSB noise **Simulated results †Estimated from graph

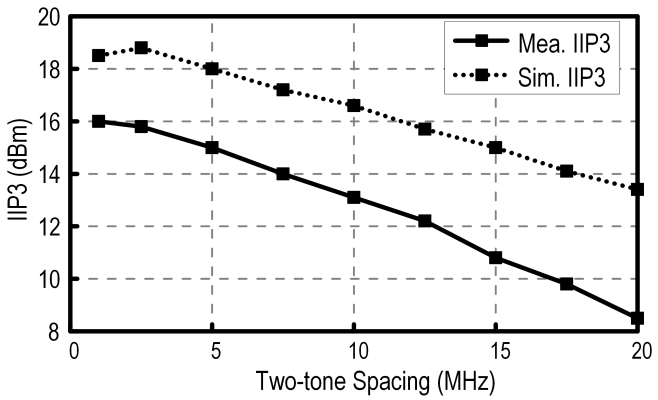

Fig. 17. Measured and simulated IIP3 versus two-tone spacing.

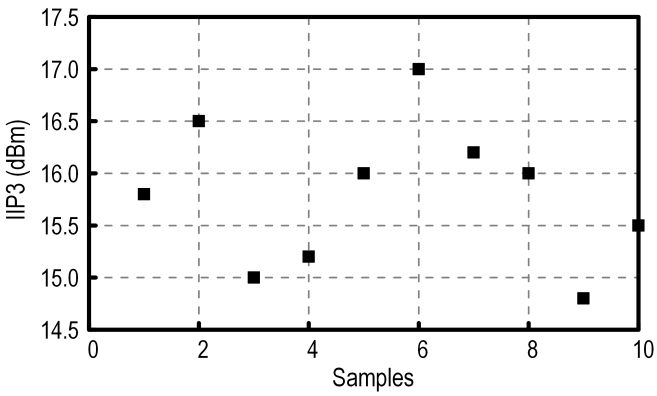

Fig. 18. Measured IIP3 over ten samples.

2.4 and 2.401 GHz with 1-MHz frequency offset to extract the IIP3 performance. Fig. 16(b) shows the output power against input power for both fundamental and IM3 components, resulting in an IIP3 of +16 dBm. As the IM3 suppression is dependent on the two-tone spacing $\omega_2 - \omega_1$, IIP3 results would vary under different two-tone spacing frequency, as shown in Fig. 17. An increase in frequency space causes a decrease in IIP3 performance.

Fig. 18 shows the measured IIP3 for a sample of ten chips at the operating frequency of 2.4 GHz, where the gate-bias voltage of $M_{1,2}$ and $M_{3,4}$ is adjusted externally to maintain the desired IIP3 performance.

In addition, Fig. 19 shows the simulated performance of the uncalibrated and calibrated IIP3 for various process, voltage, and temperature (PVT) conditions at 2.4 GHz. As expected, the optimum gate biasing technique is sensitive to the PVT variation. We can deduce that after applying the external gate-bias voltage calibration for both transistors $M_{1,2}$ and $M_{3,4}$, all the obtained IIP3 is significantly improved.

Table II summarizes the performance of the proposed highly linear balun-LNA mixer. The comparison with prior reported works proximating at the same operating frequency in the CMOS technology is tabulated, adopting the figure of merits (FOM) [32]. For a fair comparison, the headroom is accounted in the computation as

$$\mathrm{FOM} = 10\log\left(\frac{10^{\mathrm{CG(dB)}/20} \times 10^{(\mathrm{IIP3(dB)}-10)/20}}{10^{\mathrm{NF(dB)}/10} \times P_{\mathrm{DC}}(\mathrm{mW}) \times V_{\mathrm{DD}}(\mathrm{V})}\right). \quad (36)$$

The presented architecture strikes a good balance between CG, NF, linearity, and power consumption. Therefore, it achieves a superior FOM with only 0.36 mW of additional power consumption from the squaring circuit.

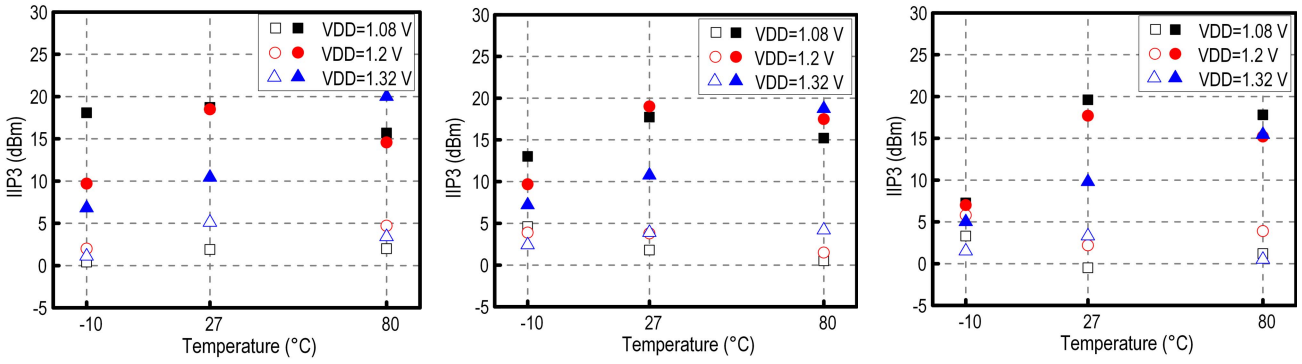

Fig. 19. Simulated IIP3 with PVT variations. (a) Typical corner. (b) Slow–slow corner. (c) Fast–fast corner. The open symbol represents uncalibrated IIP3 and solid symbol represents calibrated IIP3.

V. Conclusion

In this article, a novel solution to improve the linearity of the conventional ISD transconductance stage by implementing both optimum biasing and IM2 injection techniques was presented. The optimum biasing technique was employed in the input transistors to set the second-order derivative transconductance to zero. The use of the IM2 injection technique at the bulk of the input transistors suppresses the second-order feedback components. The measurement result in the 0.13-μm CMOS process at 2.4 GHz showed that the differential balun-LNA mixer only dissipates 3.15 mW of power from 1.2-V power supply with an NF of 7.2 dB, a CG of 22 dB, an IIP3 of +16 dBm, and a $P_{1\ \mathrm{dB}}$ of −20.4 dBm with no off-chip components required. Comparing with the state-of-the-art architecture, a high linearity, high CG, and low power consumption solution was presented.

Appendix

In this appendix, a complete IIP3 derivation of the Volterra series kernels for the proposed ISD transconductance (referring Fig. 9) is given. Each harmonic order in (21)–(23) can be solved by equating each order components in (25)–(27). Therefore, we excite the circuit with a single tone and transform the obtained linear transfer functions into the matrix in (37), shown at the bottom of the page. Now, the first-order Volterra kernels can be solved easily by using Cramer's rule yielding

$$A_1(\omega) = \frac{1}{Z_x(\omega)} \cdot \frac{1}{g_{m1} + g_p(\omega)} \times \{a(\omega)((g_{m1} + g_{\mathrm{ds1}} + g_{\mathrm{mb1}})Z_s(\omega) + b(\omega)) + g_{\mathrm{ds1}} b(\omega) Z_L(\omega)\} \tag{38}$$

$$B_1(j\omega) = \frac{Z_s(\omega)}{Z_x(\omega)} \cdot \frac{1}{g_{m1} + g_p(\omega)} \times \begin{Bmatrix} a(\omega)(g_{m1} + Y_{\mathrm{gs1}}(\omega)) \\ +g_{\mathrm{ds1}} c(\omega) Z_L(\omega) \end{Bmatrix} \tag{39}$$

$$C_1(\omega) = -\frac{Z_L(\omega)}{Z_x(\omega)} \cdot \frac{1}{g_{m1} + g_p(\omega)} \times \{g_{m1}(Y_{\mathrm{gd1}}(\omega) Z_s(\omega) - 1) + g_{\mathrm{mb1}} c(\omega) Z_s(\omega) + b(\omega) Y_{\mathrm{gd1}}(\omega)\} \tag{40}$$

$$\begin{bmatrix} \frac{1}{Z_1(\omega)} + Y_{\mathrm{gs1}}(\omega) + Y_{\mathrm{gd1}}(\omega) & -Y_{\mathrm{gs1}}(\omega) & -Y_{\mathrm{gd1}}(\omega) \\ g_{m1} - Y_{\mathrm{gd1}}(\omega) & -(g_{m1} + g_{\mathrm{ds1}} + g_{\mathrm{mb1}}) & g_{\mathrm{ds1}} + Y_{\mathrm{gd1}}(\omega) + \frac{1}{Z_L(\omega)} \\ g_{m1} + Y_{\mathrm{gs1}}(\omega) & -\left(g_{m1} + g_{\mathrm{ds1}} + g_{\mathrm{mb1}} + Y_{\mathrm{gs1}}(\omega) + \frac{1}{Z_s(\omega)}\right) & g_{\mathrm{ds1}} \end{bmatrix} \begin{bmatrix} A_1(\omega) \\ B_1(\omega) \\ C_1(\omega) \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_1(\omega)} \\ 0 \\ 0 \end{bmatrix} \tag{37}$$

$$\begin{bmatrix} \sum_{i=1}^{\{2,3\}} \left(\frac{1}{Z_1(\pm\omega_i)} + Y_{\mathrm{gs1}}(\pm\omega_i) + Y_{\mathrm{gd1}}(\pm\omega_i)\right) & -\sum_{i=1}^{\{2,3\}} Y_{\mathrm{gs1}}(\pm\omega_i) & -\sum_{i=1}^{\{2,3\}} Y_{\mathrm{gd1}}(\pm\omega_i) \\ g_{m1} - \sum_{i=1}^{\{2,3\}} Y_{\mathrm{gd1}}(\pm\omega_i) & -g_{m1} - g_{\mathrm{ds1}} - g_{\mathrm{mb1}} & \sum_{i=1}^{\{2,3\}} \left(Y_{\mathrm{gd1}}(\pm\omega_i) + \frac{1}{Z_L(\pm\omega_i)}\right) \\ g_{m1} + \sum_{i=1}^{\{2,3\}} Y_{\mathrm{gs1}}(\pm\omega_i) & -g_{m1} - g_{\mathrm{ds1}} - g_{\mathrm{mb1}} - \sum_{i=1}^{\{2,3\}} (Y_{\mathrm{gs1}}(\pm\omega_i) + Y_s(\pm\omega_i)) & g_{\mathrm{ds1}} \end{bmatrix} \cdot \begin{bmatrix} A_n(\omega_1, \ldots n) \\ B_n(\omega_1, \ldots n) \\ C_n(\omega_1, \ldots n) \end{bmatrix} = \begin{bmatrix} 0 \\ -(i_{n,ds(gm)}^{n\in\{2,3\}} + i_{n,ds(gmb)}^{n\in\{2,3\}}) \\ -(i_{n,ds(gm)}^{n\in\{2,3\}} + i_{n,ds(gmb)}^{n\in\{2,3\}}) \end{bmatrix} \tag{42}$$

where

$$g_p(\omega) = \frac{1}{Z_x(\omega)} \cdot \left\{ \begin{matrix} g_{\mathrm{ds1}}(Z_x(\omega) + Z_y(\omega)) + Y_{\mathrm{gs1}}(\omega) Z_x(\omega) \\ +(g_{m\mathrm{b1}} + 1)(a(\omega) + c(\omega) Z_1(\omega)) \end{matrix} \right\}. \tag{41}$$

By following the same procedure with two- and three-tone excitations, one acquires matrix (42), shown at the bottom of the previous page. $\sum_{i=1}^{\{2,3\}}(\pm\omega_i)$ indicates the frequency dependence of the passive components for the second- and third-order analyses; it can be $\pm\omega_1 \pm \omega_2$ or $\pm\omega_1 \pm \omega_2 \pm \omega_3$ depending on the nonlinearity order. Alternatively, the second and third nonlinearities of the drain current due to the transconductance and bulk transconductance are represented as $i_{n,ds(gm)}^{\{2,3\}}$ and $i_{n,ds(gmb)}^{\{2,3\}}$, respectively, which can be obtained by substituting (21)–(24) into (18). Consequently, $i_{n,ds(gm)}^{\{2,3\}}$ and $i_{n,ds(gmb)}^{\{2,3\}}$ are given as

$$\begin{aligned} &i_{2,ds(gm)} + i_{2,ds(gmb)} \\ &= g'_{m1}(A_1(\omega_1)A_1(\omega_2) - 2\overline{A_1(\omega_1)B_1(\omega_2)} + B_1(\omega_1)B_1(\omega_2)) \\ &\quad - g'_{m\mathrm{b1}} B_1(\omega_1)B_1(\omega_2) + g_{m\mathrm{b1}} D_2(\omega_1, \omega_2) \end{aligned} \tag{43}$$

$$\begin{aligned} &i_{3,ds(gm)} + i_{3,ds(gmb)} \\ &= g''_{m1} \left(\begin{matrix} \overline{A_1(\omega_1)} - \overline{B_1(\omega_1)} - 3\overline{A_1(\omega_1)A_1(\omega_2)B_1(\omega_3)} \\ +3\overline{A_1(\omega_1)B_1(\omega_2)B_1(\omega_3)} \end{matrix} \right) \\ &\quad + 2g'_{m1} \left(\begin{matrix} \overline{A_1(\omega_1)A_2(\pm\omega_2,\pm\omega_3)} - \overline{A_1(\omega_1)B_2(\pm\omega_2,\pm\omega_3)} \\ -\overline{B_1(\omega_1)A_2(\pm\omega_2,\pm\omega_3)} + \overline{B_1(\omega_1)B_2(\pm\omega_2,\pm\omega_3)} \end{matrix} \right) \\ &\quad - 2g'_{m\mathrm{b1}} \left(\begin{matrix} \overline{B_1(\omega_1)B_2(\pm\omega_2,\pm\omega_3)} \\ -\overline{B_1(\omega_1)D_2(\pm\omega_2,\pm\omega_3)} \end{matrix} \right) - g''_{m\mathrm{b1}} \overline{B_1(\omega_1)}. \end{aligned} \tag{44}$$

From (42), with the Cramer rules, the second- and third-order Volterra kernels, $A_{\mathrm{n}}(\omega_1, \ldots \omega_{\mathrm{n}})$, $B_{\mathrm{n}}(\omega_1, \ldots \omega_{\mathrm{n}})$, and $C_{\mathrm{n}}(\omega_1, \ldots \omega_{\mathrm{n}})$, are computed as

$$\begin{aligned} &A_2(\pm\omega_1, \pm\omega_2) \\ &= -\left\{ \begin{matrix} g'_{m1}(A_1(\omega_1)A_1(\omega_2) - 2\overline{A_1(\omega_1)B_1(\omega_2)}) \\ +(g'_{m1} - g'_{m\mathrm{b1}})B_1(\omega_1)B_1(\omega_2) + g_{m\mathrm{b1}} D_2(\omega_1, \omega_2) \end{matrix} \right\} \\ &\quad \times \sum_{i=1,2} \left(\frac{1}{g_{m1} + g_p(\pm\omega_i)} \cdot \frac{(a(\pm\omega_i) - b(\pm\omega_i))Z_1(\pm\omega_i)}{Z_x(\pm\omega_i)} \right) \end{aligned} \tag{45}$$

$$\begin{aligned} &B_2(\pm\omega_1, \pm\omega_2) \\ &= -A_2(\pm\omega_1, \pm\omega_2) \\ &\quad \times \sum_{i=1,2} \left\{ \frac{Z_s(\pm\omega_i)}{Z_1(\pm\omega_i)} \cdot \frac{a(\pm\omega_i) + c(\pm\omega_i)Z_1(\pm\omega_i)}{a(\pm\omega_i) - b(\pm\omega_i)} \right\} \end{aligned} \tag{46}$$

$$\begin{aligned} &C_2(\pm\omega_1, \pm\omega_2) \\ &= A_2(\pm\omega_1, \pm\omega_2) \times \sum_{i=1,2} \left\{ \frac{Z_L(\pm\omega_i)}{Z_1(\pm\omega_i)} \cdot \frac{\alpha(\pm\omega_i)}{a(\pm\omega_i) - b(\pm\omega_i)} \right\} \end{aligned} \tag{47}$$

$$\begin{aligned} &A_3(\pm\omega_1, \pm\omega_2, \pm\omega_3) \\ &= -(i_{3,ds(gm)} + i_{3,ds(gmb)}) \\ &\quad \times \sum_{i=1}^{\{2,3\}} \left(\frac{1}{g_{m1} + g_p(\pm\omega_i)} \cdot \frac{(a(\pm\omega_i) - b(\pm\omega_i))Z_1(\pm\omega_i)}{Z_x(\pm\omega_i)} \right) \end{aligned} \tag{48}$$

$$\begin{aligned} &B_3(\pm\omega_1, \pm\omega_2, \pm\omega_3) \\ &= -A_3(\pm\omega_1, \pm\omega_2, \pm\omega_3) \\ &\quad \times \sum_{i=1}^{\{2,3\}} \left(\frac{Z_s(\pm\omega_i)}{Z_1(\pm\omega_i)} \cdot \frac{a(\pm\omega_i) + c(\pm\omega_i)Z_1(\pm\omega_i)}{a(\pm\omega_i) - b(\pm\omega_i)} \right) \end{aligned} \tag{49}$$

$$\begin{aligned} &C_3(\pm\omega_1, \pm\omega_2, \pm\omega_3) \\ &= A_3(\pm\omega_1, \pm\omega_2, \pm\omega_3) \\ &\quad \times \sum_{i=1}^{\{2,3\}} \left\{ \frac{Z_L(\pm\omega_i)}{Z_1(\pm\omega_i)} \cdot \frac{\alpha(\pm\omega_i))}{a(\pm\omega_i) - b(\pm\omega_i)} \right\}. \end{aligned} \tag{50}$$

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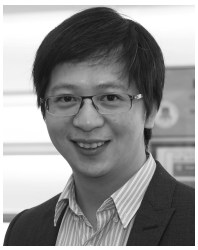

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