Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators

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***Abstract*—The digital low dropout regulator (D-LDO) has drawn significant attention recently for its low-voltage operation and process-scalability. However, the D-LDO inherently suffers from limit cycle oscillation (LCO). To address this issue, the modes and amplitudes of LCO are calculated in this work and verified by SPICE simulation in a 65-nm CMOS process. An LCO reduction technique for the D-LDO is then proposed, by adding two unit power transistors in parallel with the main power MOS array as a feedforward path. This technique sets the LCO mode to 1 and effectively reduces the ripple amplitude for a wide (0.5–20 mA) load current range. When compared with the dead-zone scheme, this technique minimizes LCO with negligible circuit complexity and design difficulty.**

***Index Terms*—Compensation zero, describing function, digital control, feedforward path, limit cycle oscillation (LCO), low dropout regulator (LDO), sampled nonlinear system.**

I. Introduction

A digital low dropout regulator (D-LDO) based on bidirectional shift register was first proposed in [1], and it has recently drawn significant attention [2]. The block diagram is shown in Fig. 1(a), where the power transistor in an analog LDO (A-LDO) [3] is replaced by the PMOS power transistor array, and a sampled comparator is used to sense the difference between the output voltage $V_{\rm OUT}$ and the reference voltage $V_{\rm REF}$. To minimize the steady-state error, the comparator output is fed to an integrator implemented by a serial-in parallel-out bidirectional shift register. The output of the bidirectional shift register $D(t)$ is then applied to control the number of power transistors to be turned on. Both the comparator and the bidirectional shift register are operating at the sampling frequency F_S. A load capacitor C_L is placed at the $V_{\rm OUT}$ node to reduce the output voltage ripple. The D-LDO in this topology can be scaled with process, be operated at low input voltage, and be fully integrated in a system-on-chip (SoC) with ease.

Manuscript received October 20, 2015; revised December 6, 2015; accepted February 19, 2016. Date of publication February 25, 2016; date of current version August 25, 2016. This work was supported by Macao Science & Technology Development Fund (FDCT) 122/2014/A3 and SKL/AMS-VLSI/11-Y3 and by Research Grants of the University of Macau. This brief was recommended by Associate Editor Y.-S. Hwang.

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Digital Object Identifier 10.1109/TCSII.2016.2534778

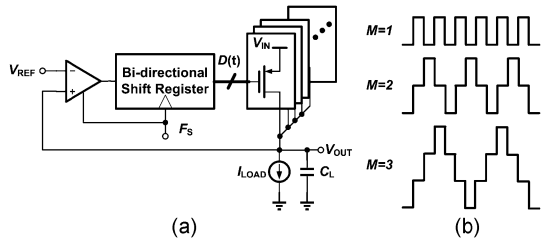

Fig. 1. (a) Block diagram of a conventional D-LDO. (b) Waveforms of the code $D(t)$ with mode-1, 2, and 3 LCOs.

However, the inherent quantization errors with this architecture will originate a steady-state limit cycle oscillation (LCO). As defined in [4], the period of LCO is $2M$ times of the sampling period T_S, where M is the mode of LCO. The waveforms of the $D(t)$ with $M = 1, 2,$ and 3 LCO are shown in Fig. 1(b).

Inciting large and unpredicted output voltage variations, LCO is generally considered to be undesirable [5]. Several previous works on LCO reduction have been published for nonsampled control systems, e.g., the digitally controlled dc–dc converter [6]–[8]. In [6], the criteria on control law and quantization resolution are suggested for LCO elimination. In [7] and [8], LCO was reduced with a higher ADC resolution which increased circuit complexity. For sampled control systems, such as the D-LDO, a dead-zone is added to the comparator stage (essentially a 1-bit ADC) for LCO reduction [9].

LCO reduction on D-LDO should be especially focused on two aspects, namely, the light load current and the low F_S conditions, which are desirable for extended load range and improved current efficiency with adaptive clock scheme [10], respectively. Nevertheless, light load current results in larger load resistance under a fixed $V_{\rm OUT}$, whereas low F_S allows longer charging/discharging time on C_L. Both conditions can incite larger LCO amplitudes and thus need special attention.

To tackle these issues, an LCO reduction technique is proposed by adding a feedforward path to the D-LDO loop. This brief is organized as follows. Analysis on the occurrence of LCO is given in Section II. Then, the proposed technique and its implementation are presented in Section III. A comparison with the dead-zone scheme is given in Section IV. Finally, a brief conclusion is drawn in Section V.

II. Analysis on LCO

The steady-state model of a conventional D-LDO is shown in Fig. 2, which consists of a sampled comparator N, a delay unit of one clock period z^{-1}, a bidirectional shift register, and a first-order plant driven by a zero-order-hold (ZOH), representing the continuous time plant consisting of the power MOS array and the load [10]. The z^{-1} is used to model the equivalent delay between the comparator and the bidirectional shift register since they are synchronously sampled. Once sampled, the comparator

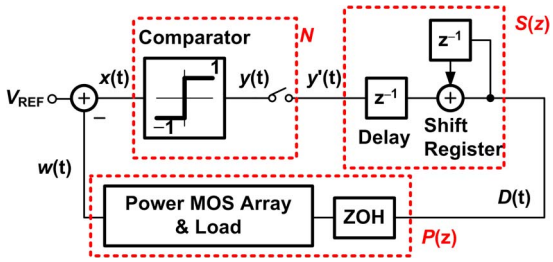

Fig. 2. Steady-state model of a conventional D-LDO.

will increase the bidirectional shift register by one count if $V_{\rm OUT}$ is larger than $V_{\rm REF}$ and will decrease by one count if smaller. This confirms the D-LDO as a nonlinear sampled control system, which can be investigated by describing function methods ([4] and [11]).

The transfer function of the bidirectional shift register including the z^{-1} delay is given as in [10]

$$S(z) = \frac{1}{1-z^{-1}} \cdot z^{-1} = \frac{1}{z-1}. \tag{1}$$

In addition, the z-domain model of the ZOH-based continuous time plant is

$$P(z) = I_{\rm UNIT} \cdot (R_{\rm LOAD} \| R_{\rm PASS}) \cdot \frac{1-e^{-\frac{T_S}{\tau}}}{z-e^{-\frac{T_S}{\tau}}} \tag{2}$$

where $I_{\rm UNIT}$ is the unit current provided by a single turned-on power transistor, $R_{\rm LOAD}$ is the load resistance, $R_{\rm PASS}$ is the combined resistance of the power transistors (given by $V_{\rm DS}/I_{\rm LOAD}$, where $V_{\rm DS}$ is the drain–source voltage of the power transistors), and τ is the time constant of the output pole $(R_{\rm LOAD} \| R_{\rm PASS}) \cdot C_L$. Therefore, the sinusoidal response function of the linear parts of this system is derived as

$$W(e^{j\omega T_S}) = S(e^{j\omega T_S}) P(e^{j\omega T_S}). \tag{3}$$

For the describing function of the comparator, we can assume that the input to the comparator is $x(t)$, while $y(t)$ represents the unsampled comparator output, and $y'(t)$ is the sampled output. Without loss of generality, the time origin is assumed to coincide with one of the sampling points. Then, $x(t)$ can be expressed as

$$x(t) = A \sin\left(\frac{\omega_S}{2M} t + \varphi\right), \quad \varphi \in \left(0, \frac{\pi}{M}\right) \tag{4}$$

where A is the LCO amplitude, ω_S is the angular sampling frequency, $\omega_S/2M$ is thus the angular LCO frequency, and φ is the phase shift. Obviously, for a $\omega_S/2M$ sinusoidal wave sampled by F_S, φ should be within 0 and π/M.

As derived in [4], the describing function of such sampled comparator, defined as the ratio between the phasor representations of $y'(t)$ and $x(t)$, can be written as

$$N(A,\varphi) = \frac{2}{MT_S A} \sum_{m=0}^{M-1} \sin\left(\frac{\pi}{2M} + \frac{m\pi}{M}\right) \angle \left(\frac{180^\circ}{2M} - \varphi\right). \tag{5}$$

According to the Nyquist criterion, if a mode-M LCO exists, the following condition should be met:

$$N(A,\varphi) \cdot W(e^{j\omega T_S}) = 1 \angle -180^\circ, \quad \varphi \in \left(0, \frac{\pi}{M}\right) \tag{6}$$

where ω is equal to the angular LCO frequency $\omega_S/2M$. Based on (6), the LCO mode and amplitude can be calculated.

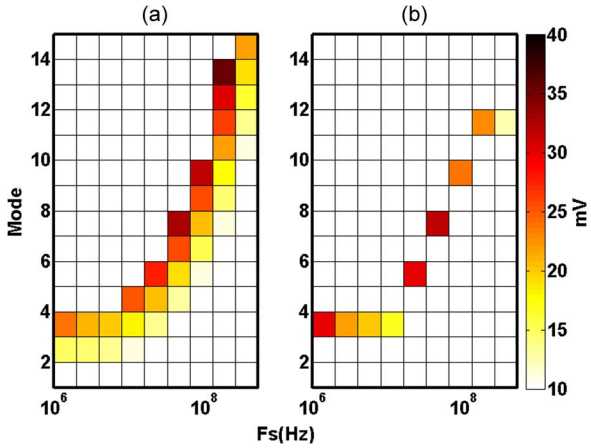

Fig. 3. LCO modes and amplitudes using (a) MATLAB calculation and (b) SPICE simulation with F_S from 1 to 256 MHz.

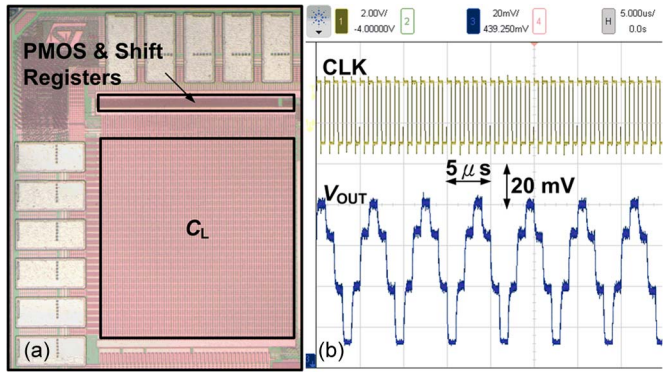

Fig. 4. (a) Chip microphotograph of the measured D-LDO and (b) the measured LCO with 1-MHz F_S.

A numerical calculation on LCO versus F_S (from 1 to 256 MHz) is performed using MATLAB, with a 1-mA load current and a 1-nF C_L. The LCO modes and amplitudes are plotted in Fig. 3(a), where the y-axis shows the possible modes of LCO and the color bar shows the corresponding amplitudes. Note that more than one possible LCO mode exists for most of the cases, but which mode the system will be settled depends on the prior values of the system variables [4]. Meanwhile, to consolidate the theoretical analysis, transistor-level SPICE simulations are performed with identical conditions as a comparison. The simulated results are given in Fig. 3(b). The calculated modes successfully cover those obtained from a simulation with a wide range of F_S, and the amplitudes also match quite well. Specifically, the $F_S = 1$ MHz case is verified by an on-chip D-LDO [12] of which the microphotograph is shown in Fig. 4(a), with a mode-3 LCO observed in Fig. 4(b), as predicted. The D-LDO in Fig. 1 is implemented with a 65-nm standard CMOS process and consumes 2.5-μA quiescent current at 1-MHz F_S, thus achieving 99.98% current efficiency with a maximum 20-mA load current.

III. LCO Reduction Technique

To address the issues discussed in Section I, the proposed D-LDO is designed with 1-MHz F_S over a wide load range. With the same parameters as used in Section II, the calculated possible modes and amplitudes of LCO with 1–20-mA load current are shown in Fig. 5(a). Note that a larger LCO amplitude will be incited with lighter load (a 50-mV peak-to-peak ripple is incited with 1-mA load current).

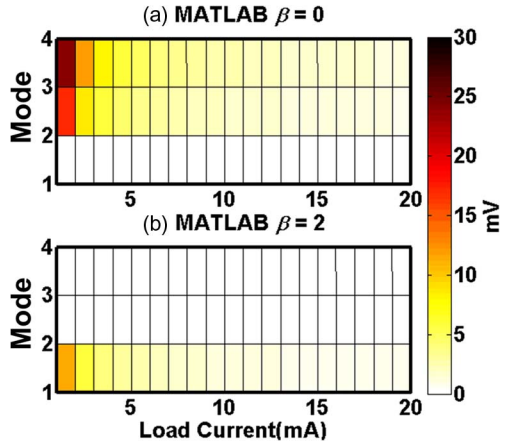

Fig. 5. MATLAB calculated results (a) without LCO reduction and (b) with $\beta = 2$, with 1-MHz F_S and load current from 1 to 20 mA.

TABLE I
PHASE SHIFT CAUSED BY THE COMPONENTS OF THE D-LDO

θ_N	θ_S	θ_P
$\frac{\pi}{2M} - \varphi$	$-\frac{\pi}{2} - \frac{\pi}{2M}$	$-\tan^{-1}\left(\frac{\pi}{M}\frac{\tau}{T_S}\right) - \frac{\pi}{2M}$

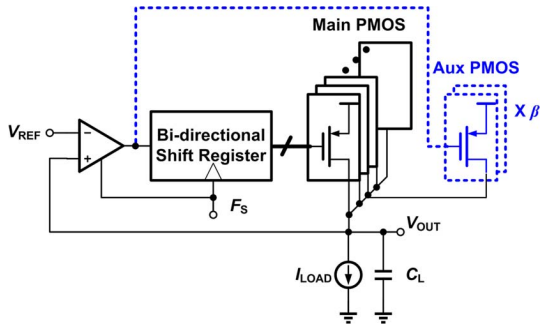

Fig. 6. Implementation of the modified D-LDO with LCO reduction.

If the LCO mode is set to 1, the number of active power transistors in the steady state will be minimized, and thus, the amplitude of LCO will be reduced. However, the mode-1 LCO cannot be guaranteed with the conventional D-LDO topology, as discussed in the following. The signal phase shifts are θ_N, θ_S, and θ_P, representing the phase shifts caused by $N(A, \varphi)$, $S(z)$, and $P(z)$, respectively. These phase shifts are calculated and summarized in Table I. Substituting them into (6), the phase shift for a steady LCO (φ_{LCO}) can be written as

$$\varphi_{\mathrm{LCO}} = \frac{\pi}{2} - \frac{\pi}{2M} - \tan^{-1}\left(\frac{\pi}{M}\frac{\tau}{T_S}\right), \quad \varphi_{\mathrm{LCO}} \in \left(0, \frac{\pi}{M}\right). \tag{7}$$

Since the last term of (7), $-\tan^{-1}[(\pi/M)(\tau/T_S)]$, is within $[-\pi/2, 0]$, $M = 1$ is not a possible solution of (7).

To make $M = 1$, a feedforward path is proposed to be inserted into the D-LDO, as the dashed block in Fig. 6. The steady-state model of this modified D-LDO is shown in Fig. 7. Here, the sampled comparator output is directly used to drive a set of auxiliary power transistors (Aux PMOS, β in strength) in parallel with the original power MOS array (Main PMOS). The size of the unit power transistor is the same for the Aux and Main PMOS arrays. The control word of Aux PMOS is $A(t)$. With this configuration, both the power consumption and the area overheads are negligible.

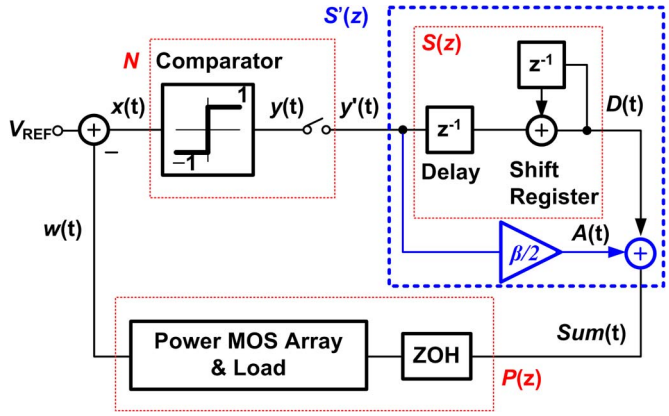

Fig. 7. Steady-state model of a modified D-LDO with the proposed LCO reduction technique.

The summed control word [summation of $D(t)$ and $A(t)$] $\mathrm{Sum}(t)$ can be expressed as

$$\mathrm{Sum}(t) = \begin{cases} \beta + D(t), & \text{if } y'(t) = 1 \\ D(t), & \text{if } y'(t) = -1 \end{cases}$$
$$\text{or } \mathrm{Sum}(t) = \frac{\beta}{2} y'(t) + D(t) + \frac{\beta}{2}. \tag{8}$$

A dc value of $\beta/2$, corresponding to the third term of (8), is introduced. If only a small signal is considered, the transfer function of the bidirectional shift register and the z^{-1} delay plus the feedforward path is given as $S'(z)$:

$$S'(z) = S(z) + \frac{\beta}{2} = \frac{1}{z-1} + \frac{\beta}{2}. \tag{9}$$

The feedforward path bypasses the integrator and thus adds a zero to the D-LDO loop. The LCO modes and amplitudes can therefore be calculated by replacing $S(z)$ with $S'(z)$ in (7). Now, the remaining issue is to determine the value of β.

In this work, $\beta = 2$ is selected to achieve minimum LCO mode and amplitude, and the reason is as follows. The calculated LCO modes and amplitudes with $\beta = 2$ are shown in Fig. 5(b). Comparing to the case with $\beta = 0$, the proposed technique sets the LCO to mode-1, which, in turn, effectively reduces the LCO amplitudes. The maximum LCO amplitude is only 11 mV at 1-mA load current.

How the LCO is set to mode-1 for $\beta = 2$ can be intuitively illustrated by Fig. 8. In mode-1, the comparator output $y'(t)$ oscillates at a frequency of $F_S/2$. With the z^{-1} delay, $D(t)$ will be 1 unit in strength, $F_S/2$ in frequency, but 180° lagging from $y'(t)$. Meanwhile, $A(t)$, which is directly driven by $y'(t)$, will be in phase with $y'(t)$ but β-unit in strength. Consequently, $\mathrm{Sum}(t)$ will also be in phase with $y'(t)$ and $(\beta - 1)$ unit in strength. $\mathrm{Sum}(t)$ is then converted to the output current by the PMOS array and generates V_{OUT} with LCO at $F_S/2$ with 180° lagging. With an additional phase lag due to the output RC delay, V_{OUT} is sampled and compared with V_{REF}, and the comparator output $y'(t + T_S)$ coincides with $y'(t)$. With this feedback loop, the steady-state mode-1 LCO is maintained.

Note that, from Fig. 8, mode-1 LCO would also steadily exist when $\beta > 2$. Nevertheless, as the oscillation amplitude of $\mathrm{Sum}(t)$ is equal to $(\beta - 1)$ unit, the LCO amplitude increases with β. This is verified by simulations as in Fig. 9, where transient waveforms of V_{OUT} are plotted with β ranging from 2 to 5. In addition, note from (9), with larger β, the dc value of V_{OUT} would deviate more from V_{REF}. Thus, $\beta > 2$ is not preferred.

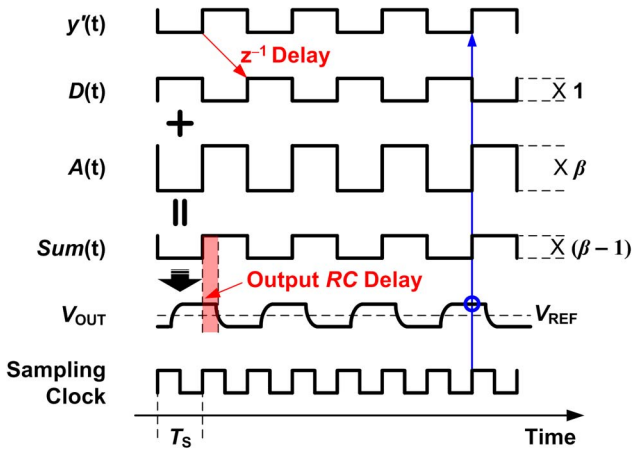

Fig. 8. Conceptual waveforms of a steady-state mode-1 LCO.

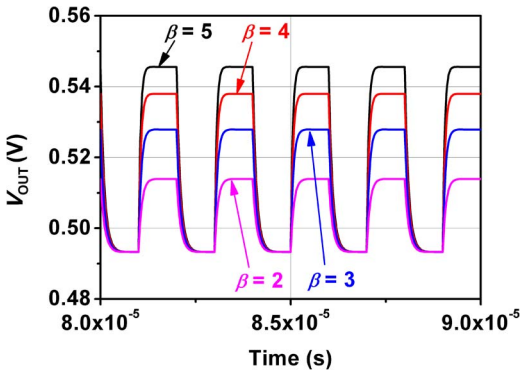

Fig. 9. SPICE simulation results of D-LDO with β value range from 2 to 5, 1-MHz sampling frequency, 1-mA load current, $V_{\rm IN} = 0.6$ V, and $V_{\rm REF} = 0.5$ V.

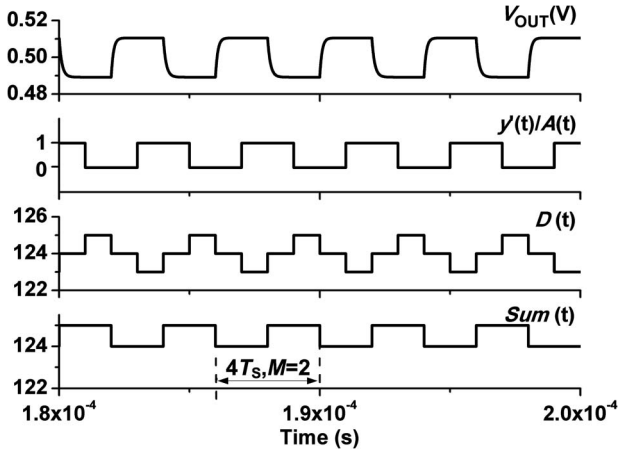

Fig. 10. SPICE simulation results of D-LDO in the $\beta = 1$ case, with 1-MHz F_S and 1-mA load current.

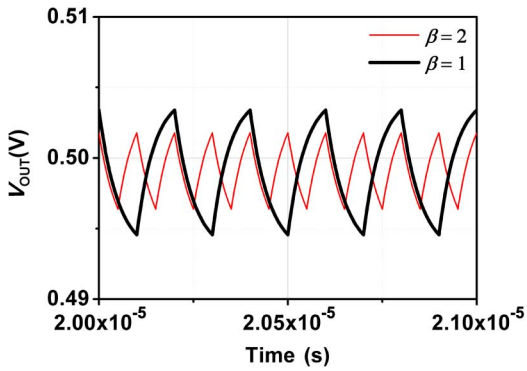

Fig. 11. SPICE-simulated $V_{\rm OUT}$ waveforms for $\beta = 1$ and 2 cases, with 20-MHz F_S and 1-mA load current.

For $\beta = 1$, a mode-2, rather than mode-1 LCO, is observed in both calculation and simulation. SPICE-simulated steady-state waveforms of the D-LDO with $\beta = 1$ are shown in Fig. 10. A mode-2 LCO, with Sum(t) oscillation amplitude equal to 1, can be steadily obtained with the combined $D(t)$ and $A(t)$. Consequently, with $\beta = 1$, a comparable LCO amplitude but with two times of the period is observed when compared with the $\beta = 2$ case, as long as F_S is below the output pole frequency. However, for F_S higher than the output pole frequency, the C_L will not be sufficiently charged or discharged in one clock period, and the longer LCO period incited by $\beta = 1$ will result in a larger LCO amplitude. Fig. 11 shows the simulated $V_{\rm OUT}$ waveforms with $\beta = 1$ and 2, with $F_S = 20$ MHz and load current $= 1$ mA. In this comparison, an approximately 50% reduction in LCO amplitude is achieved with $\beta = 2$.

For a theoretical analysis, the phase shift caused by $S'(z)$ can be calculated as

$$\theta_{S'} = -\tan^{-1}\frac{\cos\frac{\pi}{2M}}{(\beta-1)\sin\frac{\pi}{2M}}. \tag{10}$$

For $\beta \geq 2$ and $M = 1$, $\theta_{S'}$ adds an additional phase shift of π when comparing to θ_S in Table I, which makes $M = 1$ a solution of (7). Meanwhile, $M > 1$ is less likely to meet (7) because the τ/T_S term can be estimated to be much smaller than 1 at low F_S. This corroborates the mode-1 LCO existence for $\beta \geq 2$, which can be further verified by the numerical calculation given in Fig. 5(b) and the SPICE simulation shown in Fig. 9.

For $\beta = 1$, θ_S is a constant equal to $-\pi/2$ according to (10), regardless of the value of M. Therefore, (7) can be rewritten as

$$\varphi_{\rm LCO} = \frac{\pi}{2} - \tan^{-1}\frac{\pi}{M}\frac{\tau}{T_S}, \quad \varphi_{\rm LCO} \in \left(0, \frac{\pi}{M}\right). \tag{11}$$

Based on the aforementioned discussion on τ/T_S, only mode-1 and mode-2 can possibly be achieved for (11). However, Sum(t) will become 0 in mode-1 as shown in Fig. 8, indicating that a stable oscillation cannot be built up, and thus, only mode-2 is achievable in this case.

To sum up, $\beta = 2$ is selected based on two considerations. First, it outweighs the $\beta > 2$ cases by achieving lower LCO amplitudes and dc derivations. Second, when comparing to the $\beta = 1$ case, it shortens the LCO period and thereby reduces the LCO amplitude as well.

To further substantiate the proposed LCO reduction technique, the simulated LCO modes and amplitudes with load current from 1 to 20 mA are plotted in Fig. 12. Comparing to Fig. 5, the simulated cases coincide well with the calculated ones. Moreover, the simulated transient waveforms of $V_{\rm OUT}$ are shown in Fig. 13 with $\beta = 0$ and $\beta = 2$, with load currents of 0.5 and 20 mA, respectively. All of these results are simulated with $F_S = 1$ MHz, $V_{\rm IN} = 0.6$ V, and $V_{\rm REF} = 0.5$ V. Because of the LCO mode reduction from 3 to 1 with the proposed technique, the LCO amplitudes are reduced to at least one third of the original values. In particular, for the light load case of 0.5 mA, the LCO amplitude is reduced from 140 to 30 mV peak-to-peak.

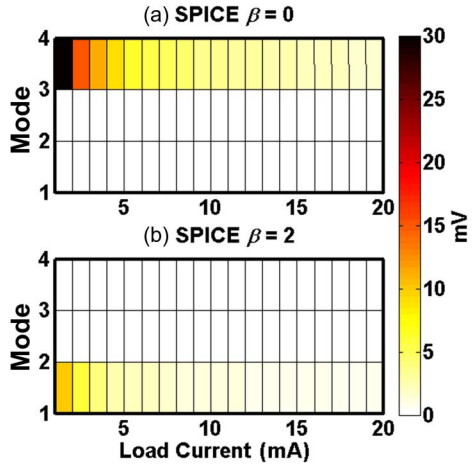

Fig. 12. SPICE-simulated LCO modes and amplitudes with load current range from 1 to 20 mA, with (a) $\beta = 0$ and (b) $\beta = 2$.

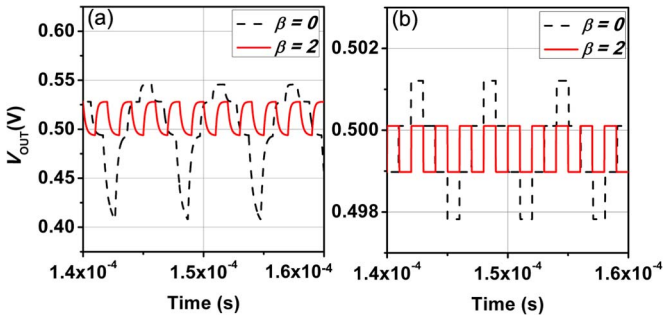

Fig. 13. Simulated results of the proposed D-LDO in $\beta = 0$ and 2 cases, with (a) 0.5- and (b) 20-mA load currents, at $F_S = 1$ MHz and $V_{\rm REF} = 0.5$ V.

IV. Comparison With the Dead-Zone Scheme

As introduced in Section I, a dead-zone scheme helps to eliminate LCO in a D-LDO. However, the resultant output steady-state dc error will be no smaller than the LCO amplitude with the proposed scheme, as discussed in the following.

Let the two consecutive control words that make $V_{\rm OUT}$ closest to $V_{\rm REF}$ be D_K and D_{K+1}. With the dead-zone operation, the D-LDO will stabilize to their corresponding output voltages $V_{\rm OUT}(D_K)$ or $V_{\rm OUT}(D_{K+1})$, depending on the initial condition. For the proposed scheme, once the LCO mode is set to 1, the digital control word will only oscillate between D_K and D_{K+1}. Thus, in the C_L sufficiently charged/discharged scenario, both output errors are either $|V_{\rm OUT}(D_{K+1}) - V_{\rm REF}|$ or $|V_{\rm OUT}(D_K) - V_{\rm REF}|$. However, for a higher F_S and an insufficient C_L charging/discharging time, the error of the proposed scheme will be smaller.

This can be verified in Fig. 14, where the $V_{\rm OUT}$ waveforms of the two D-LDOs with the dead-zone and proposed schemes are simulated with 1- and 10-MHz F_S, respectively. As predicted, the output error of the proposed scheme is significantly reduced with the increase of F_S.

Moreover, the dead-zone scheme not only increases the circuit complexity but also prevents the D-LDO from instant $V_{\rm OUT}$ error detection and consequently limits its transient response. Finally, the strong dependence on the design parameters, as well as the multiplicity of the comparator describing function [4], increases the difficulty of selecting the dead-zone window.

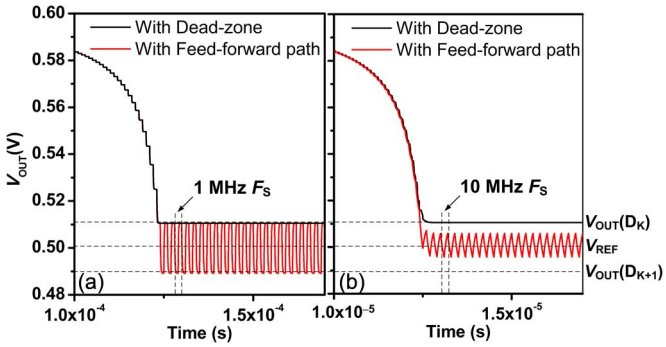

Fig. 14. Simulated $V_{\rm OUT}$ waveforms of the D-LDOs with either $\pm$20-mV dead-zone or $\beta = 2$ feedforward scheme, under $V_{\rm IN} = 0.6$ V, $V_{\rm REF} = 0.5$ V, $I_{\rm LOAD} = 1$ mA, (a) 1 MHz, and (b) 10 MHz F_S.

V. Conclusion

In this brief, the LCO occurrence in a D-LDO has been analyzed. The possible modes and amplitudes of LCO are calculated with MATLAB and substantiated by SPICE simulations. Based on the analysis, an LCO reduction technique has been proposed by inserting a feedforward path into the D-LDO loop. This technique enforces a mode-1 LCO and thus reduces the LCO amplitude. In a particular case, the LCO amplitude is reduced from 140 to 30 mV when the load current is 0.5 mA. In addition, this technique is implemented by adding only two auxiliary unit power transistors in parallel with the main PMOS array. Comparing with the dead-zone scheme, the proposed technique minimizes the D-LDO LCO with insignificant circuit complexity and design difficulty.

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