Transactions Briefs

Passive Noise Shaping in SAR ADC With Improved Efficiency

Yan Song, Chi-Hang Chan, Yan Zhu, Li Geng, Seng-Pan U, and Rui Paulo Martins

***Abstract*— This brief reports a passive noise-shaping (PNS) scheme for successive approximation register (SAR) analog-to-digital converter (ADC) based on the two-step integration with passive gain and comparator gain techniques. The analysis shows that the proposed method achieves a better noise-shaping (NS) efficiency than prior arts, which enhances the noise attenuation by 14 dB. A design example is provided which further adopts the delta-sampling technique to relieve the conversion efficiency loss due to the oversampling in the NS SAR ADC. The efficiency of the proposed PNS scheme and the performance of the ADC are verified by simulation achieving a 13.2 effective number of bits with a 10-b ADC architecture and eight conversion cycles for a signal bandwidth of 2 MHz sampled at 100 MS/s. The calculated Schreier figure of merit (FoM) and Walden FoM are 176.8 dB and 16 fJ/conv.-step, respectively.**

***Index Terms*— Analog-to-digital converter (ADC), delta sampling, oversampling, passive noise shaping (PNS), successive approximation register (SAR).**

I. Introduction

Energy-efficient applications, such as Internet-of-Things, wearable equipment, and wireless sensors require energy-efficient analog-to-digital converters (ADCs) with a resolution of at least 10 b and submegahertz input bandwidth (BW) [1]–[4]. Successive approximation register (SAR) ADCs are popular in these applications due to their simple structure and dynamic operation, leading to excellent energy efficiency (Walden FoM $<$ 10 fJ/conv.-step) [1], [2]. However, the achieved effective number of bits (ENOB) of the SAR ADCs are limited to 10 b where the thermal noise from the comparator dominates the performance [4]–[7]. Designs achieving high accuracy (ENOB $>$10 b) often need a low-noise preamplifier to suppress the input-referred noise of the comparator [4], [6] that consumes a large amount of static power. The figure of merit (FoM), in such cases, is larger than 30 fJ/conv.-step. Other types of designs can achieve both high resolution and high energy efficiency with oversampling techniques, but with limited BW ($<$20 kHz) [1], [2]. The aim of this brief is to improve the conversion accuracy to more than 13 b in medium-resolution SAR ADCs with megahertz input BW, while the conversion still maintains an excellent efficiency.

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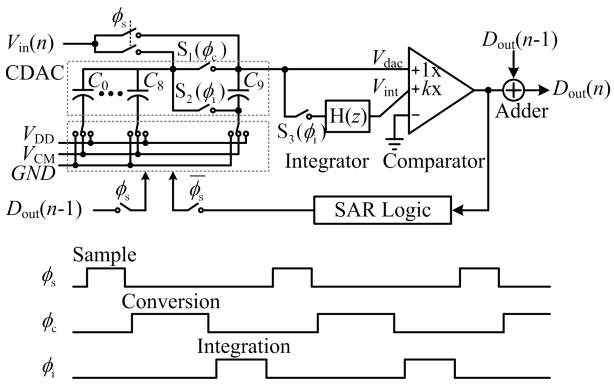


Fig. 1. Block diagram of the SAR ADC with PNS and its timing diagram.

To improve the resolution with reduced noise in the band of interest of the SAR ADC, oversampling [1], [2] and noise shaping (NS) [4], [5], [8] can be adopted. In [4], an active NS structure implemented with an amplifier based FIR-IIR filter exhibits good performance. However, the amplifier consumes static power and introduces extra noise. A passive NS structure was reported in [8], which uses only switched capacitors (SCs) to realize the NS. But, the proposed NS scheme has very weak integration effect of the residue voltage and limited performance. Other drawback of the existing NS SAR ADCs [8], [9] is the limited BW due to the large oversampling ratio (OSR).

In this brief, we propose a two-step integration procedure combining the passive gain from the digital-to-analog converter (DAC) and comparator to improve the NS efficiency. The efficiency of the proposed technique will be demonstrated with a design example in a 65-nm CMOS process. This brief extends the concept of the delta-sampling scheme [10] to enhance the conversion efficiency of the NS SAR ADC under oversampling.

II. NS SAR ADC Review

The NS technique is typically adopted to increase the conversion resolution. Such concept can be applied in the SAR architecture as presented in [4]. There are two key points to realize NS in the SAR ADC: 1) a full resolution residue voltage on the DAC capacitor array should be generated after each conversion; and 2) the residue voltage needs to be sampled and integrated, then fed back to the quantizer.

The SAR ADC with passive noise-shaping (PNS) scheme uses passive SC circuits to perform sampling and integration of the residue voltage, which avoids active amplifiers thus saving power. However, the charge-sharing effect in the SC circuits degrades the noise transfer function (NTF), limiting the efficiency of NS. It affects the NTF in two domains: 1) the voltage attenuation of the sampled residue voltage brings positive pole in the NTF; and 2) the weak integration effect leads to the zero of the NTF smaller than one. These two issues result in a high magnitude of the NTF at low

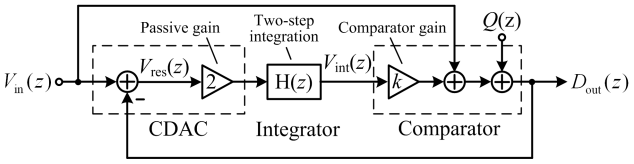


Fig. 2. Signal flow diagram of the PNS SAR ADC.

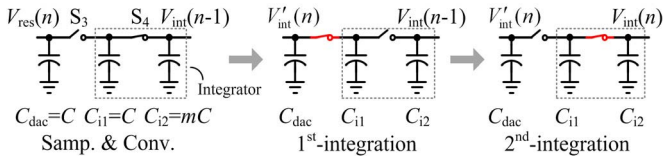


Fig. 3. Two-step integration process.

frequency, leading to a weak effect of noise attenuation in the signal band.

III. Proposed PNS SAR ADC

A. ADC Architecture

Fig. 1 shows the architecture of the proposed 10-b SAR ADC and its timing diagram. A single-ended structure is presented as an example, which mainly consists of a capacitive DAC (CDAC) array, a comparator, an adder, the integrator, and the SAR logic. In the sampling phase ($\Phi_s = 1$), the top plates of the CDAC capacitors are connected to the input, while the previous output code, $D_{\text{out}}(n-1)$, is applied to the bottom-plates of the CDAC capacitors. In this way, the difference voltage between the previous and current samples is acquired on the CDAC array, performing delta sampling. Meanwhile, S_1 opens during the sampling period to avoid the charge-injection effect. In the conversion phase ($\Phi_c = 1$), the SAR logic and the CDAC perform V_{cm}-based switching [11] for binary-search approximation of V_{dac}. At the end of the conversion, an extra switching of the unit capacitor (C_0) according to the LSB decision is added to get the full-resolution (10 b) residue [4]. During the integration phase ($\Phi_i = 1$), the residue voltage on the top plate of C_9 is passively boosted by 2, and transferred to the integrator through S_3. Afterward, the integrator executes a two-step passive integration. The integrated voltage V_{int} is then fed back to another positive input of the comparator. In the next conversion cycle, V_{int} is amplified k times at the comparator with sizing ratio between input pairs. Then, $k \times V_{\text{int}}$ and V_{dac} are summed in the current domain at the comparator who decides accordingly. The above operation processes introduce noise shaping and delta sampling in the SAR ADC, which improve the resolution and conversion efficiency. Fig. 2 shows the equivalent signal flow diagram of the proposed PNS SAR ADC, where $Q(z)$ represents the quantization error and D_{out} is the final output.

B. Proposed PNS Structure With High Efficiency

We propose a two-step integration method to enhance the efficiency of the passive integration. As Fig. 3 shows, the integrator consists of two capacitors, C_{i1} and C_{i2}, whose ratio is set as $1{:}m$. When the conversion finishes, the residue voltage of $V_{\text{res}}(n)$ is left on the top plate of C_{dac}, where C_{dac} is the equivalent capacitor of the CDAC array. $V_{\text{int}}(n-1)$ is the output voltage of the integrator in the previous cycle. In the first-integration step S_3 is closed. Supposing that C_{i1} is equal to C_{dac}, after the charge is redistributed on the top plates of C_{dac} and C_{i1}, the integrated voltage of the first step

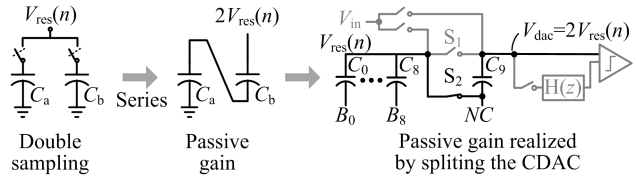


Fig. 4. Passive gain realized by the CDAC in the SAR ADC.

will become

$$V'_{\text{int}}(n) = \frac{1}{2}V_{\text{res}}(n) + \frac{1}{2}V_{\text{int}}(n-1). \tag{1}$$

Then, the second-integration process starts, with S_3 opened and S_4 closed. When the charge redistribution on the top plates of C_{i1} and C_{i2} ceases, the integrated voltage of the current cycle can be expressed as

$$V_{\text{int}}(n) = \frac{1}{2m+2}V_{\text{res}}(n) + \frac{2m+1}{2m+2}V_{\text{int}}(n-1). \tag{2}$$

Based on (2) and the signal flow diagram from Fig. 2, the transfer function of the SAR ADC will be obtained as

$$D_{\text{out}}(z) = V_{\text{in}}(z) + \left(1 - \frac{2m+1}{2m+2}z^{-1}\right) \Big/ \left(1 - \frac{m}{m+1}z^{-1}\right) \cdot Q(z). \tag{3}$$

From (3) we can derive that with the help of the two-step integration method, we realize a NTF containing a zero closer to one when m becomes large. However, due to the charge-sharing effect, $V_{\text{res}}(n)$ is attenuated by $1/(2m+2)$ as (2) shows, which induces a positive pole in the NTF and degrades the NS efficiency.

The pole of the NTF can be moved closer to zero by compensating the voltage attenuation of $V_{\text{res}}(n)$, where the passive gain method is then adopted [7]. Fig. 4 shows the passive gain generated in the CDAC of the SAR ADC. The basic idea is double-sampling the voltage of $V_{\text{res}}(n)$ into two capacitors C_a and C_b, as Fig. 4 shows. Then, the two capacitors are connected in series and the voltage on the top plate of C_b is amplified to $2V_{\text{res}}(n)$, thus achieving a gain of 2. Based on this concept, we add two switches (S_1 and S_2) in the CDAC of the SAR ADC. Then, the CDAC is separated into two parts with the same capacitance, C_9 and C_{8-0}. After the conversion, $V_{\text{res}}(n)$ is left on the top plates of C_9 and C_{8-0}, then S_1 opens and S_2 closes to boost the top plate voltage of C_9 to $2V_{\text{res}}(n)$ due to the series connection. Then, the boosted voltage is later transferred to the integrator in the integration phase. Considering the passive gain, the attenuation factor of $V_{\text{res}}(n)$ in (2) is improved to $1/(m+1)$. Combining the two-step integration and the passive gain techniques, the transfer function of the SAR ADC is

$$D_{\text{out}}(z) = V_{\text{in}}(z) + \left(1 - \frac{2m+1}{2m+2}z^{-1}\right) \Big/ \left(1 - \frac{2m-1}{2m+2}z^{-1}\right) \cdot Q(z). \tag{4}$$

The positive pole of the NTF in (4) is closer to zero than that in (3), resulting in a better suppression of $Q(z)$ at low frequency.

To further compensate the attenuation of $V_{\text{res}}(n)$, we adopt the comparator gain technique [9]. Fig. 5 shows the circuit schematic of the adopted comparator [4]. By sizing the input transistor of V_{int} path k times larger than that of the V_{dac} path, we achieve an equivalent gain ratio of $k:1$ between the input voltages of the two paths. It is proven in [9] that the comparator gain can only compensate for the attenuation of $V_{\text{res}}(n)$ and not the $V_{\text{int}}(n)$ loss. Thus, if we choose $k = m+1$, the attenuation factor of $V_{\text{res}}(n)$ in (2) can be fully compensated. With this configuration, the transfer function of the

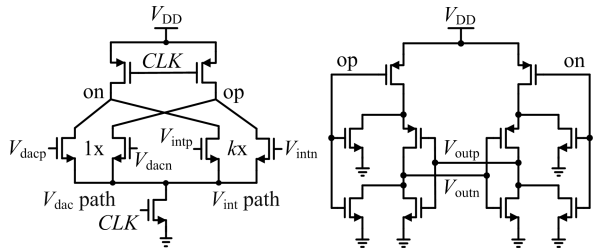


Fig. 5. Comparator schematic.

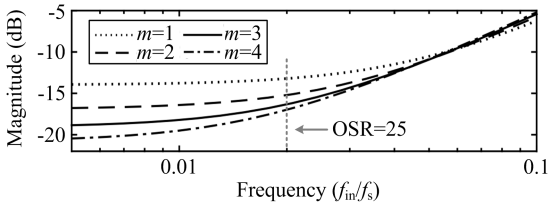


Fig. 6. Proposed NTF versus different m.

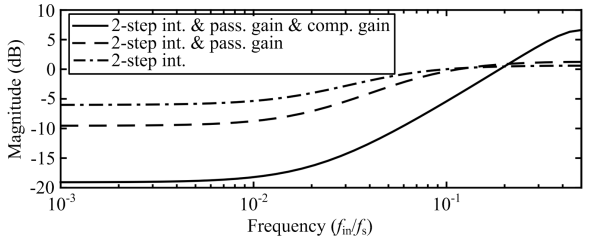


Fig. 7. Bode-diagrams of the NTFs with different techniques when $m = 3$.

SAR ADC is

$$D_{\text{out}}(z) = V_{\text{in}}(z) + \left(1 - \frac{2m+1}{2m+2}z^{-1}\right) \Big/ \left(1 + \frac{1}{2m+2}z^{-1}\right) \cdot Q(z). \tag{5}$$

In (5), the pole of the NTF is negative, which helps to improve the noise attenuation at low frequency.

It is worth to note that, similar to the conventional SAR ADC, the comparator offset does not affect the linearity and the NTF of the NS SAR ADC. According to simulation, 1σ comparator offset voltage is 4 mV. Thus, we reduce the input amplitude by 0.2 dB guaranteeing that the ADC will not saturate due to the comparator offset. Moreover, the NS effect in our design can be easily modified by configuring the capacitance ratio of C_{i1} and C_{i2}, corresponding to the value of m. Fig. 6 shows the bode diagrams of the NTF expressed in (5) with $m = 1 - 4$. The NTF has a lower magnitude at low frequency (OSR $= 25$) when m has a larger value. Thus, a better noise-shaping effect can be achieved. However, when m gets larger, the comparator gain ($k = m + 1$) of the integration path increases. The additional thermal noise introduced in the integration path from the DAC capacitors (C_{i1}, and C_{i2}) is also amplified k times in the comparator. Since these thermal noises cannot be shaped [4], [9], they greatly affect the signal-to-noise-and-distortion ratio (SNDR) of the ADC, as shown later through simulation. Furthermore, a larger k leads to larger power dissipation in the comparator, which degrades the power efficiency. In fact, the comparator gain is expected to be as small as possible in the PNS SAR ADC. Based on the above, we adopt the passive gain method to relax the comparator gain by two.

Fig. 7 shows the bode diagrams of the NTFs in (3)–(5) when $m = 3$. From Fig. 7 we can infer that the NS with the two-step integration method achieves a noise attenuation of 6 dB at low frequency. While combining the passive gain method, the noise attenuation is improved by 4 dB. Further by adopting the comparator gain method, 8 dB more attenuation of the noise is achieved. Finally, the NTF has a magnitude of -18 dB at low frequency.

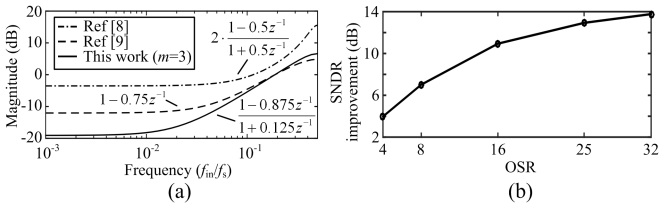


Fig. 8. (a) Bode-diagrams comparison of the NTFs in this brief and other related works. (b) SNDR improvement when compared with [8].

C. Comparison With Other State-of-the-Art Works

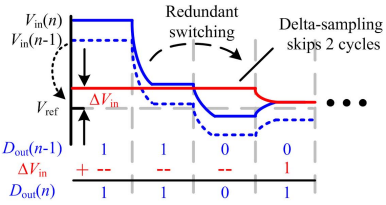
Since the PNS SAR ADC proposed in [8] does not need any operational transconductance amplifier, it can achieve low power. However, it imposes a weak integration effect, leading to a zero located at 0.5 of the NTF. As a result, the noise attenuation in the signal band is small. In [9], two capacitors are added in the integration path. One capacitor samples the V_{res} from the DAC array first, and then it is connected to the other for integration. With this method, the zero of the NTF in [9] improves to 0.75. However, the first capacitor, performing V_{res} sampling, is reset after each conversion cycle, thus partially losing the integrated voltage held from the previous cycle. This reset process degrades the integration effect and the NS efficiency.

In our design, the capacitors C_{i1} and C_{i2} in the integration path will not reset during the whole conversion cycle. C_{i1} performs V_{res} sampling while holding half of the integrated voltage of the previous cycle, as presented in (1). Then the mixed voltage is transferred to C_{i2} for the following integration process. The two-step integration method prevents much V_{int} loss due to the charge sharing, resulting in a better integration effect. Compared to [9], our design achieves a NTF with a zero closer to one. Moreover, the passive gain generated by the DAC capacitors avoids a large gain provided by the comparator, which saves power and reduces the noise from the comparator. Fig. 8(a) shows the NTF of the proposed method with $m = 3$, which achieves a magnitude of 14 dB lower than that in [8] at low frequency. Fig. 8(b) shows the SNDR improvement of this design when compared with [8] at different OSRs. The SNDR improvement becomes even more significant for larger OSRs.

The extra capacitors for the integration induce area overhead in the passive NS SAR ADCs. In [8] and [9], extra capacitors of $2C_{\text{dac}}$ and $4/3C_{\text{dac}}$ are required, respectively, to perform the passive integration, where C_{dac} represents the capacitance of the CDAC, while in our design only $1C_{\text{dac}}$ is added in the passive integrator when $m = 3$. In [4], although the active amplifier is used, the kT/C noise from the capacitor in the integrator still cannot be shaped. To keep the noise in accordance with the desired resolution of the ADC, the capacitor size should not be smaller than $1C_{\text{dac}}$, as stated in [4].

IV. Delta Sampling Improving Conversion Efficiency

With the oversampling, the input variation of the SAR ADC is small between two adjacent samples, like $V_{\text{in}}(n-1)$ and $V_{\text{in}}(n)$, as shown in Fig. 9. The energy is wasted due to the redundant leading bits conversion in conventional SA approach. In [12], prediction logic is designed to improve the conversion efficiency. However, a redundant bit is needed in the SAR ADC to tolerate the error between the predicted and the real output codes. In our design,



OSR v.s. required bits and power reduction

OSR	Required bits	Normalized power
1	10	1
2–5	9	0.86
6–12	8	0.73
13–25	7	0.62
26-50	6	0.52

Fig. 9. Principle of the delta-sampling scheme, and the saving of bits and power reduction versus OSR with delta sampling in the SAR ADC.

only the difference between two adjacent samples (ΔV_{in}) is acquired and resolved to reduce the switching steps based on the delta-sampling method, thus saving the power drawn from the CDAC switching, comparator, and logic circuits. Meanwhile, no redundant bit is necessary.

We utilize the structure of an SAR ADC, which consists of a CDAC, a comparator and the control logic. By simply adding a memory array, an adder, and modifying the switching logic, the delta sampling can be realized. The number of switching steps is determined by the maximum input variation, ensuring that ΔV_{in} can be resolved with the LSBs. For a full-scale sinusoidal input, the maximum variation is related with the OSR. Thus, the relationship between the OSR and the required switching steps can be calculated, as summarized in Fig. 9. It also shows the estimated power reduction based on the approach from [10].

From Fig. 8(b), it can be recognized that the SNDR has a relatively small improvement ($\sim$ 3 dB) when the OSR is above 25. Therefore, we select OSR $=$ 25. With the help of the delta-sampling method, this design needs only eight clock cycles (seven cycles of conversion and one cycle of integration) in one conversion, while the ADC in [8] and [9] need 12 clock cycles (ten cycles of conversion and two cycles of integration) and 13 clock cycles (11 cycles of conversion and two cycles of integration), respectively, under the same 10-b SAR ADC structure. Consequently, the conversion efficiency of the proposed SAR ADC can be significantly improved.

V. Simulation Results

This design was implemented in 65-nm CMOS technology. The supply voltage is set to 1 V. The CDAC is a binary-weighted capacitor array and its total capacitance in each half is 1 pF. The transistor-level simulations without and with transient noise have been carried out to verify the performance of the proposed PNS SAR ADC. To model the parasitic effects, we added 10% and 20% top plate and bottom-plate parasitics to all the capacitors, respectively.

Fig. 10 shows the simulated SNDR with Monte Carlo (MC) and corner analysis of the proposed NS SAR ADC when $m = 3$ and OSR $= 25$. The simulations without transient noise verify the shaping effect of the quantization noise floor of the proposed NS structure. The results show that the SNDR is around 90 dB and does not vary much. They are close to the theoretical SNDR of 94 dB. The simulations with transient noise exhibit the SNDR limitation around 82 dB due to the thermal noise in the SAR ADC. The capacitor mismatch of the CDAC is omitted in the above simulations in order to show the effectiveness of the shaping in our scheme. When taking the capacitor mismatch into account, the worst case SNDR is limited at around 80 dB which is close to the noise level of this design.

Fig. 11 shows the simulated SNDR of the SAR ADC under different OSRs and m with transient noise. In Fig. 11(a), when the OSR is larger than 25, the SNDR increases about 3 dB with 2$\times$ OSR which implies the NS has a weak effect on improving the SNDR and only the oversampling contributes to the difference. Thus, an OSR of 25 is suitable for this design. In Fig. 11(b), the additional

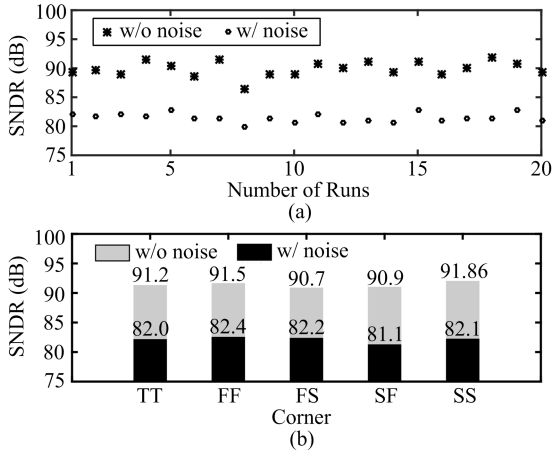


Fig. 10. SNDR spread of (a) MC and (b) corner simulations of the NS SAR ADC ($m = 3$ and OSR $= 25$) with and without transient noise at 100 MS/s.

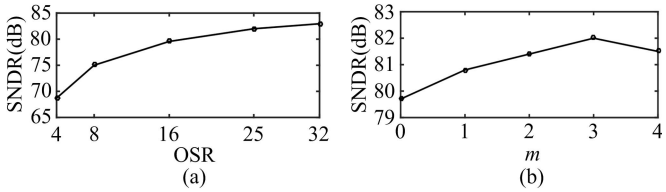


Fig. 11. Simulated SNDR of the NS SAR ADC under different (a) OSR and (b) m with transient noise.

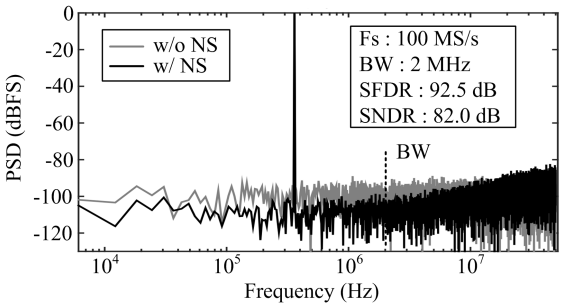


Fig. 12. Simulated (a) PSD and (b) differential nonlinearity and integral nonlinearity of the proposed PNS SAR ADC.

unshaped thermal noise from the integration path is larger than the NTF magnitude improvement at $m \geq 4$, as discussed in Section III-B. Therefore, the SNDR drops. Thus, $m = 3$ is suitable here. With this configuration, the additional thermal noise from the integration path limits the SNDR of the ADC to 82 dB.

Fig. 12 shows the simulated 16384-point fast Fourier transform spectrum of the ADC with a 360-kHz input signal at 100 MS/s and $m = 3$. The ADC has a full-scale input range of 1 V_{pp}. The signal BW is 2 MHz with an OSR of 25. The ADC achieves a SNDR of 82 dB equivalent to an ENOB of 13.3 b. The proposed PNS SAR ADC allows a conventional 10-bit SAR ADC to achieve an additional 3 b of resolution. Fig. 13 shows the simulated SNDR versus the input amplitude and input frequency. When the input frequency is near the BW (2 MHz), the simulated SNDR is 81.3 dB. The power consumption of the SAR ADC is 561 μW at 100 MS/s and 1 V supply with 2-MHz input frequency. The analog circuits, including the sampling front-end, the CDAC and the comparator, consume 240 μW. The digital circuit consumes 321 μW. Also, according to the simulation if the design does not utilize the delta-sampling

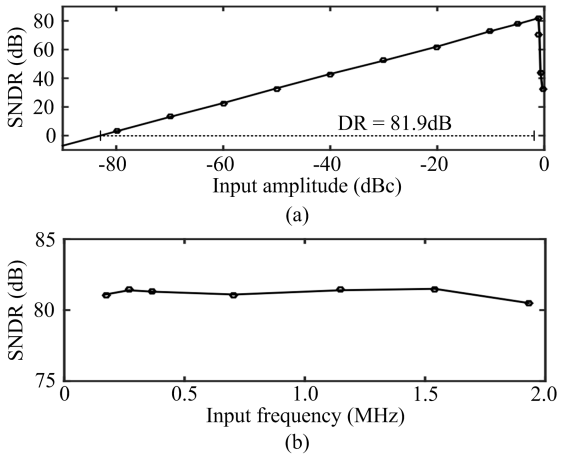


Fig. 13. Simulated SNDR versus (a) input amplitude and (b) input frequency.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Specification	VLSI'15 [8]*	ESSCIRC'16 [9]*	VLSI'17 [13]*	This Work**
Architecture	PNS SAR	PNS SAR	PNS SAR	PNS SAR
Technology (nm)	65	130	40	65
Supply (V)	0.8	1.2	1.1	1
Bandwidth (MHz)	6.25	0.125	0.262	2
ENOB (bit)	9.35	12.0	13.0	13.2
Power (μW)	120.7	61	143	561
FOM_W (fJ/conv)	14.8	59.6	33.3	16.0
FOM_S (dB)	165.2	167.1	173.0	176.8

* Measurement results ** Simulation results

scheme, the power consumption is 748 μW. The calculated FoMs are 176.8 dB, which shows a superior performance to previous passive NS SAR ADCs [4], [8], [9]. The performance comparison with previous related works is presented in Table I.

VI. CONCLUSION

This brief proposed an improved PNS structure in an SAR ADC. The presented two-step integration method, combined with the passive gain and the comparator gain techniques, achieves a better NS efficiency when compared with the prior arts. Meanwhile, we adopted the delta-sampling technique to reduce the drawback of a large OSR in the NS SAR ADC, improving the conversion and energy efficiency. A design example of the PNS SAR ADC has also been presented, which confirmed the effectiveness of the proposed solutions.

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