A Fully Integrated LDO With 50-mV Dropout for Power Efficiency Optimization

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***Abstract*—This brief presents, a fully integrated low-dropout regulator (LDO) with 50-mV dropout voltage for high power efficiency, with a LDO-self-supplied differential error amplifier (EA) for higher power supply rejection (PSR), and a coupled transient enhancement unit for fast transient response. With 50-mV dropout voltage, the LDO can achieve 94.4% power efficiency in the full load condition. The LDO is fabricated in a standard 28-nm bulk CMOS process with 0.0086-mm^2 active area. It features a 288-MHz unity-gain bandwidth (UGB) at 20-mA load current, while consuming a quiescent current of 33 μA. With such high bandwidth and the coupled transient enhancement unit, the proposed LDO achieves 270-ps response time for a 0-to-20-mA load transient with 100-ps edge time. The self-supplied EA helps to achieve a PSR of −30 dB even with only 50-mV dropout. The ultra-fast response, small area, and high efficiency features make the proposed LDO very suitable for working as distributed point-of-load regulators in a digital system.**

***Index Terms*—Low-dropout regulator, output-capacitor-free, high power efficiency, ultra-fast response.**

I. Introduction

THE VERY large-scale integrated (VLSI) circuits need fully-integrated power management unit (PMU) to optimize the power efficiency and to reduce printed circuit board (PCB) area and design cost. One of the primary goals of the PMU is to provide high-quality power supplies to the integrated circuits with the minimal power losses. Analog units need a high power-supply-rejection (PSR) regulator, while digital units need an ultra-fast transient response regulator [1]. So, a PMU usually uses various combinations of the topologies like linear regulators, inductive and capacitive dc-dc converters to satisfy different applications. Usually, the linear regulators have certain dropout voltage, and its power efficiency degrades significantly when the output voltage largely different from the input voltage. Fig. 1 shows the LDO power efficiency versus load current with different quiescent current I_Q and dropout voltages. Previous LDO designs mainly focused on the current efficiency optimization with low quiescent current [2]–[4], which is good for longer standby time within one battery charging period. In this brief, we try to maximize the power efficiency instead of the current efficiency and propose an LDO with only 50-mV dropout voltage.

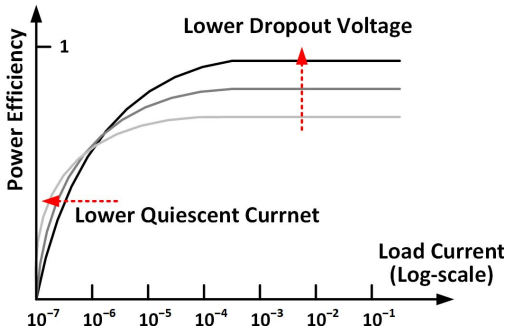

Fig. 1. The LDO power efficiency versus load current with different quiescent currents and dropout voltages.

For low-voltage high-performance digital circuits, the regulator need to have both high PSR and fast transient response. In microprocessors, for example, its maximum clock frequency is determined by the most critical path. So a large voltage droop during transient will limits its operating frequency. And the supply noise will also affect the clock timing of the microprocessor [5]. Therefore, in addition to high power efficiency, we need an ultra-fast transient solution. To get a fast transient response, many topologies and techniques have been proposed in the past decade. The LDO based on replica-biased flipped voltage follower (FVF) [6] has demonstrated an ultra-fast load regulation, but with a low current efficiency of 94%. Also, its load regulation is limited by the output impedance of the replica-biased output stage. Therefore, [6] used a distributed dual-loop architecture to get better DC accuracy, which required additional current consumption.

When the biasing current is in the deep-sub-mA range and the load current is in the mA range, the dropout voltage is the key factor that influences power efficiency. A smaller dropout voltage also means a smaller drain-to-source voltage V_{DS} of the power transistor. Therefore, a larger transistor size is required for the same output current. Also, a smaller V_{DS} means the power transistor will operate more likely in the linear region which decreases the gain and thus the PSR. Most of the previous papers designed the LDOs with 150-mV to 300-mV dropout voltages for a decent PSR. So, when we tradeoff dropout voltage for power efficiency, these are the

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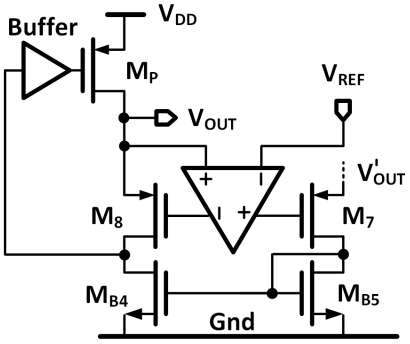

Fig. 2. Basic structure of the proposed ultra-fast 50-mV dropout regulator.

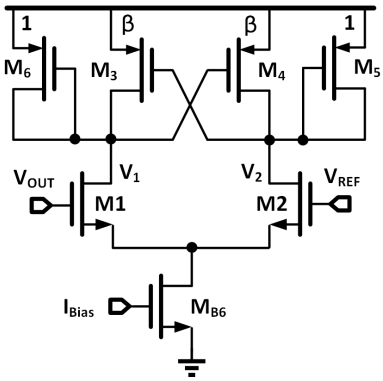

Fig. 3. The structure of the gain boost stage with cross-coupled pair.

design challenges that we are going to solve in our 50-mV dropout LDO design.

The rest of this brief is organized as follows. Section II introduces the circuit implementation of our proposed LDO. Section III analyzes the stability issues. The measurement results are given in Section IV. And Section V draws the conclusions.

II. Implementation of the Proposed Scheme

Fig. 2 shows the basic structure of this brief. As the FVF-based loop has a low gain, especially in the 50-mV dropout condition, we use an LDO-self-supplied differential amplifier to regulate V_{OUT} through the gate of M8 as well. In addition, we use the current mirror MB4 and MB5, which set the bias current for the FVF stage, to further regulate the output.

A. The Main Loop of the Proposed LDO

As shown in the Fig. 2, the main loop of the proposed LDO uses the flipped-voltage-follower (FVF) structure. In the FVF structure, M8 works as a common-gate stage together with the super source follower and the power stage, it can generate a high-bandwidth but a medium-low-gain loop. Meanwhile, the gates of M8 and MB4 are independent from the main loop of the FVF-based LDO, which means more design freedom to add auxiliary loop(s) to enhance the DC gain and transient response speed.

The current of a PMOS which working in the linear region can be expressed as

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}V_{od}V_{DS}, \tag{1}$$

where μ_p is the mobility of charge carriers, C_{ox} is the gate-oxide capacitance, V_{od} is the overdrive voltage of the PMOS, V_{DS} is the drain-source voltage. The output current is proportional to the V_{DS} under certain overdrive voltage and transistor size. When reducing the dropout voltage, the LDO need to enlarge the size of the power PMOS to maintain the output current capability, which will introduce more parasitic capacitance to the gate of the power PMOS.

To restrain the output voltage variation during ultra-fast load transient edge times, like sub-ns, the driving stage which connects the pass transistor should have a high slew rate, and the control loop should have a wide bandwidth. However, the parasitic capacitance on the gate of the pass transistor will decrease the slew rate and bandwidth. To deal with this drawback, previous works mostly used source follower [7] or current buffer [2]. While, the proposed LDO uses the super source follower (SSF) [8] which uses a local shunt feedback unit to dramatically reduce the output impedance. In this brief, about total 30% of the biasing current budget has been allocated to the SSF for pushing the pole on the gate of the pass transistor to high frequency. But the LDO only with the SSF is still not good enough to handle the ultra-fast load transients, especially in some high-performance applications that the load current may jump from zero to the full load in sub-ns time scale. Therefore, the proposed circuit uses a dynamic biasing to accelerate the regulation speed, which will be discussed in Section II-D.

As mentioned above, reducing the dropout voltage is also of concern for the DC gain consideration. The gain of the power stage can be expressed as

$$\begin{aligned} A_P &= g_{m,linear}R_{OUT} \\ &\approx \mu_n C_{ox}\frac{W}{L}V_{DS}\Big/\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) \\ &= V_{DS}/V_{GS}-V_{TH}, \end{aligned} \tag{2}$$

where $g_{m,linear}$ is the transconductance of the PMOS working in the linear region. As the V_{DS} in our design is only 50 mV, most likely is smaller than V_{GS}-V_{TH}, indicating that the A_P is smaller than one. Notice that this problem does not exist for normal 200-mV dropout regulators, of which the power stage can provide about 20 dB gain for the control loop. To alleviate the low loop gain issue, a gain boost stage is added in the proposed LDO, as shown in the Fig. 2, and is going to be discussed in the next sub-section.

B. The Gain Boost Stage

As shown in Fig. 3, the gain boost stage uses a single stage differential amplifier with a cross-coupled PMOS pair [10] to increase the gain. The cross-coupled pair generates a negative resistance which can counteract the equivalent resistance of the diode-connected transistors M6 and M5. It can effectively increase the resistance of the internal nodes V_1 and V_2. The size ratio of the transistors pairs (M3, M4) and (M6, M5) is set as $1:\beta$, where the β is smaller than 1 to maintain it works as an amplifier not a hysteresis comparator, considering the random mismatch during fabrication. If β is larger than 1, which means the negative resistance has over-compensated, and then this stage will be a latched comparator.

With the help of the cross-coupled pair, the gain is boosted by a factor of $((1+\beta)g_m + g_{ds})/((1-\beta)g_m + g_{ds})$, compared to the differential amplifier without a cross-coupled pair, where g_m is the transconductance of the M3, M4, and g_{ds} is the total output conductance of the node V_1 or V_2. The gain boost stage with cross-coupled pair operates with the same

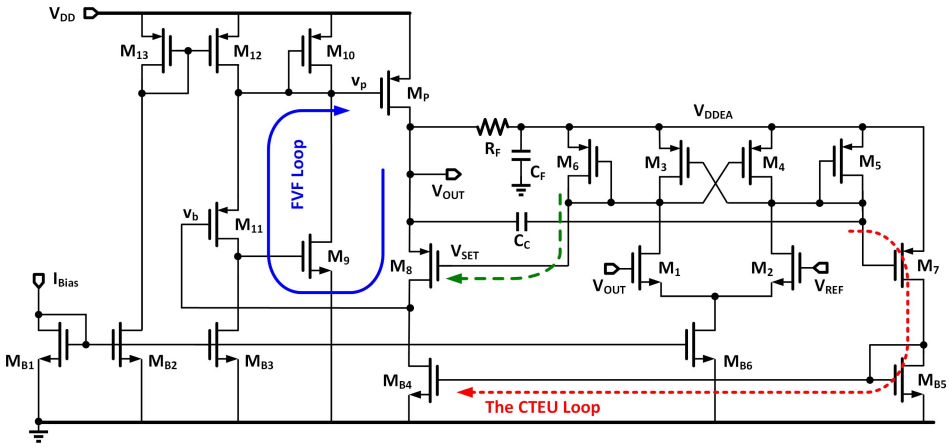

Fig. 4. Full schematic of the proposed LDO.

bias current, such that enhances the gain without increasing current consumption.

C. Self-Supplied Differential EA

Fig. 4 shows the full schematic of the proposed LDO design. As the gain boost stage is regulating the output voltage through M8 and MB4, which are located at the low-side of the regulator. We use the LDO output itself to supply the gain boost stage. From the V_{SET}-V_{OUT} point of view, M8 operates as a source follower, therefore, the gate of M8 (V_{SET}) should be clean. MB4 serves as NMOS current source, of which the gate should also be referred to ground. In other words, the gates of M8 and MB4 should be shielded from the supply noise for higher PSR. That can prevent the PSR degradation above the corner frequency of the auxiliary amplifier. A low pass filter formed by $R_F = 50\Omega$ and $C_F = 3$pF is added to generate a dedicated clean V_{DDEA}. Since the EA only consumes μA-level quiescent current, the size of C_F can be small while the value of R_F can be large.

D. Coupled Transient Enhancement Unit (CTEU)

The SSF uses local shunt feedback to decrease the output impedance. The shunt feedback is realized with a pull-down path which means the buffer can pull down the gate voltage of the pass transistor M_P fast during the light-to-heavy load transition. Meanwhile, the other stages also need high pull-down speed to match the speed of the buffer stage. In the prior works, the pull-down speed of node V_b is determined by the fixed current source of the MB4. For high-speed pull-down operation, MB4 needs more biasing current which is unfavorable for a low quiescent current design. Therefore, the CTEU is added in the proposed LDO to further improve the transient performance, as shown in Fig. 4.

The CTEU utilizes the dynamic biasing scheme which has better performance than the adaptive biasing scheme in terms of current efficiency and response speed. The dynamic biasing can boost the bias current and thus the response speed instantaneously when the load transient happens. On the other hand, the adaptive biasing scheme changes the bias current accordingly to the load condition. Therefore, the adaptive biasing scheme has a small bias current and low bandwidth in light load condition, which mainly improves the loop stability and the heavy-load PSR, but has no improvement on transient response speed.

Adding an extra branch to the circuit would consume the limited current budget, so that the proposed CTEU only reuses a coupling capacitor C_C which also works as a compensation capacitor in the auxiliary loop. From the small-signal point of view, the cap C_C contributes a left half-plane (LHP) pole P_2 and a LHP zero Z_0 to the control loop. And the Z_0 is one of the two zeros in the control loop, which is the key factor to cancel the non-dominant poles. Meanwhile, for large signal, when there is a load transient, the output variation will be coupled through C_C to the gate of M7. The M7 stage is a common source amplifier, and it will amplify the transient signal to the gate of MB4. If there is an undershoot at the output, MB4 will pull down the voltage of the node V_b. And then the buffer will pull down the gate voltage of the M_p to increase the output current to stop the V_{OUT} dropping. The transfer function of the CTEU loop is given by:

$$\mathrm{H_{CTEU}} = \frac{C_C s}{C_C s + g_{ds5} + g_{m5}} \mathrm{A_1 A_b A_p}, \tag{3}$$

$$\mathrm{A_1} = g_{m7}\left(r_{o7}||r_{ob5}||\frac{1}{g_{mb5}}\right) g_{mb4}(r_{ob4}||r_{o8}), \tag{4}$$

$$\mathrm{A_b} = \frac{g_{\mathrm{m11}}(g_{\mathrm{dsb3}} + g_{\mathrm{m9}})}{2g_{\mathrm{ds10}}g_{\mathrm{ds11}} + g_{\mathrm{m11}}(g_{\mathrm{dsb3}} + g_{\mathrm{m9}}) + g_{\mathrm{ds11}}g_{\mathrm{T}}} \approx 1, \tag{5}$$

$$g_{\mathrm{T}} = 2g_{\mathrm{ds12}} + 2g_{\mathrm{ds9}} + g_{\mathrm{dsb3}} + 2g_{\mathrm{m10}} + g_{\mathrm{m9}}, \tag{6}$$

$$A_P(s) = \frac{g_{mP}(R_{oP}||R_L)}{1 + sC_L(R_{oP}||R_L)}. \tag{7}$$

Here, $\mathrm{A_1}$ is the gain of the M7 stage plus the MB4 stage. And $\mathrm{A_b}$ is the gain of the SSF. Then, for simplicity, we assume that the $\mathrm{A_b} \approx 1$. Obviously, the equation (3) shows that the CTEU path is a highpass loop.

$$A_v(s) = \frac{g_{mp}(r_{o8}||r_{oB4})R_1 R_O\left[(1 + C_F R_F s)(G_{m2} + G_{m3}g_{m1}r_6 + (G_{m2} + G_{m3})r_6 C_C s)\right]}{r_6(g_{m1} + C_C s)(1 + C_1 R_1 s)(1 + C_O R_O s + C_F s(R_F + R_O + C_O R_O R_F s))} \tag{8}$$

$$R_1 = (g_{dsB3} + g_{ds11})/\left[g_{ds11}(g_{dst} + g_{m9}) + g_{m9}g_{m11} + g_{dsB3}(g_{ds11} + g_{dst} + g_{m11})\right] \tag{9}$$

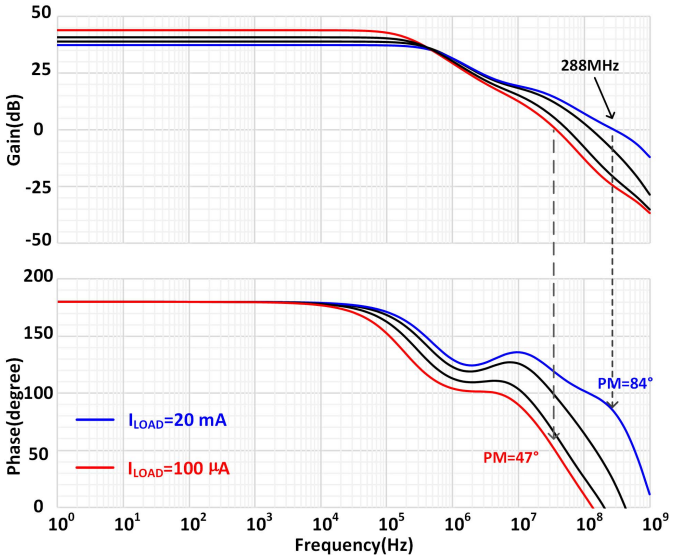

Fig. 5. Simulated Bode plot of the LDO with V_{IN} = 0.9V, and V_{OUT} = 0.85 V.

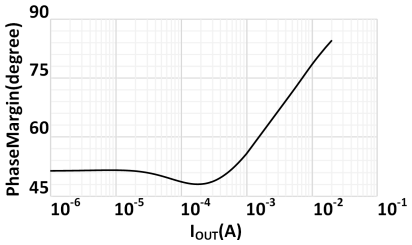

Fig. 6. Simulated phase margin versus output current of the LDO.

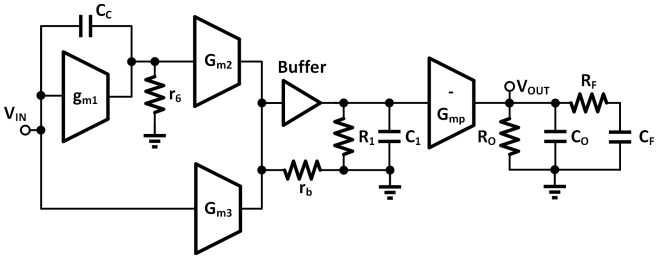

Fig. 7. Simplified small-signal model.

III. Stability Analysis

Fig. 7 shows the small-signal model of the proposed LDO which consists of three feedback loops. As we use 50-mV dropout voltage to increase the power efficiency, the gain of the power stage suffers from operating in the linear region, especially in the medium-to-heavy load range. In light load condition, the power transistor works in subthreshold region and gives higher output impedance, which contributes relatively more gain to the FVF loop. The increased impedance on the output node will lower the output pole P_{Out}, making it as the dominant pole in the light load condition. In the medium-to-heavy load conditions, the pole on the gate of transistor M7(P_{M7}) serves as the dominant pole, to enable higher output current without using large load capacitor.

Fig. 5 shows the simulated bode plots in different loading conditions. The loop gain at 100-µA load current is 5 dB higher than the 1-mA load current situation. When the load changes, P_{Out} will move toward P_{M7}, which needs extra compensation technique to keep the loop being stability.

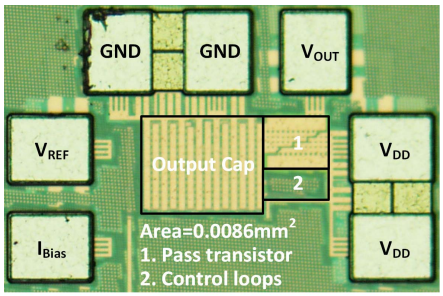

Fig. 8. Micrograph of the fabricated prototype.

The signal paths in the circuits have two parts. FVF loop is the main loop, which utilized the FVF structure to form an ultra-fast low-gain loop. The gain boost path contains the EA and the proposed compensation circuits. The capacitor C_F works as decoupling cap and the compensation cap at the same time. The transfer function of the entire LDO is given by equation (8), at the bottom of the previous page. There are four LHP poles, including two alternative dominant poles are $P_{M7} = 1/(2\pi r_6 C_C)$ and $P_{Out} = 1/(2\pi R_O C_O)$. And there are two LHP zeros in the overall control loop, while the zeros are generated by the capacitors C_C and C_F. The two zeros compensate the phase and make the entire control loop stable in all loading conditions. In the transfer function,

$$G_{m2} = g_{m7} g_{mB4} (r_{o7} || r_{oB5} || \frac{1}{g_{mB5}}), \tag{10}$$

$$G_{m3} = g_{m8}(1 + g_{m1}(r_{o1} || r_{o6} || r_{o3})), \tag{11}$$

$$r_6 = r_{o6} || r_{o3} || r_{o1}, \tag{12}$$

$$g_{dst} = g_{m10} + g_{ds10} + g_{ds9} + g_{ds12}. \tag{13}$$

In the I_{LOAD} = 100 µA condition (the red lines), the pass transistor works in the subthreshold region and the P_{Out} is the dominant pole, while the control loop has 44-dB DC gain with a phase margin of 47°. The blue line is the full load condition with I_{LOAD} = 20 mA. In this condition, the pass transistor works in the linear region and the P_{M7} is the dominant pole, with a DC gain of 38 dB and a phase margin of 84°. The phase margin versus output current is shown in the Fig. 6. This pole exchange scheme combines the advantages of the both P_{Out} dominant case and P_{M7} dominant case. The advantages are that the LDO has no minimum load current limitation, and the LDO can use a small on-chip load capacitor which is 30 pF in the proposed LDO.

IV. Measurement Results

The proposed LDO was fabricated in a 28nm bulk CMOS technology with 0.0086mm^2 active area. The chip micrograph is shown in Fig. 8. Fig. 9 shows the measured transient response with an on-chip load current changing from 0 µA to 20 mA within 100 ps. The voltage undershoot is 176 mV, which corresponding to a response time of 270 ps, and can be fully recovered within 220 ns. The second voltage droop following the undershoot is because the speed of the auxiliary amplifier is lower than that of the main FVF loop. The auxiliary amplifier needs more time to response. The measured

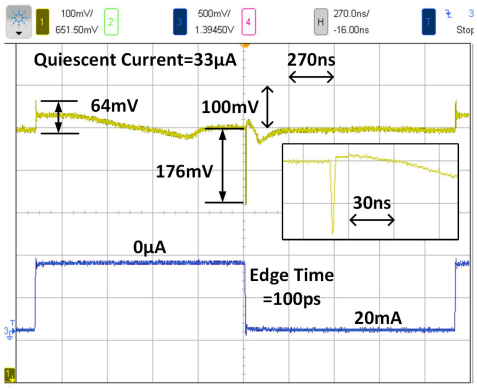

Fig. 9. Measured load-transient responses where $V_{IN} = 0.9$ V and $V_{OUT} = 0.85$ V with a 30 pF on-chip output capacitor.

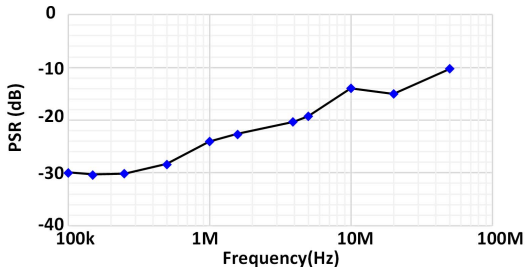

Fig. 10. Measured PSR of the proposed LDO at $I_{LOAD} = 20$ mA.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON FOR THE PROPOSED LDO

	This Work	[1] TCASI'15	[11] TPEL'18	[12] JSSC'12	[13] JSSC'15	[14] JSSC'14
Process	28nm	65nm	130nm	45nm	180nm	65nm
Area [mm^2]	0.0086	0.0234	0.0042	0.075	0.14	0.0133
Type	Analog	Analog	Analog	Hybrid	a	a
V_{DO}[V]	0.05	0.15	0.2	0.085	0.2	0.2
V_{OUT}[V]	0.85	1	0.8	0.9-1.1	1.6	0.55
Power Eff.	94.4%	87.0%	80.0%	91.4%	88.8%	73.3%
PSR[dB]	-24/1MHz	-15.5/1GHz	-57/1MHz	N.A.	-37/10MHz	-8/1MHz
DC Load Reg.	0.26V/A	1.1V /A	0.17V/A	0.23V/A	0.14V/A	0.18V/A
DC Line Reg.	17.5mV/V	27.1mV/V	2.25mV/V	N.A.	16.3mV/V	4mV/V
I_{Q_MIN} [µA]	33	50	112	1.06E+03	55	15.9–487
C_{TOTAL} [pF]	36	140	0-25	1460	128	470–1E4
ΔV_{OUT} [mV]	176	82	284	28	80	113
ΔI_{LOAD} /T_{EDGE}	20mA /100ps	10mA /200ps	25mA /300ps	42mA /N.A.	50mA /100ns	50mA /100ns
FOM1*[ps]	0.52	5.74	1.27	24.57	0.23	0.34
FOM2*[ps·V]	0.03	0.08	0.38	N.A.	8.80	3.59

* $\text{FOM1} = C_{TOTAL} \times \Delta V_{OUT} \times I_Q / \Delta I_{LOAD}^2$ $\text{FOM2} = T_{edge} \times \Delta V_{OUT} \times I_Q / \Delta I_{LOAD}$

quiescent current is 33 µA in this brief. Fig. 10 shows the measured PSR of the proposed LDO at $I_{LOAD} = 20$ mA. The PSR is better than −30 dB at low frequencies, and is −24 dB at 1 MHz.

The performances of the proposed LDO are compared with the state-of-the-art works in Table I. In the comparison table, the proposed LDO has the lowest dropout voltage which makes the proposed LDO have a 94.4% power efficient at full load condition. Also, the proposed LDO achieves competitive figure-of-merits (FoMs) among the listed designs.

V. CONCLUSION

This brief has demonstrated a 50-mV dropout-voltage LDO with a focus on maximizing the power efficiency. When the dropout voltage is reduced, the LDO suffers from the issues of large power transistor size, low loop gain, and poor PSR. Therefore, we employ a coupled transient enhancement unit for dynamic biasing to boost the response speed. And we use an LDO-self-supplied gain boost stage to improve the DC regulation and PSR of the FVF-based LDO. To extend the load current range, we design the LDO's dominant pole changes from P_{Out} to P_{M7} when the load current increases from low to high. That makes the LDO has no limit on the minimum load current while keeps small load capacitance and larger peak load current. Using the proposed techniques, we achieve a small area, fast response, wide load range, and good PSR with a high power efficiency of 94.4%.

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