澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

Major Programme:	Master of Science in Microelectronics & Master of Philosophy in Microelectronics		
Course Type:	☐ CM – Compulsory Major ☑ RE – Required Elective ☐ L&S – Languages and Skills ☐ CPE – Community and Peer Education ☐ * GE – General Education ☐ MI – Minor ☐ FE – Free Elective		
Course Title: (in Chinese and English)	Digital Integrated Circuits 數字集成電路	Suggested Year of Study:	Year 1
Duration:	☑ Semester Course ☐ Yearly Course	Credit Units:	3
Grading System:	☑ Letter Grade ☐ P/NP	Pre-requisite: (if any)	None
Medium of Instruction:	English		
Course Description:	This is an introductory course in digital integrated circuits. It covers topics from MOS inverters and different logic families. The student will learn how to model interconnect wires and design optimization with respect to a number of metrics: cost, reliability, speed and power. This course also covers sequential and dynamic logic circuit design, timing considerations, and clocking approaches, as well as the design of large system blocks, including memories, such as D-flip-flop and SRAM. This customized course from bottom-up based, which starts from the fundamental techniques for the design and analysis of digital circuits. Then, it provides a detailed understanding of basic logic synthesis and analysis algorithms and enables students to apply this knowledge in the design of digital systems and EDA tools. The course aims to give a basic idea of the digital integrated circuit design. The students will have a hands-on experience in combinational circuit optimization (two-level and multi-level synthesis), sequential circuit optimization (state encoding, retiming), timing analysis, testing, and logic verification through the lab work.		
Intended Learning Outcomes (ILO):	This course enables students to have: ・ Apply the essential knowledge in analog circuit design. ・ Apply common digital circuit building blocks, such as logic gates, adder and SRAM, with practical considerations. ・ Design and simulate analog circuits using industrial simulation tools with real-world CMOS processes.		

Major Assessment Methods:	Case Study	Role Playing	Student Presentation	Individual project / paper	Group project / paper	Group discussions	Writing Assignment	Exercises & problems	Service learning	Internship	Field study	Company visits	Reading & Writing Assessments / tests	Listening & Oral Assessments / tests	Others (please specify)
Class Participation / Discussion _____%															
Assignment(s) 70 %				√	√			√							
Test(s) _____%															
Examination _____%															
Others: Project 30 %			√	√											

Course Content: (topic outline)	- Introduction: basic CMOS device physic and technology scaling. - Basic combinational logic overview: CMOS inverters, Nand gate, OR gate, X OR gate, Full and Half Adder design and layout - Modeling of interconnect wires and optimization of design: Elmore delay theory and logical effort. - Other logic families: pass gate logic, dynamic logic and domino logic design consideration and layout. - Memory: D-Flip-Flop and SRAM design and layout - Practical labs: Logic gate layout and synthesis tools