澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

SKL 2010DP
模拟与混合信号
超大规模集成电路
国家重点实验室
（澳门大学）
State Key Laboratory of Analog and Mixed-Signal VLSI
(University of Macau)
中华人民共和国科学技术部

模擬與混合信號超大規模集成電路
國家重點實驗室
State Key Laboratory of Analog and Mixed-Signal VLSI

State Key Lab of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) Newsletter

Motto: "Locally, from (World) Quality towards (National) Quantity"

座右銘:立足本土、人才培養, 以世界級質量創建國家級規模

Year 11
No . 11

March 2022

2021 Milestones

Co-Funded by
Macao Science and Technology Development Fund (FDCT)

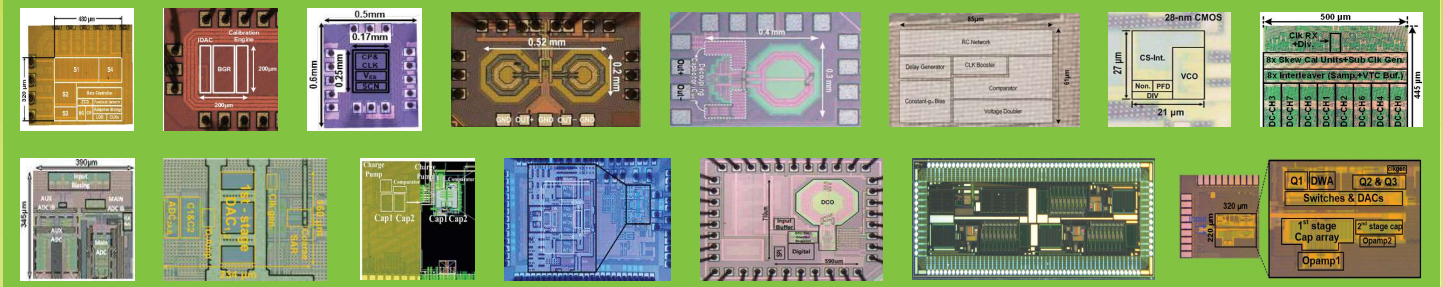
Events

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) participated in the 15th Annual Meeting of the Committee for China and Macao Cooperation in Science and Technology held in Macao, China, June 18, 2021.

Prof. Rui Martins receives the Medal of Merit – Education, in recognition of his outstanding contribution to education from Chief Executive Ho Iat Seng, February 18, 2022.

SKL AMS-VLSI held in November 2021 the 4th meeting of the Academic Committee, which recognised its development direction and provided suggestions for future development.

State-of-the-Art Chips - Designed and Tested in 2021 (16 Chips)



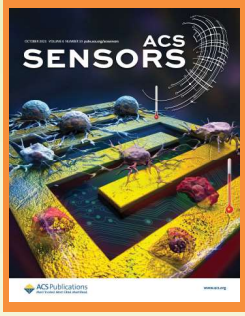
ISSCC 2022

A team of faculty members and students from the SKL AMS-VLSI and ECE/FST, University of Macau (UM) published their results to the 68th IEEE International Solid-State Circuits Conference (ISSCC) in February 2022 virtually (in San Francisco, CA, USA), the most competitive conference in the world in the field of chip design. The SKL AMS-VLSI delegation attended this significant event online. This year, 4 digest papers in the areas of DC-DC Converters, RF and AI were accepted at ISSCC 2022, "A 4A 12-to-1 Flying Capacitor Cross-Connected DC-DC Converter with Inserted D>0.5 Control Achieving >2x Transient Inductor Current Slew Rate and 0.73x Theoretical Minimum Output Undershoot of DSD" provided by T. Hu, M. Huang, Y. Lu, R. P. Martins, "A Battery-Input Sub-1V Output 92.9% Peak Efficiency 0.3A/mm2 Current Density Hybrid SC-Parallel-Inductor Buck Converter with Reduced Inductor Current in 65nm CMOS" provided by G. Cai, Y. Lu, R. Martins, "A 108nW 0.8mm2 Analog Voice Activity Detector (VAD) Featuring a Time-Domain CNN as a Programmable Feature Extractor and a Sparsity-Aware Computational Scheme in 28nm CMOS" provided by F. Chen, K-F. Un, W-H. Yu, P-I. Mak, R. P. Martins, and "A 266μW Bluetooth Low-Energy (BLE) Receiver Featuring an N-Path Passive BalunLNA and a Pipeline Down-Mixing BB-Extraction Scheme Achieving 77dB SFDR and -3dBm OOB-B-1dB" provided by H. Shao, P-I. Mak, G. Qi, R. P. Martins.

New Masters in Microelectronics Opening Ceremony

The Institute of Microelectronics (IME) organized an orientation for the Master of Philosophy and Master of Science in Microelectronics programmes to welcome 35 new postgraduate students on 15 September 2021.

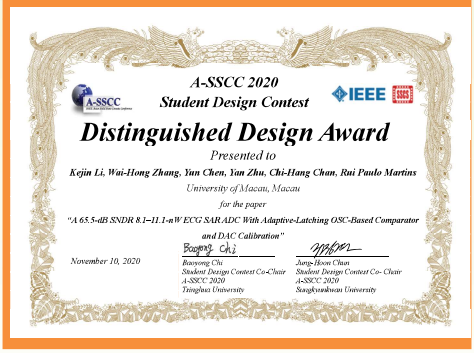
New Breakthrough in Precision Cell Measurement



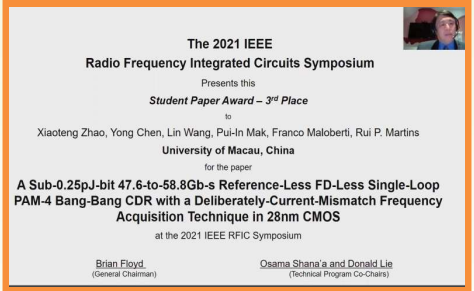
A multidisciplinary research team from the State Key Laboratory of Analog and Mixed-Signal VLSI and the Institute of Microelectronics at the University of Macau has recently proposed a new method for joint assessment of cell health, which can effectively and precisely assess cell health status by constructing a temperature-regulated electrical impedance sensing system to precisely measure cell viability and vitality. The research results were published in ACS Sensors, an international journal of the American Chemical Society in the field of sensors, and selected as the supplemental cover of the journal.

The UM, Tsinghua University, and UESTC held the Third Workshop on IC Advances in China (ICAC 2021)

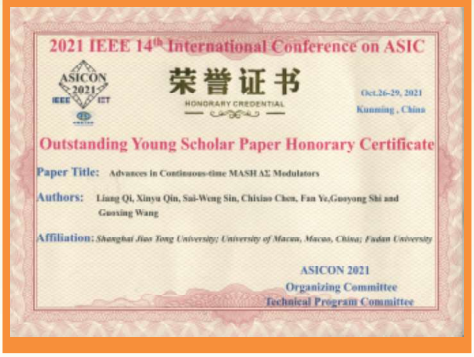
A research team from IME received the Student Design Contest Distinguished Design Award in the IEEE Asian Solid-State Circuit Conference (A-SSCC)


A-SSCC 2020
Student Design Contest
IEEE
Distinguished Design Award
Presented to
Kejin Li, Wai-Hong Zhang, Yan Chen, Yan Zhu, Chi-Hang Chan, Rui Paulo Martins
University of Macau, Macau
for the paper
"A 65.5-dB SNDR 8.1–11.1-nW ECG SAR ADC With Adaptive-Latching OSC-Based Comparator and DAC Calibration"
November 10, 2020
Baoyong Chi
Baoyong Chi
Student Design Contest Co-Chair
A-SSCC 2020
Tsinghua University
Jun-Eon Chun
Student Design Contest Co- Chair
A-SSCC 2020
Sungkyunkwan University

A research team from IME received the Best Student Paper Award (Third Place) in IEEE Radio Frequency Integrated Circuits (RFIC)


The 2021 IEEE
Radio Frequency Integrated Circuits Symposium
Presents this
Student Paper Award – 3rd Place
to
Xiaoteng Zhao, Yong Chen, Lin Wang, Pui-In Mak, Franco Maloberti, Rui P. Martins
University of Macau, China
for the paper
A Sub-0.25pJ-bit 47.6-to-58.8Gb-s Reference-Less FD-Less Single-Loop PAM-4 Bang-Bang CDR with a Deliberately-Current-Mismatch Frequency Acquisition Technique in 28nm CMOS
at the 2021 IEEE RFIC Symposium
Brian Floyd
(General Chairman)
Osama Shana'a and Donald Lie
(Technical Program Co-Chairs)

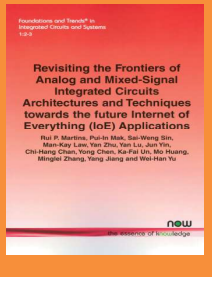
A research team from Institute of Microelectronics (IME) received the Outstanding Young Scholar Paper Award in IEEE International Conference on ASIC (ASICON)


2021 IEEE 14th International Conference on ASIC
ASICON 2021
荣誉证书
HONORARY CREDENTIAL
Oct.26-29, 2021
Kunming, China
Outstanding Young Scholar Paper Honorary Certificate
Paper Title: Advances in Continuous-time MASH ΔΣ Modulators
Authors: Liang Qi, Xinyu Qin, Sai-Weng Sin, Chixiao Chen, Fan Ye, Guoyong Shi and Guoxing Wang
Affiliation: Shanghai Jiao Tong University; University of Macau, Macao, China; Fudan University
ASICON 2021
Organizing Committee
Technical Program Committee

6 New PhD Graduates in 2021

6. **Cheng Gong**, *Advanced Control and Coordination of Hybrid Active Power Filters for Power Quality Compensation in Smart Distribution Networks*
5. **Haoran Li,** *A new method of flexible sample delivery on digital microfluidics*
4. **Ren Shen,** *Novel materials and methods for PCR enhancement on digital microfluidics*
3. **Dongyang Jiang,** *Advanced Architecture Alternatives for Time-Interleaved Delta-Sigma Modulators*
2. **Panke Wang,** *A Real-time Neural Spike Sorting System and Its Application on Neural Decoding*
1. **Jiawen Li,** *Brain Rhythm Sequencing Technique Using Electroencephalography Signal and Its Application in Health Care*

A new extensive review paper on IoE


Revisiting the Frontiers of Analog and Mixed-Signal Integrated Circuits Architectures and Techniques towards the future Internet of Everything (IoE) Applications

Selected works from research lines

In IEEE Journal of Solid-State Circuits - JSSC 2021

A 0.35-V 5,200-μm² 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator

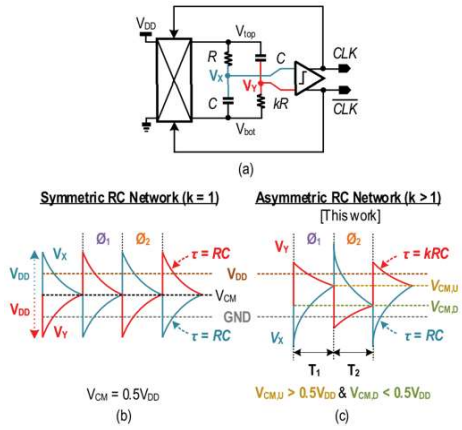
Ka-Meng Lei, Pui-In Mak, and Rui P. Martins

From Wireless and Multidisciplinary research line

Motivation

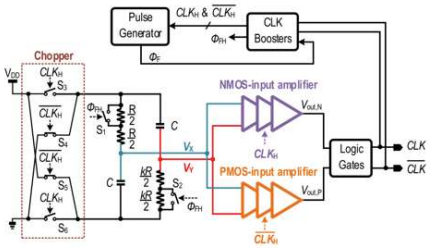
This article proposes a relaxation oscillator (RxO) that surmounts the challenges of sub-0.5-V operation and achieves high area and energy efficiencies. The key techniques are: 1) an asymmetric RC network to free the VCM restriction while preserving a swing boosted output and 2) a dual-path comparator with delay compensation to allow temperature resilience. Prototyped in 28-nm CMOS, the RxO occupies a tiny area (5,200 μm2) and achieves superior energy efficiency (667 fJ/cycle) and figure-of-merit (FoM1 = 181 dB), with respect to prior art.

Architecture

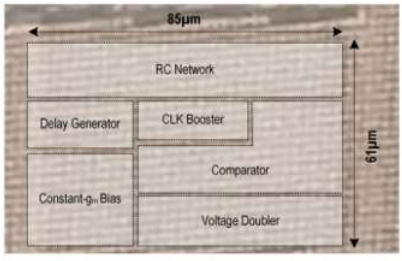


(a) Simplified schematic of the swing-boosted differential RxO. (b) Timing diagram of the output of the RC network with k = 1, where VCM is fixed at 0.5 V. (c) Timing diagram of the output of the RC network with k > 1, such that VCM,U and VCM,D suit the design of the subsequent ULV comparator (this work).

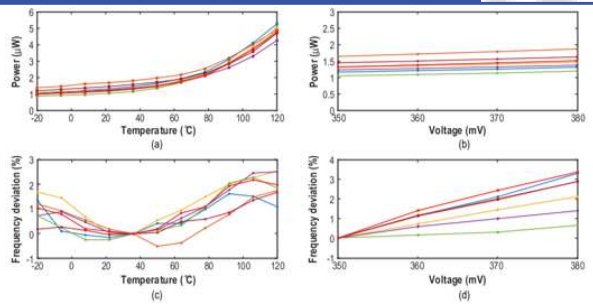
Implementation



Proposed ULV swing-boosted RxO featuring an asymmetric RC network and a dual-path comparator. The delays of the amplifiers are tracked to tackle the frequency fluctuation against temperature and voltage variations



Verification



Measured performance of the RxO from 7 chip samples. (a) P vs. T. (b) P vs. VDD. (c) Δf vs. T. (d) Δf vs. VDD.

	Koo, ISSCC'17 [11]	Mikulić, ESSCIRC'17 [8]	Liu, JSSC'19 [12]	Savanth, JSSC'19 [9]	Lee, JSSC'20 [13]	This work
Process (nm)	180	350	65	65	180	28
Frequency (MHz)	0.44	1	1.05	1.2	10.5	2.1
V_{DD} (V)	1.4 ~ 3.3	3 ~ 4.5	0.98 ~ 1.02	0.9 ~ 1.8	1.4 ~ 2.0	**0.35 ~ 0.38**
Power (μW)	21.3	210	69	0.82	219.8	1.4
Energy efficiency (pJ/cycle)	48.4	210	65.7	0.68	20.9	**0.67**
T_{range} (°C)	−20 to 100	−40 to 125	−15 to 55	−20 to 125	−40 to 125	−20 to 120
TC (ppm/°C)	169	24.3	4.3	100	137	158
Variation across V_{DD}	0.04%	0.42%	0.17%	±0.54%	2.64%	2.3%
Line sensitivity ($\frac{\Delta f}{f}\frac{\Delta V}{V}$)	0.03%	0.84%	4.25%	±0.54%	6.16%	26.8%
Area (μm²)	58,000	40,000	51,000	5,000	15,000	**5,200**
Period jitter (ps_{rms})	1,060	-	160	-	9.86	800
Startup time (μs)	-	11	8	10	-	**3.6**
No. of samples	100	5	-	7*	15	7
FoM_1 (dB)	162	165	174	183	168	**181**
FoM_2 (dBc/Hz)	−152.7 (@10 kHz)	-	-	-	−157.7 (@1 kHz)	−143.4 (@ 10 kHz)

*For temperature stability measurement.
†Deduced from the numbers of cycles to start, which may underestimate the true startup time.

This work was supported in part by the Science and Technology Development Fund, Macau SAR under Grant 0043/2020/A1 and Grant SKLAMSV(UM)-2020–2022.

In IEEE International Solid-State Circuits Conference - ISSCC 2021

A 25MHz-BW 75dB-SNDR Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC with Background Offset Calibration

Hongshuai Zhang, Yan Zhu, Chi-Hang Chan, Rui Paulo Martins

From Data Conversion and Signal Processing research line

Motivation

By breaking the conversion in two-step with a pipeline scheme, it can enhance the speed and relax the comparator noise either through the inter-stage redundancy or gain. While further adopting the noise shaping technique, the critical comparator noise can be further suppressed. Although the residue amplifier (RA) in these architectures enable pipeline and/or noise shaping, its gain accuracy and linearity are crucial and often need conscious design.

In this work, a MASH N-0 structure realized by a noise-shaping SAR-assisted pipeline architecture is introduced, which has an inherent gain error tolerance ability. An Nth order noise shaping SAR ADC in the first stage shapes the quantization error and comparator noise in all stages, together with the in-ter-stage gain error, gain nonlinearity and partial noise from the RA, thus relaxing the comparator and RA design.

Architecture

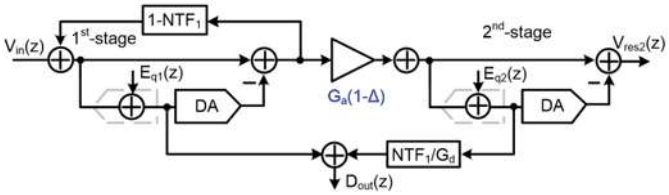


Fig. 1. the MASH N-0 SAR assisted pipelined ADC.

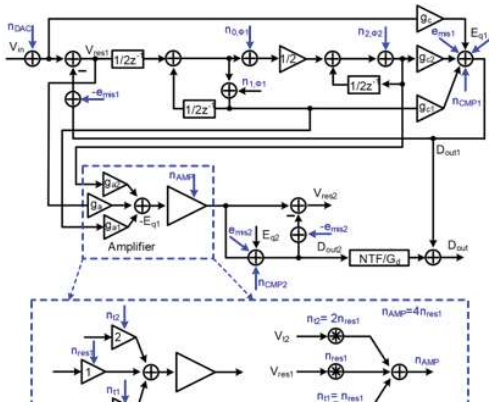


Fig. 2. Noise and mismatch analysis of the MASH 2-0 structure.

Implementation

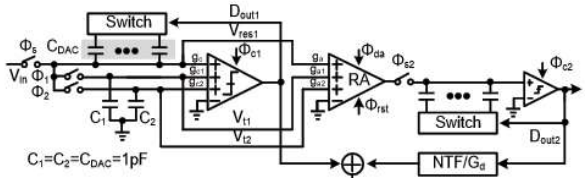


Fig. 3. The proposed CIFF MASH 2-0 SAR-assisted pipeline.

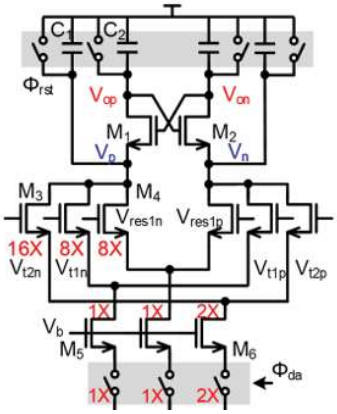
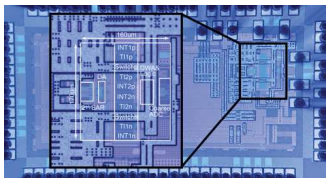
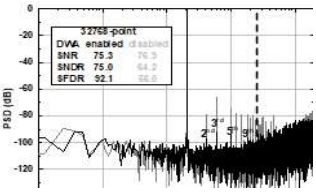


Fig. 4. The proposed amplifier schematic.

Verification





(a) (b)

(a) Die photo. (b) Output Spectrum of the ADC.

TABLE OF COMPARISON

	Gregoire ISSCC 08	Yoshioka ISSCC 17	Song VLSI 18	Hsu CICC 20	This work
Process[nm]	180	28	65	40	28
Architecture	Pipeline ADC	Pipeline SAR	0-1 MASH	Pipeline SAR	2-0 MASH
Gain Error Suppression	**CLS**	**Digital Amplifier**	**Close-loop Opamp**	**2nd-order GES**	**Inherent Architecture**
DAC Mismatch Solution	**N/A**	**N/A**	**Foreground Off-chip Calibration**	**Foreground Off-chip Calibration**	**4b DWA**
Supply [V]	1.2	0.7	1.0	1.0	1.0
Fs [MS/s]	**20.2**	**160**	**200**	**100**	**400**
Power [mW]	7.5	1.9	4.5	1.38	1.26
Area [mm²]	2.3	0.097	0.014	0.054	0.027

This work was Funded by The Science and Technology Development Fund, Macau SAR (File no. 0004/2020/AKP and SKL-AMSV (UM)-2020-2022) and Research Grants of University of Macau (MYRG2019-00021-AMSV).

In IEEE Transactions on Power Electronics - TPEL 2021

A 2.4-GHz CMOS Differential Class-DE Rectifier With Coupled Inductors

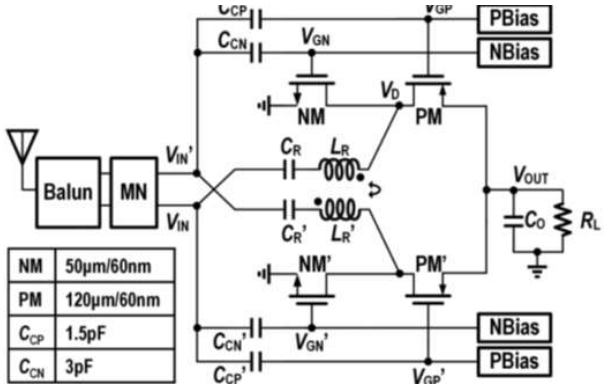
Tingxu Hu, Mo Huang, Yan Lu, Xiuyin Zhang, Franco Maloberti, Rui. Martins

From Integrated Power research line

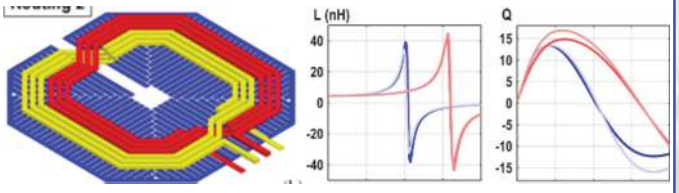
Motivation

Class-DE radio frequency (RF) rectifiers improves the power conversion ratio (PCE) by zero-voltage switching (ZVS) and zero-current switching (ZCS). The conventional class-DE rectifier has a limited loading range if meeting ZVS/ZCS and input impedance matching simultaneously. Adding another LC network is a solution to extend the loading range. This article presents a 2.4GHz differential class-DE rectifier with coupled inductors. This reduce the extra LC network from the conventional design, while maintaining a wide loading range, ZVS/ZCS and input impedance matching. The coupled inductors save significant silicon area of a differential design. Meanwhile, the rectifier uses adaptive bias to extend the input power range. It achieves a peak 68.5% PCE at 9-dBm input power, while maintains >40% PCE within a wide 16-dB input power range. It is suitable for energy-harvesting applications.

Architecture

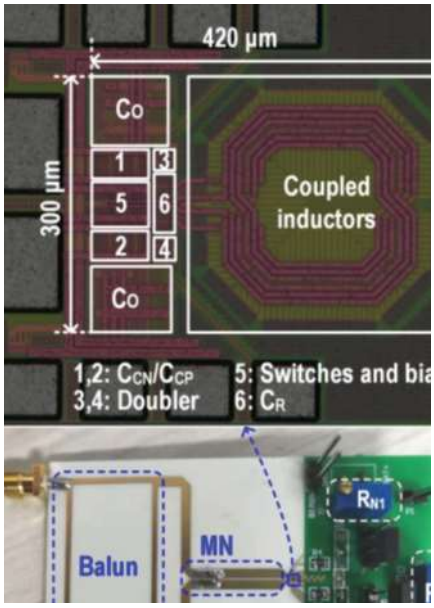


Schematic of the proposed rectifier



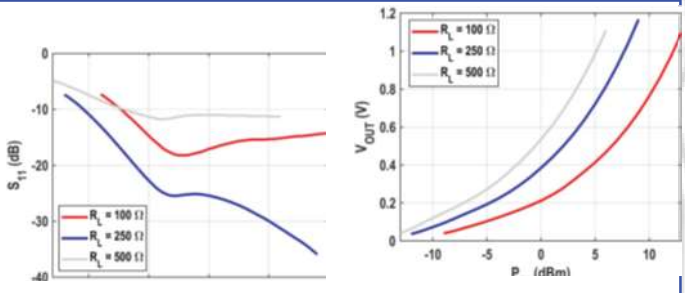
Coupled inductors layout, and the SRF and Q's improvement from the conventional routing.

Implementation

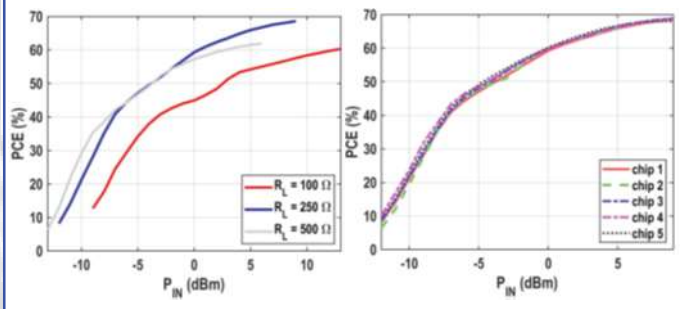


Chip and PCB photographs

Verification



Measured S11 and output voltage



Measured efficiencies

This work was supported in part by the Key-Area Research and Development Program of Guangdong Province under Grant 2019B010140002; in part by the Natural Science Foundation of China under Grant 61974046; in part by the Science and Technology Development Fund, Macau, SAR, under Grant 45/2019/A3 and Grant SKL-AMSV(UM)-2020-2022; and in part by the Research Committee of the University of Macau under Grant MYRG2020-00117-IME.

In IEEE Journal of Solid-State Circuits - JSSC 2022

Design of Reference-Less Single-Loop PAM-4 CDR Using Deliberate Strobe Points on Clock for Frequency Acquisition

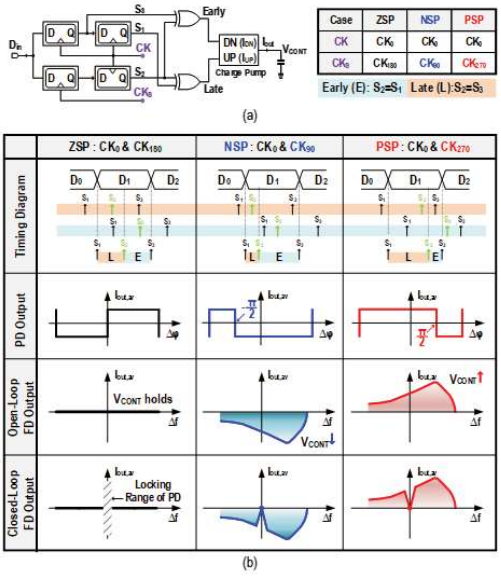
Xiaoteng Zhao, Yong Chen, Pui-In Mak, and Rui P. Martins

From Wireless and Multidisciplinary research line

Motivation

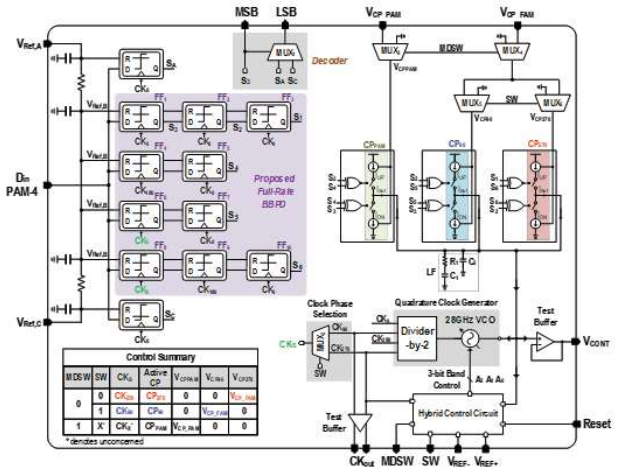
In the design of reference-less clock and data recovery circuits, the key challenge is to achieve fast, robust, and wide frequency acquisition. Prior work adopted a deliberate delay cell in the data path for single-sided frequency capture ability. However, the delay is sensitive to the process, voltage, and temperature (PVT) variations. Furthermore, it requires off-chip capacitors to complete the control logic with relative long acquisition time. This work reported a reference-less FD-less single-loop full-rate BBCDR. It features fast and robust frequency acquisition ability for PAM-4 signal. The key idea is the deliberate strobe points for the clock and corresponding hybrid control circuits. With the help of them, the proposed CDR enhances the single-sided frequency capture and speeds up frequency acquisition with state-of-the-art energy efficiency.

Architecture

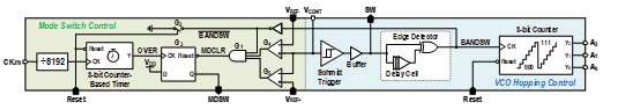


(a) Block diagram of the proposed BBPD and (b) its operation principle that uses clock-phase selection to realize ZSP/NSP/PSP.

Implementation

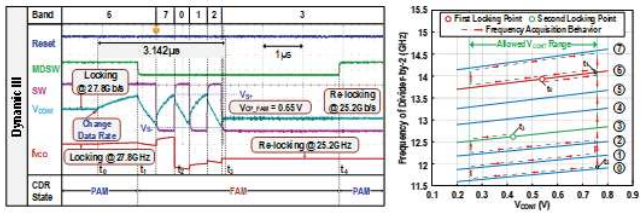


Complete diagram of the proposed BBCDR with its control summary

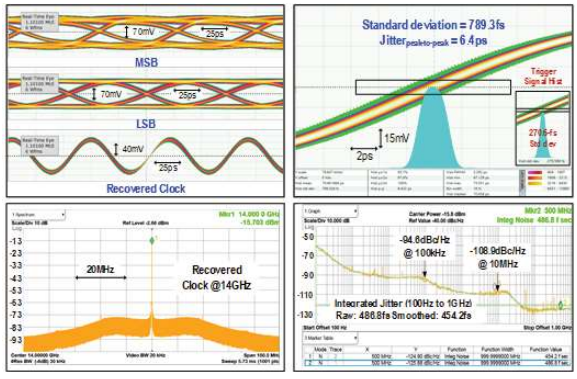


Block diagram of the proposed hybrid control circuits

Verification



Measured dynamic process and frequency traveling route



Eye diagram, jitter histogram, recovered clock spectrum, and phase noise under 28-Gb/s PAM-4 input.

This work was supported in part by Guangzhou Science and Technology Innovation and Development of Special Funds (GSTIC) [EF002/IME-CY/2019/GSTIC] and in part by Macau Science and Technology Development Fund (FDCT), Macau SAR [SKL-AMSV(UM)-2020-2022].

In IEEE Transactions on Power Electronics - TPEL 2021

Design and Analysis of Vector Proportional-Integral Current Controller for LC-Coupling Hybrid Active Power Filter with Minimum DC-Link Voltage

Cheng Gong, Wai-Kit Sou, and Chi-Seng Lam

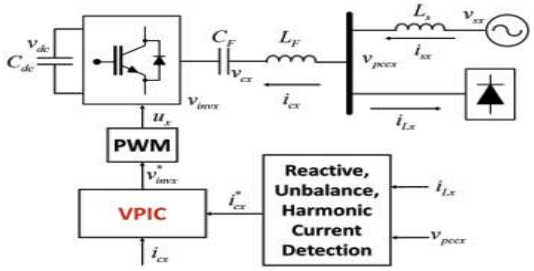
From Integrated Power research line

Motivation

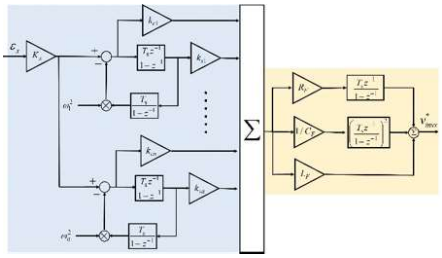
LC coupling hybrid active power filter (LC-HAPF) is a cost-effective solution for power quality issues, which operates under low DC-link voltage. The low DC-link operating voltage benefits of low switching loss and low current ripple. However, the controller design under low DC-link voltage condition is still lack of study.

In this paper, a vector proportional-integral controller (VPIC) is proposed for the LC-HAPF. The VPIC provides ideally zero steady-state error at selected harmonic frequencies and optimizes transient response. Moreover, the VPIC ensures the LC-HAPF performance even under its minimum DC-link voltage condition. The advantages of the proposed VPIC are verified by simulation and experimental results in comparison with the quasi-proportional-resonant controller (QPRC), proportional multi-resonant controller (PMRC), and second-order sliding mode controller (SOSMC).

Architecture

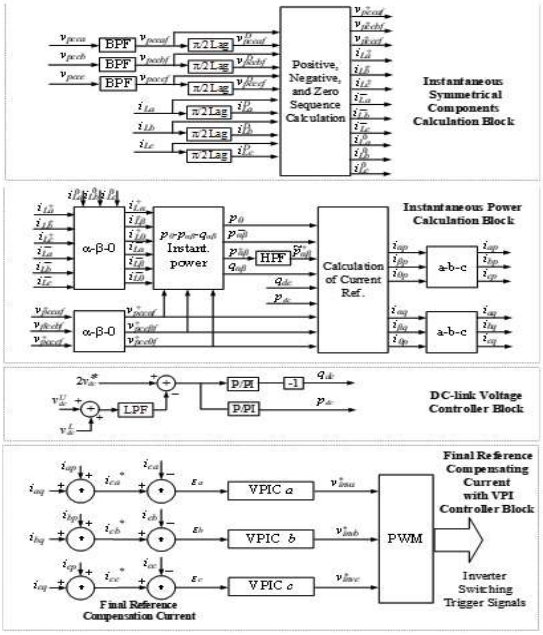


Single-phase equivalent diagram of the LC-HAPF with the proposed VPIC.



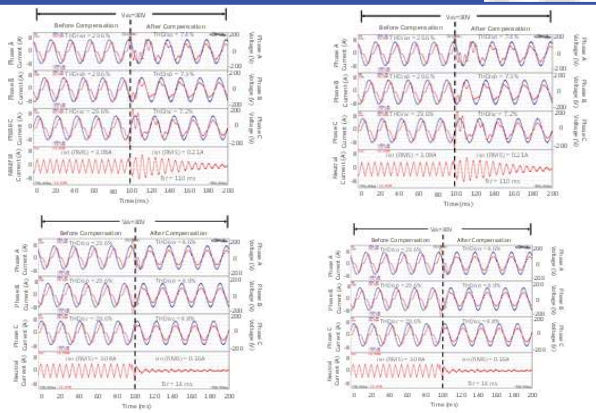
z-domain block diagram of the proposed VPIC.

Implementation



Overall control diagram of LC-HAPF with the proposed VPIC

Verification



Experimental results of LC-HAPF under minimum DC-link voltage with different current controllers: (a) QPRC; (b) PMRC; (c) SOSMC; (d) proposed VPIC.

Index (phase *a*)	Before Compensation	After Compensation			
		QPRC	PMRC	SOSMC	VPIC
T_{st} (ms)	-	30	110	60	14
PF	0.75	0.99	0.99	0.99	0.99
THD_{ica} (%)	29.6	12.1	7.4	7.9	4.6
I_{ca} (Arms)	2.74	1.26	0.21	0.18	0.16

This work was supported in part by The Science and Technology Development Fund, Macau SAR (FDCT) (File no. 025/2017/A1, 0028/2020/A1 and SKL-AMSV(UM)-2020-2022) and in part by the University of Macau (File no. MYRG2017-00090-AMSV, File no. MYRG2017-00090-AMSV).

In IEEE Journal of Solid-State Circuits - JSSC 2021

A Time-Interleaved 2nd-order ΔΣ Modulator Achieving 5 MHz Bandwidth and 86.1dB SNDR Using Digital Feedforward Extrapolation

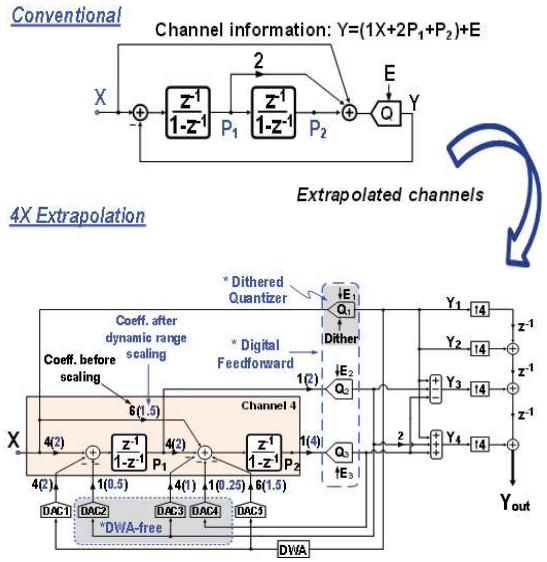
Dongyang Jiang, Liang Qi, Sai-Weng Sin, Franco Maloberti, and Rui P. Martins

From Data Conversion and Signal Processing research line

Motivation

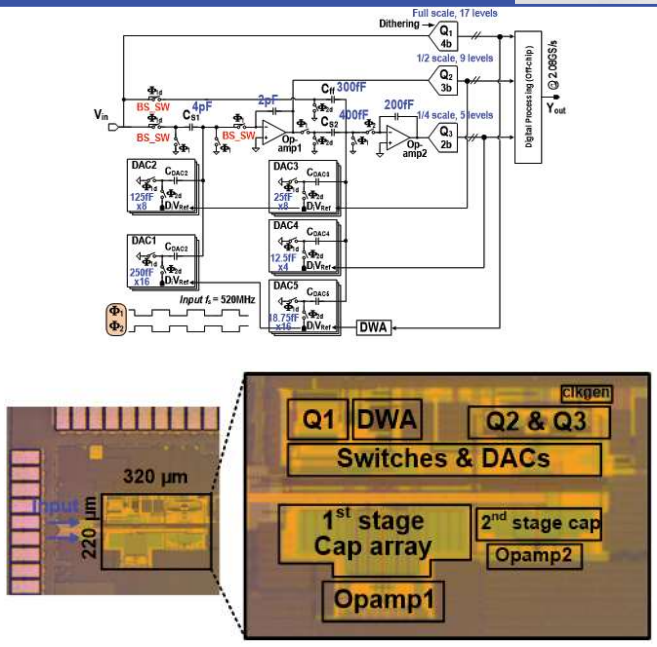
This work presents a 4X Time-Interleaved (TI) 2nd-order discrete-time (DT) Delta-sigma Modulator (DSM). We propose a digital feedforward extrapolation by firstly digitizing the internal analog nodes' information from one channel, and then extrapolating the other channels in the digital domain. As a result, this DSM only needs two operational amplifiers (opamps) to realize four interleaving paths, thus reducing analog hardware overheads. Meanwhile, we linearize the digital feedforward paths through injected dithering. We present the derivation of extrapolating TI DSM starting from a single channel DSM, while several conventional TI approaches are also listed and compared. Implemented in 28nm CMOS, this modulator achieves an equivalent output-sampling rate of 2.08GS/s, 208x OSR, and an SNDR/SFDR of 86.1dB/98dB with 5MHz bandwidth (BW). The power consumption is 23.1mW, which results in a Schreier Figure of Merit (SNDR) of 169.5dB.

Architecture



Block diagram of the proposed extrapolating 4X TI DSM with digital feedforward quantizers.

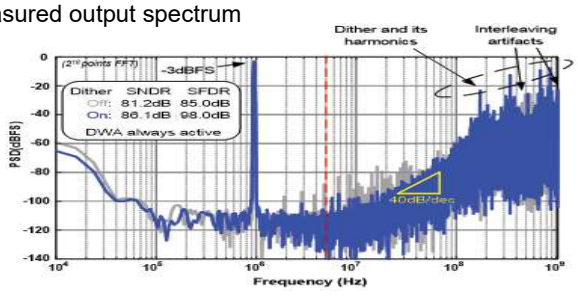
Implementation



Complete Circuit, and Chip Photograph

Verification

Measured output spectrum



Reference	This Work	JSSC 19 Jie [26]	JSSC' 20 Song [27]	JSSC'20 Qi [2]	JSSC'20 Baluni [28]	JSSC'20 Liu [30]
Architecture	TI-DT	TI-DT	DT	CT	CT	CT
Tech. (nm)	28	40	65	28	65	28
Fs (MHz)	520	400	200	1200	2560	1700
Supply (V)	1/1.15/ 1.5	1	1.2	1.2/1.5	1.1	1/1.1/ 1.5
BW (MHz)	5	50	12.5	50	20	85
SNDR (dB)	86.1	70.4	77.1	76.6	82.1	74.4
SFDR (dB)	98	88.0	90.7	87.9	97.7	87.5
DR (dB)	90	71.7	78.5	80	85	79.3
Power(mW)	23.1	13	4.5	29.2	11.3	61.8
Area (mm2)	0.07	0.061	0.014	0.085	0.37	0.51
NDSD (dBFS/Hz)	-153.0	-147.4	-148.1	-153.6	-155.1	-153.7
FOMs(dB)	169.5	166.3	171.5	168.9	174.1	165.8

$FOM_S = \mathrm{SNDR} + 10 \times \log10\left(\frac{BW}{Power}\right)$; $\mathrm{NDSD(dBFS/Hz)} = -(\mathrm{SNDR(dB)} + 10\log(\mathrm{BW}))$;

This work was funded The Science and Technology Development Fund, Macao SAR [File no. 076/2017/A2], and the Ministry of Science and Technology, China. [File no. EF001/AMSV/2018/MOST].

In IEEE Custom Integrated Circuits Conference - CICC 2021
IEEE Journal of Solid-State Circuits - JSSC 2022

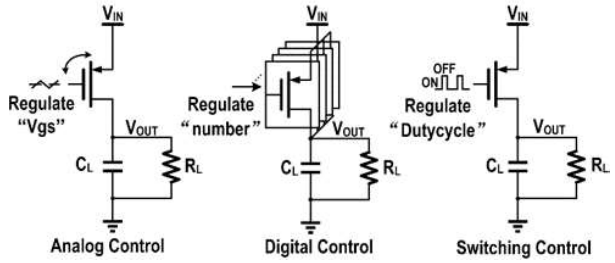
A Scalable High-Current High-Accuracy Dual-Loop Four-Phase Switching LDO for Microprocessors

Xiangyu Mao, Yan Lu, Rui Martins

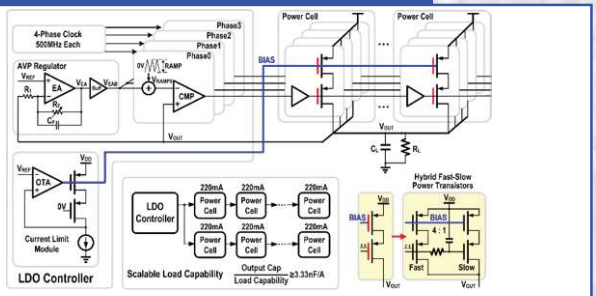
From Integrated Power Research Line

Motivation

High-performance microprocessors need high current (ampere-level), high accuracy, and fast-response power supplies for an energy-efficiency operation. Comparing to analog and digital low-dropout (LDO) regulators, the switching LDO can be a better candidate for such requirements, as it can drive large power transistor(s) fast and accurately. However, conventional switching LDOs need large load capacitance to reduce the output ripple, which restricts their applications. This work presents a 1.5-A fully-integrated switching LDO for microprocessors, with an easily scalable load capability.



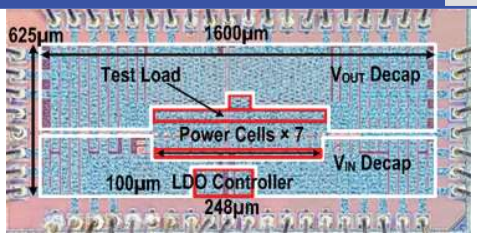
Architecture



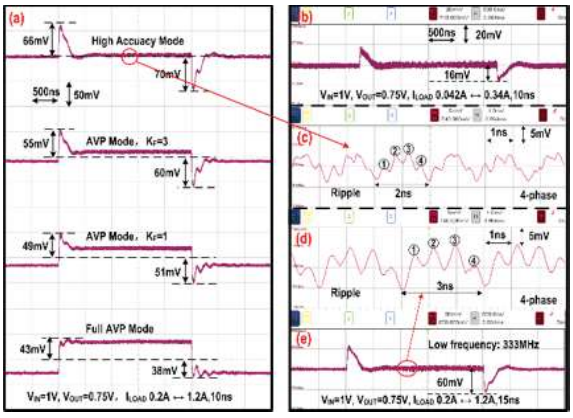
Here, we introduce three techniques together to relief the output capacitance requirement: 1) 4-phase 500-MHz pulse-width modulation (PWM) with inherent current balancing; 2) current-limited power cells resisting PVT variations; and 3) hybrid fast-slow power transistors. Therefore, we reduce significantly the load capacitance to maximum load current ratio CL/IMAX when compared with the prior switching LDOs.

Also, the proposed dual-loop architecture not only achieves a fast transient response, but also provides high-accuracy regulation. In addition, we design the tunable active voltage positioning (AVP).

Implementation

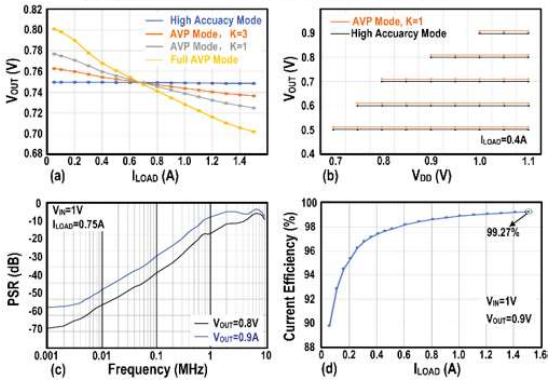


The proposed switching LDO is fabricated in 28-nm CMOS.



Verification

	[18] ISSCC	[19] JSSC	[20] CICC	This Paper
Output Cap C_L (nF)	750	481	2.7	5
Load capability I_L (A)	11.9	12	0.17	1.5
K=C_L/I_{MAX} (nF/A)	63.02	40.08	15.88	3.33



The measured load regulation is 1 mV/A and the line regulation is 1.5 mV/V. Also, we obtain a good power supply rejection (PSR) of −63 dB at 10 kHz and −20 dB at 1 MHz. The PWM automatically moves to a pulse-skipping mode at light load, reducing the quiescent current to 1.8 mA, while the peak current efficiency is 99.27%.

This work was supported in part by the Research Committee of University of Macau under grant MYRG2020-00126-IME, and Macao Science and Technology Development Fund (FDCT) under Grant SKL-AMSV(UM)-2020-2022.

In Royal Society of Chemistry Lab on a Chip - 2021

Cancer Drug Screening with an on-chip Multi-drug dispenser in Digital Microfluidics

Jiao Zhai, Caiwei Li, Haoran Li, Shuhong Yi, Ning Yang, Kai Miao, Chuxia Deng, Yanwei Jia*,

Pui-In Mak, Rui P. Martins

From Wireless and Multidisciplinary research line

Motivation

Microfluidics has been the most promising platform for drug screening with a limited number of cells. However, convenient on-chip preparation of a wide range of drug concentrations remains a large challenge and has restricted wide acceptance of microfluidics in precision medicine. In this paper, we report a digital microfluidic system with an innovative control structure and chip design for on-chip drug dispensing to generate concentrations that span three to four orders of magnitude, enabling single drug or combinatorial multi-drug screening with simple electronic control. Specifically, we utilize droplet ejection from a drug drop sitting on a special electrode, named a drug dispenser, under high-voltage pulse actuation to deliver the desired amount of drugs to be picked up by a cell suspension drop driven by low voltage sine wave actuation. This system with fewer cancercells, less drug consumption, a small footprint, and high scalability with regard to concentration could pave the way for precision medicine.

Architecture

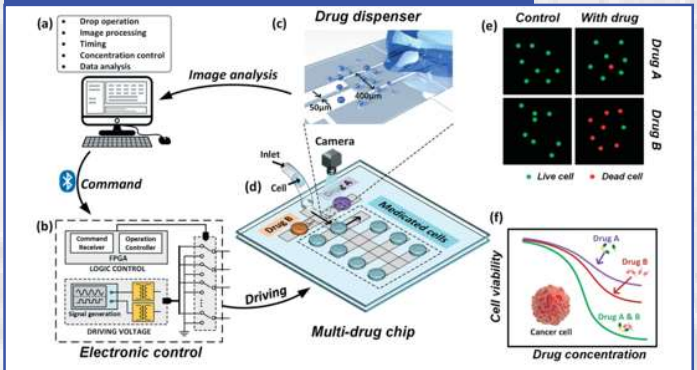


Fig. 1 A digital microfluidic (DMF) system for flexible on-chip drug dispensing for multi-drug screening: (a) the software control; (b) electronic hardware control; (c) a schematic of on-chip drug dispensing; (d) an illustration of a DMF chip with preloaded drugs and input of cell suspension; (e) cell viability identification; and (f) drug efficacy at various concentrations.

Implementation

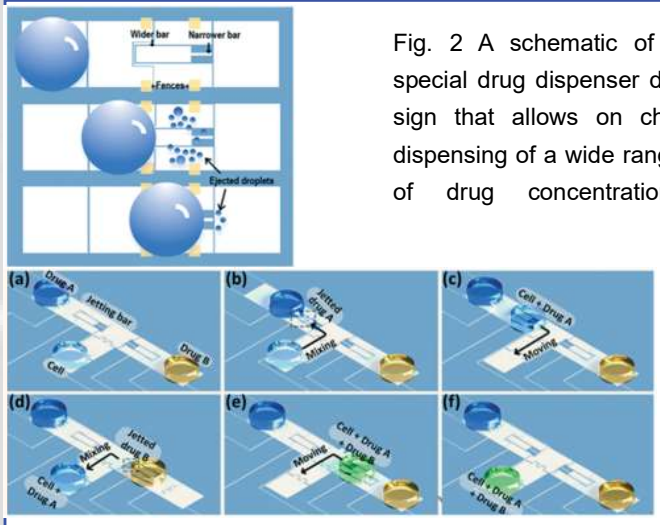


Fig. 2 A schematic of a special drug dispenser design that allows on chip dispensing of a wide range of drug concentrations

Fig. 3 Schematics of combinatorial drug screening on a digital microfluidic (DMF) chip. (a–c) The dynamic schematics of cell droplet moving and mixing with jetted drug A; (d–f) the dynamic schematics of cell-drug A mixed droplet moving and mixing with jetted drug B.

Verification

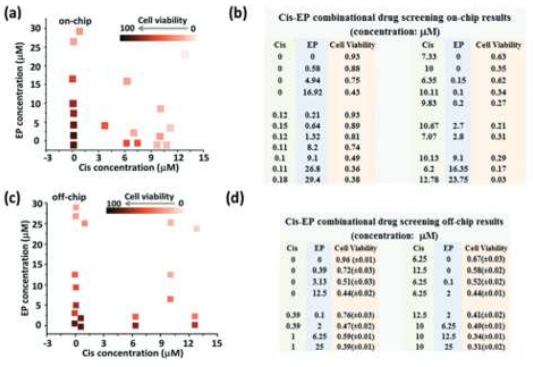


Fig. 4 Combinatorial drug screening for breast cancer cells MDA-MB-231 with on-chip drug dispensing and off-chip manual dispensing. (a and c) The combinatorial drug (cisplatin [Cis] and epirubicin [EP]) toxicity test: (a) on-chip and (c) off-chip. 16–21 drug concentration combination values were generated for the on-chip/off-chip test. (b and d) The data for different drug concentration combinations and the corresponding cell toxicitytest results: (b) on-chip and (d) off-chip.

This work was supported by the Macau Science and Technology Development Fund (FDCT) [FDCT 0053/2019/A1, FDCT0072/2020/AGJ, SKL-AMSVIJUM)/2020-2022], the University of Macau [MYRG2018-00114-AMSV], the Zhuhai Science & Technology Innovation Bureau [ZH22036302200052PWC; ZH22017002200012PWC], DAAN Gene Co., Ltd. [EF009/AMSVJYW/2018/GSTIC], and the Guangdong Department of Science and Technology [2021A0505080002].

In Royal Society of Chemistry Lab on a Chip - 2022

One-shot high-resolution melting curve analysis for KRAS point-mutation discrimination on a digital microfluidics platform

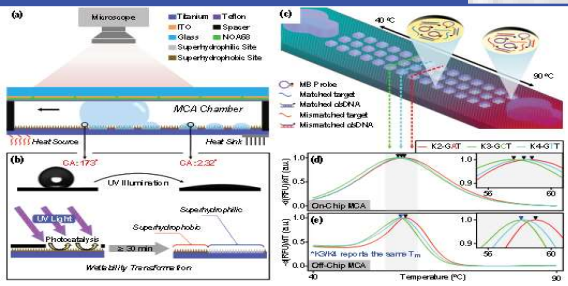
Mingzhong Li, Liang Wan, Man-Kay Law, Li Meng, Yanwei Jia, Pui-In Mak, and Rui P. Martins

From Wireless and Multidisciplinary research line

Motivation

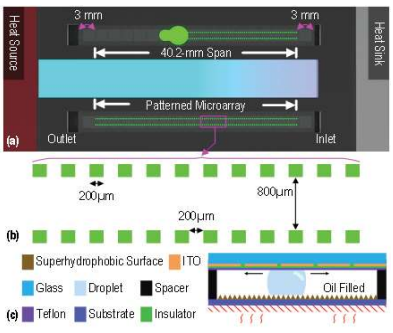
Among different existing single-nucleotide polymorphism genotyping techniques, melting curve analysis (MCA) becomes increasingly popular due to its high accuracy and straightforward procedures in extracting the melting temperature (Tm). Yet, its study on existing digital microfluidic (DMF) platforms has intrinsic limitations due to the temperature inhomogeneity within a thickened droplet during the on-chip rapid heating process. This work proposes a one-shot MCA on DMF platform through high-resolution patterning of pL-scale droplets through a functional substrate, exhibiting a superwettability contrast of >170° for passive pL-scale DNA sample isolation. This high-resolution MCA technique can successfully discriminate KRAS gene targets with single-nucleotide mutations in 3 seconds as well as a high Tm accuracy and consistency when compared with off-chip results.

Architecture



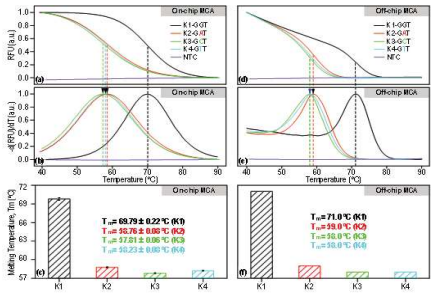
(a) Schematic of the fabricated DMF device (side view) monitored by a fluorescence microscope for MCA. (b) shows the surface wettability transformation by UV illumination. (c) Illustrative SE isometric view of the DMF device for high-resolution MCA. The DNA mix solution is transported across the super-hydrophilic patterns for passive isolation of pL-scale samples. (d) shows the successful on-chip discrimination of mutant-type (K2–K4) KRAS target-probe hybrids with point mutations based on the proposed functional substrate. In contrast, (e) shows its negative discrimination results between K3 and K4 from the off-chip tests using a commercial qPCR machine.

Implementation



(a) Schematic of the DMF device with patterned microarray for melting curve analysis. The Peltier underneath the substrate is employed for the establishment of the thermal gradient. (b) shows the detailed dimensions of the super-hydrophilic regions. (c) shows the illustrative setup for the investigation of breakdown voltage of the device. ITO electrodes are placed on the top plate. A Peltier heat source is positioned directly on the bottom surface of the DMF device for the regulation of substrate temperatures from 40 °C to 90 °C for both temperature calibration and breakdown voltage investigation.

Verification



Experimental results illustrate the (a) on-chip representative melting curves and (b) the melting peaks of the wild-type (K1) and the mutant-type (K2–K4) KRAS target-probe hybrids in codon 12 with a mutation of G→C, G→A or G→T. (c) illustrates the melting temperatures (T_m) of the on-chip MCA for all the KRAS target-probe hybrids, with values of 69.79 ± 0.22 °C (K1), 58.76 ± 0.08 °C (K2), 57.81 ± 0.06 °C (K3), and 58.23 ± 0.08 °C (K4). (d) shows the representative off-chip melting curves and (e) melting peaks of K1–K4, indicating that the (f) T_M values are 71.0 °C (K1), 59.0 °C (K2), 58.0 °C (K3), and 58.0 °C (K4). NTC (no template control) is applied.

This work was supported in part by the Macao FDCT fund under Grant 011/2019/APJ and SKL-AMSV-2020-2022, and in part the research committee of the University of Macau under Grant MYRG2017-AMSV-00221

In IEEE International Solid-State Circuits Conference - ISSCC 2021

Wideband-Harmonic-Shaping VCO Achieving High FoM and 1/f3 PN-Corner Reduction Without Manual Harmonic Tuning

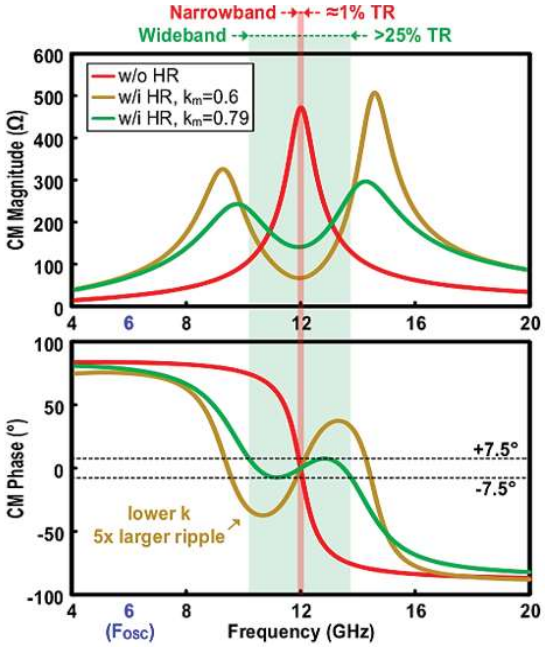
Hao Guo, Yong Chen, Pui-In Mak, and Rui P. Martins

From Wireless and Multidisciplinary reasearch line

Motivation

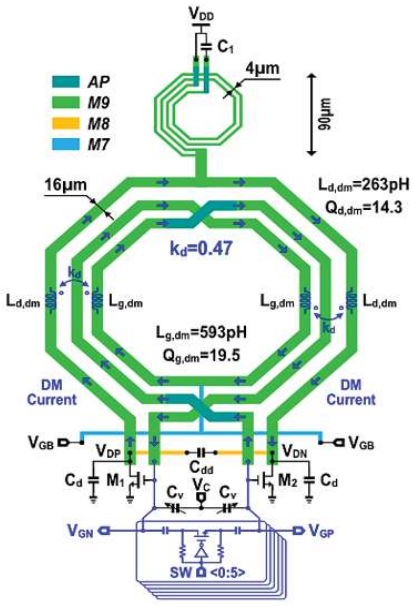
In the design of voltage-controlled oscillator circuits (VCO), the key challenge is to achieve lower PN, 1/f3 Corner, and wide tuning range (TR), Prior work requires manual harmonic tuning for aligning the 1st-to-2nd and 1st-to-3rd harmonic resonances. However, the VCO needs a multi-switched capacitor array (SCA) for multi-dimensional frequency tuning. Furthermore, Multi-switched capacitor arrays increase circuit complexity and reduce inductor Q value. This work reported VCO without manual harmonic tuning. It features no harmonic tuning also achieves high performance. The key idea is to put the head resonator (HR) on top of the 1:2-turn transformer to obtain a pair of complex zeros between two adjacent pairs of complex poles at 2FOSC. With the help of them, the proposed VCO without manual harmonic tuning with state-of-the-art FoM and wideband 1/f3 PN-corner reduction.

Architecture



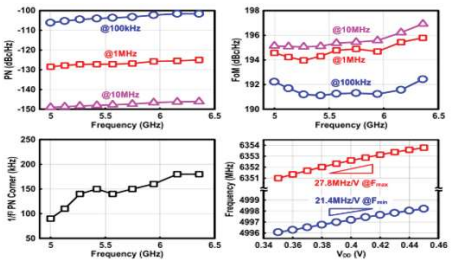
The proposed VCO tank CM magnitude and phase curves.

Implementation

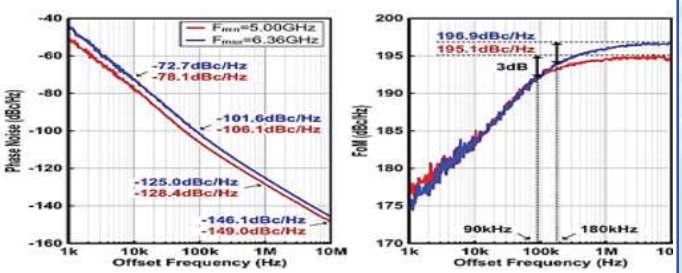


Detail of the proposed complete VCO.

Verification



Measured phase noise, 1/f3 PN corner and FoM across the frequency tuning range, and frequency pushing at Fmin and Fmax.



Measured phase noise (left) and FoM (right) at different offset frequencies.

Acknowledgement: This work was supported in part by Guangzhou Science and Technology Innovation and Development of Special Funds (GSTIC) [EF002/IME-CY/2019/GSTIC] and in part by Macau Science and Technology Development Fund (FDCT), Macau SAR [SKL-AMSV(UM)-2020-2022].

Technology Transfer Office and Commercialization Activities

In 2021, the COVID-19 pandemic has surged again in the whole world. The communications between the university and the industry were facing unprecedented difficulties. However, the professors and students of the State Key Laboratory did not slow down the pace of scientific research. With the assistance of the Technology Transfer Office, the professors carried out online discussions with enterprise experts to keep up with the pace of the industry and achieved remarkable results. 4 commercial collaboration projects were successfully concluded and received high praise from enterprises, and one of the projects was also recognized as an excellent project by the partner. 5 research cooperation projects were also progressing smoothly, three of which are in the final acceptance stage. 1 new commercial research cooperation project with a total amount of 2 million RMB was signed in 2021 and another 3 projects are in the process of contract signature. The total amount expected will be over 5 million RMB. Besides, the breakthroughs have also been made in national and government-funded projects in 2021. More than 10 projects were under research and newly approved, with a total amount of nearly 8 million RMB.

In response to the establishment of Guangdong-Macao In-depth Cooperation Zone in Hengqin, the state key laboratory invited excellent integrated circuit enterprises with potential to join the State Key Laboratory of Analog and Mixed-Signal VLSI Industry Group (AMSV-IG). Till now, the total number of AMSV-IG partners has reached 6, all of which are well-known domestic and foreign IC companies. The AMSV-IG has built an interactive communication platform for professors, students, and enterprises. Through AMSV-IG, AMSV benefitted from financial support as well as the unique advice and mentorship on critical research directions and relevant problems that only industry can provide. Industry partners gain preference and early access to AMSV's research and educational programs.

The 2021 State Key Laboratory of Analog and Mixed-Signal VLSI Industry Group Forum

Science and Technology Week 2021 cum Exhibition of Achievements on Science and Technology Innovation

Upholding Scientific Leadership in ISSCC Benchmark in terms of State-of-The-Art Chips

Academy in China	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	Total
University of Macau ★	2	1	1	3	2	3	6	7	8	6	2	4	45
Tsinghua University	1			2		1			2	5	6	9	26
HKUST	1	1	2	3	4	3	4	2	1	1		1	23
Fudan University	1	1	2	1				2	3	1		3	14
Peking University								1		1	4	5	11
Chengdu UESTC								1		3	3	1	8
Zhejiang University											2	3	5
Chinese Acad. Sci.	1		1	1							1		4
Southeast University									1	1	1		3
Univ. of S&T of China											1	2	3
Shanghai Jiaotong U.									1	1			2
Tianjin University										1		1	2
Xi'an Jiaotong U.										1			1

★★★★★★★★★★★★★★★★★★★★★
Awards and Student Research Previews (PhD) in 2011 – 2022:
★★★★★★★★★★★★★★★★★★★★★

1 x Far-East Best Paper Award (1st in China)
7 x SSCS Pre-Doctoral Achievement Awards
2 x ISSCC Silkroad Awards
1 x ISSCC Student Research Preview Award
15 x ISSCC Student Research Previews

★★★★★★★★★★★★★★★★★★★★★

Patents Granted in 2021

1. "Wireless Charging Circuit and System", US Utility Patent, Granted, No. 11,201,503 B2, December
2. "Apparatus and Method for On-Chip Microfluids Dispensing", China Patent, No. CN112449682A, WO2020024119A1 (PCT), March
3. "Wireless charging circuit, chargeable device and wireless charging system", China Patent, No. CN112421794A, February

New Academic Joined SKL AMS-VLSI in 2021 and 2022

Assistant Professor
Weihan Yu was a UM Macao Fellow at the SKL-AMSV/IME, and joined the Institute of Microelectronics as an Assistant Professor in Aug 2021. He received the B.Sc. and M.Sc. degrees in electrical and electronics engineering and Ph.D. degree in electrical and computer engineering from the University of Macao, Macao, China.

Research Interests: Radio Frequency (RF) CMOS Circuit Design and Artificial Intelligence (AI)rated Circuits.

Assistant Professor
Mingqiang Guo received his Ph.D. degree in Electrical and Computer Engineering, University of Macau, on April 2020. He will join the Institute of Microelectronics as an Assistant Professor in 2022.

Research Interest: High-speed data converters.

Assistant Professor
Yatao Peng received his Ph.D. degree in Institute of Microelectronics, University of Chinese Academy of Sciences, on July 2015. He was a Scientist in the Advanced Quantum Architecture Laboratory (AQUA), École Polytechnique Fédérale de Lausanne (EPFL), Switzerland. He will join the Institute of Microelectronics as an Assistant Professor in 2022

Research Interests: Cryogenic CMOS\SiGe BiCMOS circuits for quantum applications and radio frequency integrated circuits for wireless communication systems

Research Assistant Professor
Fangyu Mao received his Ph.D. degree in electrical and computer engineering from the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macao, Macao, China, in 2020. He will join the Institute of Microelectronics as a Research Assistant Professor in 2022.

Research Interests: include wireless power transfer and power management.

Events and Visits

Visit by a delegation of Executive Committee of Macao SAR

Visit by a delegation of Macao FDCT

Visit by a delegation from Guangdong Academy of Sciences

Visit by a delegation of the Education and Youth Development Bureau

Visit by a delegation of the Economic and Technological Development Bureau

Visit by a delegation of Macao Science Center and Guangdong Science Center

Visit by a delegation of Xinhua News Agency

Visit by students of Pui Ching Middle School

Events and Visits

Prof. Pui-In Mak from the Institute of Microelectronics (IME) delivered a speech on the 'Science and Innovation China' Greater Bay Area Innovation Forum

Publications

Major IEEE International Solid- State Circuits Conference- 15 Papers in 2021

IEEE Asian Solid-State Circuits Conference (ASSCC 2021), Nov. 2021

- "A 15.2-to-18.2GHz Balanced Dual-Core Inverse-Class-F VCO with Q-Enhanced 2nd-Harmonic Resonance Achieving 187-to-188.1dBc/Hz FoM in 28nm CMOS,"
- "A 50.4 GOPs/W FPGA-Based MobileNetV2 Accelerator using the Double-Layer MAC and DSP Efficiency Enhancement,"
- "An Arithmetic Progression Switched-Capacitor DC-DC Converter with Soft VCR Transitions Achieving 93.7% Peak Efficiency and 400 mA Output Current,"
- "A 0.46pJ/bit Ultralow-Power Entropy-Preselection-Based Strong PUF with Worst-Case BER<6.7×10-6,"
- "Auto-Calibration Technique for Current-Based Bandgap Voltage Reference,"
- "A 95% Peak Efficiency Modified KY (Boost) Converter for IoT with Continuous Flying Capacitor Charging in DCM,"
- "Modeling Attack Resistant Strong PUF Exploiting Obfuscated Interconnections With <0.83% Bit-Error Rate,"

IEEE European Solid-State Circuits Conference (ESSCIRC 2021),Sep. 2021

- "A Periodically Time-Varying Inductor Applied to the Class-D VCO for Phase Noise Improvement,"

Symposium on VLSI Circuits, Jun. 2021

- "An Auxiliary-Channel-Sharing Background Distortion and Gain CalibrationAchieving >8dB SFDR Improvement over 4th Nyquist Zone in 1GS/s ADC."
- "A 20GS/s 8b Time-Interleaved Time-Domain ADC with Input-Independent Background Timing Skew Calibration".

IEEE Custom Integrated Circuits Conference (CICC 2021), Apr. 2021

- " A Dual-Loop 4-Phase Switching LDO with Scalable Load Capability and Tunable Active Voltage Positioning for Microprocessors".
- "A 79.1dB-SNDR 20MHz-BW 2nd-Order SAR-Assisted Noise-Shaping Pipeline ADC with Gain and Offset Background Calibrations Based on Convergence Enhanced Split-Over-Time Architecture".

IEEE International Solid-State Circuits Conference (ISSCC 2021), Feb. 2021

- "A 25MHz-BW 75dB-SNDR Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC with Background Offset Calibration,"
- "A 3.5μW CMOS Vision Sensor with Illumination-Adaptive Motion Direction Detection and On-Chip Continuous Energy Havesting Cpabilities,"
- "A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz 1/f3 PN Corner Without Harmonic Tuning," [Student Research Preview]

IEEE Conferences - 16 Papers

IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2021), Nov. 2021

- "Design of Diode-Connected and Cross-Connected CMOS Rectifiers with Adaptive Tuning for RF Energy Harvesting,"
- "A real-time correlational combination algorithm to improve SNR for multi-channel neural recordings,"

4th IEEE International Conference on Integrated Circuits Technologies & Applications (ICTA 2021), Nov. 2021

- "A 0.45-V 3.3-μW Resistor-Based Temperature Sensor Achieving 10mK Resolution in 65-nm CMOS,"

The 47th Annual Conference of the IEEE Industrial Electronics Society (IECON 2021) Oct. 2021

- "An Inductive Power Transfer Converter with Irradiance-Adaptive Hybrid MPPT Control Strategy for Floating-PV System,"
- "Methodology of Inductive Power Transfer Asymmetrical Coils Design for Space-Constrained Applications,"
- "A fuzzy logic based adaptive source current THD controller for thyristor-controlled LC-coupling hybrid active power filter,"

IEEE International Conference on ASIC (ASICON 2021), Oct. 2021

- "Advances in Continuous-time MASH ΔΣ Modulators,"

International SoC Design Conference (ISOCC 2021), Oct. 2021

- "Background Timing-Skew Mismatch Calibration for Time-Interleaved ADCs,"

IEEE Midwest Symposium on Circuits and Systems (MWSCAS 2021), Aug. 2021

- "A 4-bit Mixed-Signal MAC Array with Swing Enhancement and Local Kernel Memory,"
- "On Low-Leakage CMOS Switches,"

IEEE International Symposium on Signals, Circuits and Systems (ISSCS 2021), Jul. 2021

- "A Time-Domain CMOS Temperature Sensor Using Gated Ring Oscillator With Linearity Optimization,"

IEEE Applied Power Electronics Conference and Exposition (APEC 2021), Jun. 2021

- "Always-Dual-Path Hybrid DC-DC Converter Achieving High Efficiency at Around 2:1 Step-Down Ratio,"

IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2021), Jun. 2021

- "A Sub-0.25pJ/bit 47.6-to-58.8Gb/s Reference-Less FD-Less Single-Loop PAM-4 Bang-Bang CDR with a Deliberately-Current-Mismatch Frequency Acquisition Technique in 28nm CMOS,"

IEEE International Microwave Symposium (IMS 2021), Jun. 2021

- "A 0.01mm2 1.2-pJ/bit 6.4-to-8Gb/s Reference-less FD-Less BBCDR Using a Deliberately-Clock-Selected Strobe Point Based on a 2π/3-Interval Phase,"

IEEE International Symposium on Circuits and Systems (ISCAS 2021), May 2021

- "A 3.52-GHz Harmonic-Rich-Shaping VCO with Noise Suppression and Circulation Achieving -151-dBc/Hz Phase Noise at 10-MHz Offset,"
- "Discrete-Time MASH Delta-Sigma Modulator with Second-Order Digital Noise Coupling for Wideband High-Resolution Application".

SCI Journals- 64 papers

- "A Scalable High-Current High-Accuracy Dual-Loop Four-Phase Switching LDO for Microprocessors," ***IEEE Journal of Solid-State Circuits,*** **Dec. 2021.**
- "A Two-Phase Three-Level DC-DC Buck Converter with Cross-Connected Flying Capacitors for Inductor Current Balancing," ***IEEE Transactions on Power Electronics,*** **Dec. 2021.**
- "Ratiometric fluorescence analysis for miR-141 detection with hairpin DNA-templated silver nanoclusters," ***Journal of Materials Chemistry C,*** **Dec. 2021.**
- "Cancer drug screening with an on-chip multi-drug dispenser in digital microfluidics," ***RSC Lab on a Chip,*** **Dec. 2021.**
- "A 0.15-V, 44.73% PCE charge pump with CMOS differential ring-VCO for energy harvesting systems," ***Signal Processing,*** **Dec. 2021.**
- "A 1.7-to-2.7GHz 35-38% PAE Multiband CMOS Power Amplifier Employing a Digitally-Assisted Analog Pre-distorter (DAAPD) Reconfigurable Linearization Technique," ***IEEE Transactions on Circuits and Systems II,*** **Nov. 2021.**
- "Revisiting the Frontiers of Analog and Mixed-Signal Integrated Circuits Architectures and Techniques towards the future Internet of Everything (IoE) Applications," ***Foundations and Trends in Integrated Circuits and Systems, Now,*** **Nov. 2021.**
- "A multi-path switched-capacitor-inductor hybrid DC-DC converter with reduced inductor loss and extended voltage conversion range," ***IEICE Electronics Express,*** **Dec. 2021.**
- "A 12V-to-1V switched-capacitor-assisted hybrid converter with dual-path charge conduction and zero-voltage switching," ***IEICE Electronics Express,*** **Dec. 2021.**
- "A 0.2-Terahertz Ceramic Relic Detection System Based on Iterative Threshold Filtering Imaging and Neural Network," ***Electronics,*** **Oct. 2021.**
- "A Sub-6GHz SP32T Single-Chip Switch with Nanosecond Switching Speed for 5G Communication in 0.25-μm GaAs Technology," ***Electronics,*** **Oct. 2021.**
- "Recent Advances in High-Resolution Hybrid Discrete-Time Noise-Shaping ADCs," ***IEEE Open Journal of the Solid-State Circuits Society,*** **Oct. 2021.**
- "A 1.55-to-32-Gb/s Four-Lane Fully-Integrated Transmitter with 3-Tap Feed Forward Equalizer in 28nm CMOS," ***Electronics,*** **Oct. 2021.**
- "H∞ Optimal Control Design of Static Var Compensator Coupling Hybrid Active Power Filter Based On Harmonic State-Space Modeling," ***CPSS Transactions on Power Electronics and Applications,*** **Sep. 2021.**
- "Editorial for the Special Issue on Power Quality Conditioning in Modern Power Grids Integrated Emerging Power Electronic Systems," ***CPSS Transactions on Power Electronics and Applications,*** **Sep. 2021.**
- "Guest Editorial: Modelling, Methodologies and Control Techniques of DC/AC Power Conversion Topologies for Small- and Large-scale Photovoltaic Power Systems," ***IET Power Electronics (PEL),*** **Sep. 2021.**
- "A Single-Stage Dual-Output Regulating Rectifier with Hysteretic Current-Wave Modulation," ***IEEE Journal of Solid-State Circuits,*** **Sep. 2021.**
- "A Hybrid Single-Inductor Bipolar-Output DC-DC Converter With Floating Negative Output for AMOLED Displays," ***IEEE Journal of Solid-State Circuits,*** **Sep. 2021.**
- "A 600-μm2 Ring-VCO-Based Type-II Hybrid PLL Using a 30-μW Charge-Sharing Integrator in 28-nm CMOS," ***IEEE Transactions on Circuits and Systems II,*** **Sep. 2021.**
- "A 3.36-GHz Locking-Tuned Type-I Sampling PLL with -78.6-dBc Reference Spur Merging Single-Path Reference-Feedthrough-Suppression and Narrow-Pulse-Shielding Techniques," ***IEEE Transactions on Circuits and Systems II,*** **Sep. 2021.**
- "A 0.35-V 5,200-μm2 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator," ***IEEE Journal of Solid-State Circuits,*** **Sep. 2021.**
- "An FPGA-Based Energy-Efficient Reconfigurable Convolutional Neural Network Accelerator for Object Recognition Applications," ***IEEE Transactions on Circuits and Systems II,*** **Sep. 2021.**
- "A Fully Integrated 10-V Pulse Driver Using Multiband Pulse-Frequency Modulation in 65-nm CMOS," ***IEEE Transactions on VLSI Systems,*** **Sep. 2021.**
- "Adaptive Maximum Power Point Tracking with Model-Based Negative Feedback Control and Improved V-f Model," ***IEEE Transactions on Circuits and Systems II: Express Briefs,*** **Sep. 2021.**
- "A 2.4-GHz CMOS Differential Class-DE Rectifier with Coupled Inductors," ***IEEE Transactions on Power Electronics,*** **Sep. 2021.**
- "A 6.78-MHz Single-Stage Wireless Power Receiver With Ultrafast Transient Response Using Hysteretic Control and Multilevel Current-Wave Modulation," ***IEEE Transactions on Power Electronics,*** **Sep. 2021.**
- "A 0.0285-mm2 0.68-pJ/bit Single-Loop Full-Rate Bang-Bang CDR Without Reference and Separate FD Pulling Off an 8.2(Gb/s)/μs Acquisition Speed of the PAM-4 Input in 28-nm CMOS," ***IEEE Journal of Solid-State Circuits,*** **Sep. 2021.**
- "An FPGA-Based Accelerated Architecture of Change-Point Detection for FMCW Radar Interference," ***International Journal of Circuit Theory and Applications,*** **Aug. 2021.**
- "Design and Analysis of Vector Proportional-Integral Current Controller for LC-Coupling Hybrid Active Power Filter with Minimum DC-Link Voltage," ***IEEE Transactions on Power Electronics (TPEL),*** **Aug. 2021.**
- " A Time-Interleaved 2nd-Order ΔΣ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation," ***IEEE Journal of Solid-State Circuits,*** **Aug. 2021.**
- "Temperature Tolerance Electric Cell-Substrate Impedance Sensing (ECIS) for Joint Assessment of Cell Viability and Vitality," ***ACS Sensors,*** **Aug. 2021.**
- "The Role of Renewable Energy System in Reshaping the Electrical Grid Scenario," ***IEEE Open Journal of the Industrial Electronics Society,*** **Aug. 2021.**
- "A High-Efficiency Dual-Antenna RF Energy Harvesting System using Full-Energy Extraction with Improved Input Power Response," ***IEEE Open Journal of Circuits and Systems,*** **Jul. 2021.**
- "A Highly Integrated 3-Phase 4:1 Resonant Switched-Capacitor Converter With Parasitic Loss Reduction and Fast Pre-Charge Startup," ***IEEE Transactions on Circuits and Systems II: Express Briefs,*** **Jul. 2021.**
- "A 3.3-GS/s 6-b Fully Dynamic Pipelined ADC With Linearized Dynamic Amplifier," ***IEEE Journal of Solid-State Circuits,*** **Jul. 2021.**
- "A Hybrid Boost Converter With Cross-Connected Flying Capacitors," ***IEEE Journal of Solid-State Circuits,*** **Jul. 2021.**
- "A 0.003-mm2 440fsRMS-Jitter and -64dBc-Reference-Spur Ring-VCO-Based Type-I PLL Using a Current-Reuse Sampling Phase Detector in 28-nm CMOS," ***IEEE Transactions on Circuits and Systems I,*** **Jun. 2021.**
- "A 3-Phase Resonant Switched-Capacitor Converter for Data Center 48-V Rack Power Distribution," ***IEEE Transactions on Circuits and Systems I,*** **Jun. 2021**
- "A Wide-PCE-Dynamic-Range CMOS Cross-Coupled Differential-Drive Rectifier for Ambient RF Energy Harvesting," ***IEEE Transactions on Circuits and Systems II,*** **Jun. 2021.**
- "A 40-MHz Bandwidth 75-dB SNDR Partial-Interleaving SAR-Assisted Noise-Shaping Pipeline ADC," ***IEEE Journal of Solid-State Circuits,*** **Jun. 2021.**
- "Constrained minimization of switched capacitor converter equivalent resistance by adjusting transistor sizes and duty cycles," ***Microelectronics Journal,*** **Jun. 2021.**
- "IEEE Macau Section IES Chapter 2020 Postgraduate Paper Contest [Chapter News]," ***IEEE Industrial Electronics Magazine (IEM),*** **Jun. 2021.**
- "A 6.94-fJ/Conversion-Step 12-bit 100-MS/s Asynchronous SAR ADC Exploiting Split-CDAC in 65nm CMOS," ***IEEE Access,*** **May. 2021.**
- "A 120-150GHz Power Amplifier in 28-nm CMOS Achieving 21.9-dB Gain and 11.8-dBm Psat for Sub-THz Imaging System," ***IEEE Access,*** **May. 2021.**
- "Effects of parasitic resistances on Π-source impedance networks," ***IEEE Access,*** **May. 2021.**
- "An 800 MHz-to-3.3 GHz 20-MHz Channel Bandwidth WPD CMOS Power Amplifier For Multiband Uplink Radio Transceivers," ***IEEE Transactions on Circuits and Systems II,*** **Apr. 2021.**
- "A Fully Integrated FVF LDO With Enhanced Full-Spectrum Power Supply Rejection," ***IEEE Transactions on Power Electronics,*** **Apr. 2021.**
- "Optimization of MEMS Vibration Energy Harvester with Perforated Electrode," ***Journal of Microelectromechanical Systems,*** **Apr. 2021.**
- "Bird's-eye view of Analog and Mixed-Signal Chips for the 21st Century," ***International Journal of Circuit Theory and Applications,*** **Mar. 2021.**
- "Assessment of Active and Hybrid Power Filters under Space Vector Modulation," ***IEEE Transactions on Power Electronics (TPEL),*** **Mar. 2021.**
- "Second-order sliding mode current controller for LC-coupling hybrid active power filter," ***IEEE Transactions on Industrial Electronics (TIE),*** **Mar. 2021.**
- "Wideband Variable-Gain Amplifiers Based on a Pseudo-Current-Steering Gain-Tuning Technique," ***IEEE Access,*** **Mar. 2021.**
- "A 190.3-dBc/Hz FoM 16-GHz Rotary Travelling-Wave Oscillator With Reliable Direction Contro," ***IET Electronics Letters,*** **Mar. 2021.**
- "Circuit Techniques for High Efficiency Fully-Integrated Switched-Capacitor Converters," ***IEEE Transactions on Circuits and Systems II,*** **Feb. 2021.**
- "A 7-bit 2 GS/s Time-Interleaved SAR ADC With TIming Skew Calibration Based on Current Integrating Sampler," ***IEEE Transactions on Circuits and Systems II,*** **Feb. 2021.**
- "Instantaneous Active and Reactive Load Signature applied in Non-Intrusive Load Monitoring systems," ***IET Smart Grid (SG),*** **Feb. 2021.**
- "SARS-CoV-2 RNA Detection with Duplex-Specific Nuclease Signal Amplification," ***MDPI Micromachines,*** **Feb. 2021.**
- "Design of Fast Transient Response Voltage-Mode Buck Converter with Hybrid Feedforward and Feedback Technique," ***IEEE Journal of Emerging and Selected Topics in Power Electronics,*** **Feb. 2021**
- "Spray-coated electret materials with enhanced stability in a harsh environment for an MEMS energy harvesting device," ***Microsystems & Nanoengineering,*** **Feb. 2021.**
- "Simulation of Crystalline Silicon Photovoltaic Cells for Wearable Applications," ***IEEE Access,*** **Jan. 2021.**
- "A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS," ***IEEE Transactions on Circuits and Systems I,*** **Jan. 2021.**
- "Startup Time and Energy-Reduction Techniques for Crystal Oscillators in the IoT Era," ***IEEE Transactions on Circuits and Systems II,*** **Jan. 2021.**
- "A Millimeter-Wave CMOS VCO Featuring a Mode-Ambiguity-Aware Multi-Resonant-RCLM Tank," ***IEEE Transactions on Circuits and Systems - I,*** **Jan. 2021.**
- "Review of Analog-Assisted-Digital and Digital-Assisted-Analog Low Dropout Regulators," ***IEEE Transactions on Circuits and Systems II: Express Briefs,*** **Jan. 2021.**