A Periodically Time-Varying Inductor Applied to The Class-D VCO for Phase Noise Improvement

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***Abstract* — This paper proposes a periodically time-varying (PTV) inductor applied to a class-D oscillator resulting in a 4.7V_{DD} output swing that effectively improves the phase noise in both $1/f^2$ and $1/f^3$ regions. Without extra switches, the PTV inductor is realized by reusing the original cross-coupled transistors in the class-D oscillator that semi-periodically cancel the magnetic flux between two coupled inductors. Fabricated in 65nm LP CMOS, the oscillator prototype operating at 0.35V measures FoMs of 192.5±1dBc/Hz at 1MHz offset frequency and 194.6±0.3dBc/Hz at 10MHz offset frequency, over a frequency tuning range from 3.67 to 4.43GHz.**

Keywords—Voltage-controlled oscillator (VCO), class-D oscillator, phase noise, flicker noise upconversion, common-mode resonance, periodically time-varying inductor

I. Introduction

The emerging wireless communication systems demand local oscillator (LO) signals with low phase noise to support denser modulation schemes. As a critical component in the phase-locked loop (PLL), the voltage-controlled oscillator (VCO) not only dominates the out-of-band phase noise at a large offset frequency but also substantially contributes to the phase noise at the middle offset frequency close to the PLL bandwidth. Thus it is critical to minimize VCO's phase noise in both $1/f^2$ and $1/f^3$ regions.

The conventional class-B VCO suffers from a reduced output voltage swing due to the voltage drop V_S across the tail current source or resistor, limiting its phase noise performance. Since the supply voltage V_{DD} keeps decreasing as technology scales down while Vs remains relatively constant, the output swing limitation is exacerbated in the advanced CMOS technology. The class-D VCO [1] provides a simple yet effective and stable solution to break the output swing limitation at low V_{DD} at the GHz frequency band, achieving low phase noise stably across a wide tuning range. Taking advantage of better switches with small turn-on resistance and parasitic capacitance offered by the advanced CMOS technology, the class-D VCO favored by the low-voltage applications removes the current control circuitry and reaches a peak oscillation amplitude of ~3.3V_{DD}. Since the class-D VCO is only composed of an LC tank and two large-size cross-coupled transistors mimicking ideal switches, it also benefits a compact chip area and a simple design procedure.

To minimize the phase noise in the $1/f^2$ region, the original class-D VCO [1] as shown in Fig. 1(a) adopts a single-turn inductor with a small inductance and a high-quality factor (Q). Although an excellent phase noise at the $1/f^2$ region is recorded, the class-D VCO employing a single-turn inductor is sensitive to the flicker noise upconversion, especially when oscillating at the highest frequency. As

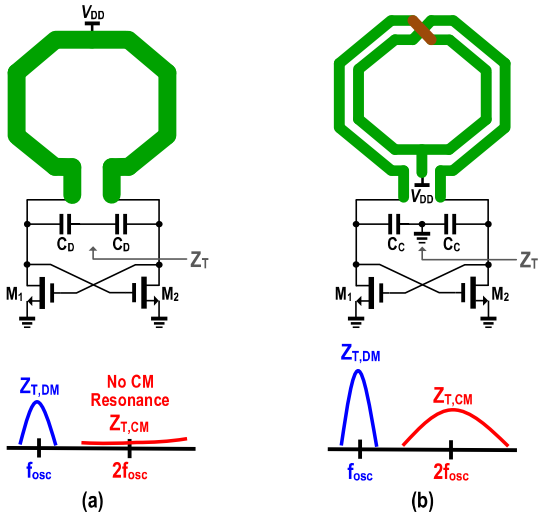

Fig. 1. Conventional class-D oscillators using (a) a single-turn inductor [1] and (b) a 2-turn F_2 inductor [3].

reported by [1], the measured $1/f^3$ phase noise corner frequency is 2.1MHz at the highest oscillation frequency (f_{osc}=4.8GHz). Since the large parasitic capacitors C_{gs} from the two cross-coupled transistors affect the tank common-mode (CM) impedance, employing a tail filter resonant at $2f_{osc}$ becomes less effective to suppress the flicker noise upconversion [2]. The measurement shows that the $1/f^3$ phase noise corner frequency is still 1.5MHz with the help of a tail filter [1], which is higher than a typical bandwidth of an LC-VCO-based PLL.

On the other hand, using an LC tank with implicit CM resonance can help to suppress the flicker noise upconversion in the class-D VCO. To locate the tank CM resonant frequency at two times of the oscillation frequency f_{osc}, [3] proposed an F2 inductor with a CM inductor to be one-forth of the differential-mode (DM) inductance L_{DM}, i.e., $L_{CM} = L_{DM}/4$. Resonant with the single-ended tank capacitors C_C, the F_2 tank achieves a CM resonant frequency at $2f_{osc}$, which effectively reduce the $1/f^3$ corner frequency of the class-D VCO to below 100kHz. However, the F_2 inductor relying on the magnetic flux cancellation to reduce L_{CM} must be realized by a 2-turn inductor with small trace space, which inevitably results in a large L_{DM} and contradicts the goal of low phase noise in the $1/f^2$ region. Typically, the L_{DM} of a 2-turn inductor with a small trace space can be three times larger than a single-turn inductor if both inductors have a similar radius. Assuming the Q is the same, using the F_2 inductor will degrade the phase noise in the $1/f^2$ region by 4.8dB according to Leeson's equation.

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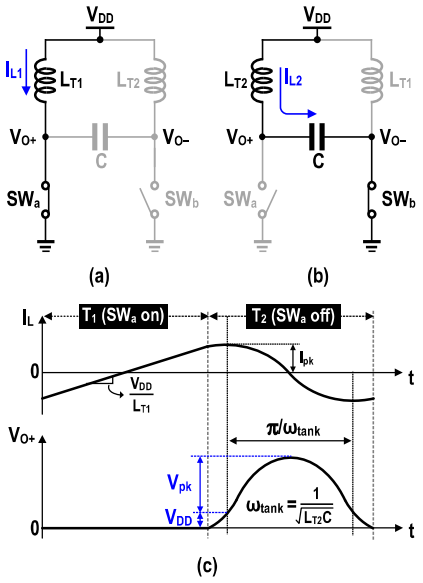

Fig. 2. Class-D oscillator operating in the semi-period of (a) T_1 and (b) T_2, and (c) the corresponding current and voltage waveform in time domain.

Aiming to improve the phase noise at both $1/f^2$ and $1/f^3$ regions for the class-D VCO, this paper proposes a periodically time-varying (PTV) inductor to boost the output voltage swing, compensating the phase noise degradation due to the use of an F_2 inductor. The PTV inductor can be realized by reusing the original cross-coupled transistors in the class-D VCO that semi-periodically cancel the magnetic flux between two coupled inductors without the need for extra switches. Compared with the class-D VCO using a single-turn inductor and a tail filter [1], our design using the proposed PTV inductor reduces the $1/f^3$ corner frequency from 1.5MHz to 450kHz while improves the phase noise at 10MHz by 2.5dB at the highest frequency.

II. Proposed Class-D VCO Using a PTV Inductor

A. Concept

The class-D VCO experiences two different working modes during one oscillation period [1]. During the first period (T_1), the switch SW_a is on, and SW_b is off [Fig. 2(a)]. Assuming that the tank inductor and SW_a are lossless, the inductor current I_{L1} ramps up linearly with time at a slope of V_{DD}/L_{T1}, where L_{T1} is the tank inductance during T_1. Entering the second semi-period (T_2), SW_a is off, and SW_b is on. The tank inductor L_{T2} and capacitor C form a series resonant tank [Fig. 2(b)]. This series resonance renders I_{L2} like a portion of sinusoid waveform with a frequency of $\omega_{tank} = \sqrt{1/L_{T2}C}$. The amplitude of the sinusoid I_{L2} during T_2 is [1]:

$$I_{pk} = \frac{2.27V_{DD}}{\omega_{tank}L_{T1}} \tag{1}$$

By integrating I_{L2} on the tank capacitor C, we obtain a sinusoidal output voltage V_{O+} with an amplitude:

$$V_{pk} = \frac{I_{PP}}{\omega_{tank}C} \tag{2}$$

In the original class-D VCO, the tank inductance is the same during both T_1 and T_2 ($L_{T1} = L_{T2}$), resulting in $V_{pk} = 2.27V_{DD}$. Thus the output voltage swing can theoretically reach $V_{DD} + V_{pk} = 3.27V_{DD}$. The above analysis also reveals that I_{PP} depends on L_{T1} while ω_{tank} depends on L_{T2}. For the same ω_{tank}, if we can make $L_{T1} < L_{T2}$, a large sinusoid current I_{L2} will be integrated into a small tank capacitor C, resulting in a boosted V_{pk}:

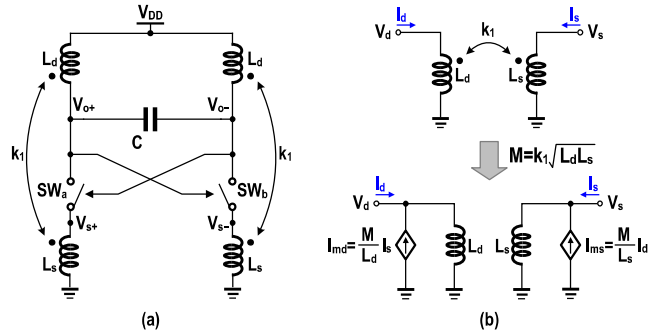

Fig. 3. (a) The implementation of PTV inductors utilizing the cross-coupled switches and the coupled inductors, and (b) the equivalent model of the coupled inductors.

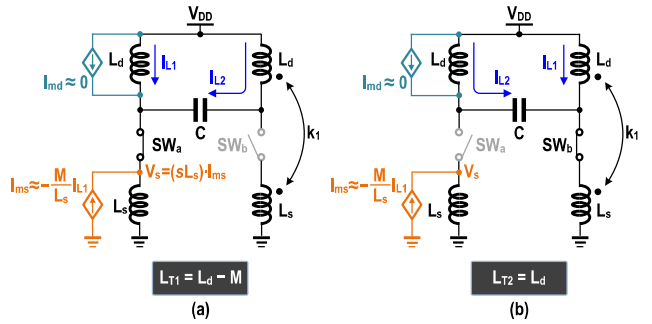

Fig. 4. (a) The circuits to derive the equivalent tank inductance in the semi-period of (b) T_1 and (c) T_2.

$$V_{pk} = 2.27V_{DD} \cdot \frac{L_{T2}}{L_{T1}} \tag{3}$$

Here, the L_{T2}/L_{T1} represents the amplitude boosting factor compared with the original class-D VCO.

B. Implementation of the PTV Inductor

In practice, we do not want to employ extra switches to vary the inductance periodically since they will inevitably introduce more noise and in turn impairs the phase noise improvement. In the implementation, the function to the change the inductance is absorbed by the original class-D switches SW_a and SW_b and the periodical inductance variation is realized by adding another inductor L_s that magnetically couples (k_1) with the tank inductor L_d as shown in Fig. 3(a).

Using the equivalent model of the coupled inductors as shown in Fig. 3(b), we can derive the equivalent tank inductance in T_1 and T_2. When SW_a is on, and SW_b is off, the left L_d is in the semi-period T_1 while the right L_d is in the semi-period T_2 [Fig. 4(a)]. During the class-D operation, the current flows through the switch mainly during a short time when the switch transits between on- and off-states. During the rest of the time, most of the tank current circulates between the tank inductors and capacitor, i.e., $I_{L1} \approx -I_{L2}$. Thus, we can assume no current flowing into L_s through SW_a during most time of T_1. Since we do not intendedly add any capacitors at the V_s node, the capacitor connected to L_s that comes from the parasitic capacitors of the switch is small, and the current from it can be ignored. In this case, the induced

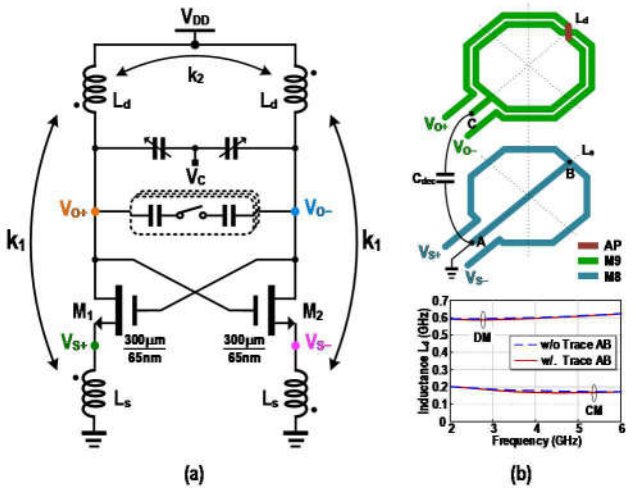

Fig. 5. (a) The detailed schematic of the class-D VCO using a PTV inductor and F_2 tank. (b) The transformer layout and EM-simulated DM and CM inductance of L_d.

current in the L_d can be ignored ($I_{md} \approx 0$) and I_{ms} just equals to $-(M/L_s)I_{L1}$, where $M = k_1\sqrt{L_dL_s}$ is the mutual inductance induced by the magnetic coupling. This I_{ms} serves to pull down V_s to a negative voltage of $-sMI_{L1}$, which increases the voltage drop across the left L_d to $V_{DD} + sMI_{L1}$ and boosts the current flowing through the left L_d during T_1 to $I_{L1} = (V_{DD} + sMI_{L1})/sL_d$. Then I_{L1} can be calculated as:

$$I_{L1} = \frac{V_{DD}}{s(L_d - M)} \tag{4}$$

It indicates that the equivalent tank inductance L_{T1} is reduced to $L_d - M$ with the help of the coupled inductor L_s.

The equivalent tank inductance L_{T2} can be founded by analyzing the left L_d in Fig. 4(b) that stays in T_2. Since the SW_a is off, the left L_d and L_s are electrically isolated. Again, by ignoring the current from the small parasitic capacitor connected to L_s, there is no induced current in the right L_d ($I_{md} \approx 0$), resulting in $L_{T2} = L_d$. With the help of the SW_a and SW_b, the coupled inductors function like a PTV inductor without the need for extra switches, offering two different equivalent tank inductances in every semi-period. The amplitude-boosting factor is now decided by the coupled inductor:

$$\frac{L_{T2}}{L_{T1}} = \frac{1}{1 - k_1\sqrt{\frac{L_s}{L_d}}} \tag{5}$$

Although the class-D VCO with a PTV inductor looks schematically similar to the transformer-feedback VCO (TF-VCO) firstly proposed in [4], their working principles are different. Yet, the TF-VCO operating in the class-B mode suffers from a degraded tank Q when the cross-coupled transistors enter into the deep triode region at a high output swing, nullifying the phase noise improvement obtained from the oscillation amplitude boosting. While in the class-D operation where the cross-coupled transistors with large sizes are adopted, a high output swing helps further to reduce the turn-on resistance of the cross-coupled transistors in T_1 and shorten the switch's transition time between on- and off-states. These all aid in suppressing the noise contribution from the cross-coupled switches.

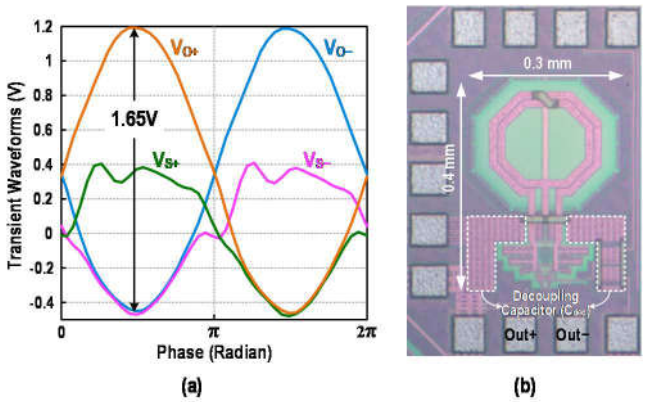

Fig. 6. (a) The simulated voltage waveform at V_{DD} = 0.35V and (b) the chip photograph.

C. VCO and F_2 Tank Design

Fig. 5(a) shows the detailed schematic of the class-D VCO using a PTV inductor. A 5-bit binary switched-capacitor array (SCA) and AMOS varactors are employed for coarse and fine frequency tuning, respectively. A fixed differential capacitor of 130fF is entailed to improve the phase noise at the highest frequency [1].

For a given L_d, increasing either k_1 or L_s helps to achieve a large amplitude-boosting factor according to (5). Since a large L_s reduces the loop gain, which impairs the startup condition, we focus on maximizing k_1 through the transformer design by stacking L_d atop of L_s as shown in Fig. 5(b). According to the EM simulation, L_d = 600pH, L_s = 192pH and k_1 = 0.87, resulting in L_{T2}/L_{T1} = 2. According to (3), $V_{pk} = 4.54V_{DD}$, and the output swing is boosted to $5.54V_{DD}$. Compared with the original class-D VCO with an output swing of $3.27V_{DD}$, our design can theoretically reduce the phase noise by 4.6dB due to the enlarged output swing according to Leeson's equation. At V_{DD} = 0.35V, the simulated output swing is $4.7V_{DD}$ as shown in Fig. 6(a), which is smaller than the prediction due to the loss from the LC tank and switches.

The stacked transformer also enables a larger coupling coefficient k_2 within the two turns of L_d, resulting in a small CM inductance $L_{d,CM}$ of 170nH due to the magnetic-flux cancellation. As verified by the simulation results [Fig. 5(b)], the routing path (AB) connecting the center tap of L_s to the ground negligibly affects the DM or CM inductance of L_d. Since there is a small differential capacitor in the tank when all the switches in the SCA are turned off, the $L_{d,CM}$ is designed to be larger than one-quarter of L_d to locate the CM resonance at the highest frequency. The low-Q CM inductance secures a low $1/f^3$ phase noise even when the ratio of CM-to-DM resonant frequencies departs from two.

The simulated Qs of L_d and L_s are 20 and 6 at 4GHz, respectively. The phase noise contributed from the loss of L_s is less critical since L_s is 3× smaller than L_d and only contributes to the output phase noise during T_1.

III. Measurement Results

The class-D VCO using a PTV inductor is prototyped in 65nm LP CMOS technology with a standard supply voltage of 1.2V, as shown in Fig. 6(b). The VCO occupies a compact area of 0.12mm^2, including a decoupling capacitor. Fig. 7 plots the phase noise measured at 3.67GHz and 4.44GHz at V_{DD} = 0.35V, which meet the cellular standards with enough

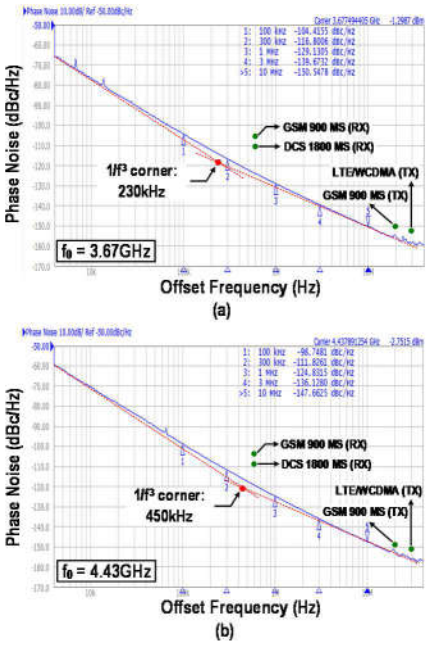

Fig. 7. Measured phase noise profiles at (a) 3.67GHz and (b) 4.44GHz.

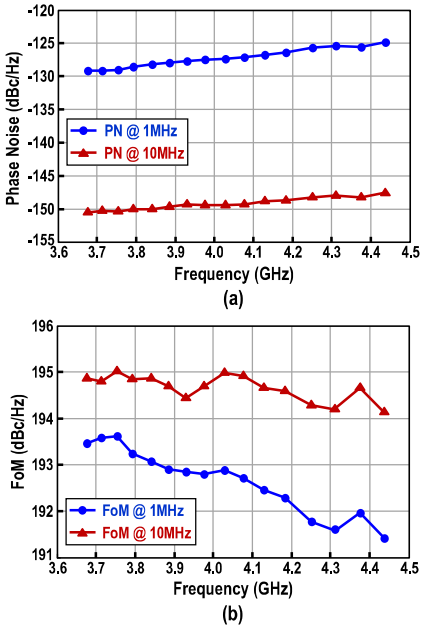

Fig. 8. Measured (a) phase noises and (b) FoMs across the frequency tuning range.

TABLE I PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUSLY PUBLISHED CLASS-D VCOS AND LOW-VOLTAGE VCOS

	JSSC'13 [1]		JSSC'13 [3]		ISSCC'19 [5]		ISSCC'21 [6]	This Work	
Toplogy	Class-D w/ Tail Filter		Class-D/F_2		Switched-Mode Folded DCO		F_2 ind.+Head Resonator	Class-D w/ PTV Ind.	
Tech.	65nm CMOS		65nm CMOS		22nm FDSOI		65nm CMOS	65nm CMOS	
V_{DD} [V]	0.4		0.5		0.15		0.4	0.35	
Tuning Range [GHz]	3.0–4.8 (45%)		3.3–4.5 (31%)		4.15–4.97 (18%)		5.0–6.36 (23.9%)	3.67–4.44 (18.7%)	
Freqeuncy [GHz]	3.0	4.8	3.3	4.5	4.15	4.97	6.36	3.68	4.44
Power [mW]	6.8	3.6	4.1	2.5	1.22	0.91	3.36	4.95	4.2
PN@1MHz [dBc/Hz]	−128	−121	−123.4	−119	−119.2	−120	−125	**−129.1**	**−124.8**
PN@10MHz [dBc/Hz]	−150	−144.5	−143.4	−139	−139.2	−142.1	−146.1	**−150.5**	**−147.6**
FoM@1MHz* [dBc/Hz]	189.2	189.1	187.6	188	190.7	194.4	195.8	193.5	191.4
FoM@10MHz* [dBc/Hz]	191.2	192.6	187.6	188	190.7	196.5	196.9	194.9	194.2
1/f³ Corner [kHz]	650	1500	60	100	60	600	180	230	450
Core Area# [mm²]	0.15		0.15		0.39		0.43	**0.12**	

Including decoupling capacitor

* $\text{FoM} = -\text{PN} + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{DC}/1\text{mW})$

margin. Fig. 8 shows the measured phase noises and FoMs across the frequency tuning range. The FoMs are stable at 1MHz offset freqeuncy (192.5±1dBc/Hz) and 10MHz offset frequency (194.6±0.3dBc/Hz) over an 18.7% tuning range. Compared with the original class-D VCO with tail filter [1], the FoMs of our design are 2.3dB better at 1MHz, and 1.6dB better at 10MHz offset. Also, the $1/f^3$ corner is reduced by 3.3× at the highest frequency. The $1/f^3$corner of our design is higher than that of the class-D/F_2 topology [3] mainly because of the added varactors for continuous frequency tuning. The frequency tuning range can be further extended by increasing the capacitor in the SCA which will increase the power consumption and degrade the FoM at low oscillation frequencies. However, the performance at the highest frequency will not be affected. Compared with [5] that can operate at a lower supply voltage of 0.15V with a high peak FoM, the phase noise of our design is at least 5.5 dB better. Although [6] can achieve better FoM, it requires an extra head resonant and a large decoupling capacitor to provide a low-impedance return path for harmonic currents. Thus the core area is 3.6× larger than our design.

IV. CONCLUSION

In this paper, a periodically time-varying (PTV) inductor that can theoretically boost the output swing of the class-D VCO to 5.5V_{DD} is presented. The boosted output swing and the F_2 tank help to improve the phase noise in both $1/f^2$ and $1/f^3$ regions. The class-D VCO using the PTV inductor achieves low phase noise and high FoMs from 3.62 to 4.44GHz and occupies a compact area.

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REFERENCES

[1] L. Fanori and P. Andreani, "Class-D CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. 48, pp. 3105-3119, Dec. 2013.

[2] D. Murphy, H. Darabi and H. Wu, "Implicit Common-Mode Resonance in LC Oscillators," *IEEE J. Solid-State Circuits*, vol. 52, pp. 812-821, Mar. 2017.

[3] M. Shahmohammadi, M. Babaie and R. B. Staszewski, "A 1/f Noise Upconversion Reduction Technique for Voltage-Biased RF CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. 51, pp. 2610-2624, Nov. 2016.

[4] K. Kwok and H. C. Luong, "Ultra-Low-Voltage High-Performance CMOS VCOs Using Transformer Feedback," *IEEE J. Solid-State Circuits*, vol. 40, pp. 652-660, Mar. 2005.

[5] O. E. -Aassar and G. M. Rebeiz, "A 0.1-to-0.2V Transformer-Based Switched-Mode Folded DCO in 22nm FDSOI with Active Step-Down Impedance Achieving 197dBc/Hz Peak FoM and 40MHz/V Frequency Pushing," *ISSCC Dig. Tech. Papers*, pp. 416-417, Feb. 2019.

[6] H. Guo, Y. Chen, P. -I. Mak and R. P. Martins, "A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning," *ISSCC Dig. Tech. Papers*, pp. 294-295, Feb. 2021.