Background Timing-Skew Mismatch Calibration for Time-Interleaved ADCs

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Abstract— **Time-interleaved ADC is widely used in high-speed applications. This structure can increase the effective sampling rate of the entire converter by multiplexing multiple ADCs in parallel. However, this architecture will be affected by mismatches between different sub-converters, including offset, gain, and timing. Timing skew will produce dynamic errors, thus posing a greater challenge. This paper presents recent state-of-the-art solutions addressing the timing skew mismatch in TI ADC through two types of background blind calibration techniques: a) methods based on deterministic equalization and b) techniques based on statistical information of the input signal.**

Keywords – Time-interleaved Converter, ADC, Timing Mismatch, Mismatch Calibration, Background Calbration.

I. INTRODUCTION

Today's system in communication infrastructure, instrumentation, as well as aerospace and defense face complex challenges that need to meet the growing demands of the increasingly crowded frequency spectrum. The wide bandwidth of a gigahertz analog-to-digital converter (ADC) allows us to capture or synthesize the entire spectrum immediately. Nyquist ADCs emerge as favorable candidates over their delta-sigma friends [1] owing to their time-interleaving (TI) availabilities and simplicity. Next, we would all focus on Nyquist ADCs.

Time-interleaved topology is an effective method to realize high-speed ADC. However, the TI structure is affected by mismatches between channels between different sub-ADCs, including offset, gain, and timing mismatch [2-8]. Compared with offset and gain mismatch, timing mismatch can cause dynamic errors proportional to the input frequency and amplitude.

The foreground calibration does not apply to applications where the converter is always 'on'. Besides, these techniques cannot track the PVT changes. Overcoming these disadvantages in foreground calibration, many previous methods proposed are background calibrations, where mismatch calibration is done in the background during regular operation of the converter. In general, there are two types of background blind calibration techniques: a) methods based on deterministic equalization and b) techniques based on statistical information of the input signal.

The convergence of deterministic calibrations is typically faster than the one based on input signal statistics. However, it needs the reference ADC to do the equalization.
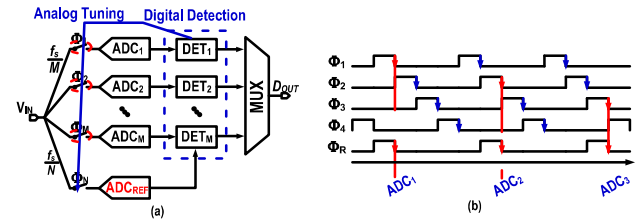

Figure 1. (a) TI ADC with a reference converter, and (b) timing diagram.

II. BACKGROUND CALIBRATION BASED ON DETERMINISTIC EQUALIZATION

The basic idea based on deterministic is to add a reference converter other than TI ADC to simultaneously sample and converter the analog input. Then we will introduce the traditional architecture assisted by the reference, and the other method used a split TI architecture.

A. TI-ADC Assisted with A Reference Converter

An M-channels TI ADC with an assisted reference converter is shown in Fig.1(a). The sub-converter is working at a sampling rate of f_s/M, and a reference ADC operating at f_s/N, where f_s is the entire ADC sample rate, while M and N are mutual prime numbers.

Fig. 1(b). exhibits the timing diagram of an example of a 4-way TI ADC with a reference ADC working at $f_s/5$. As shown in Fig.1 (b), at first, the sampling edge of Φ_R for reference coincides with the sampling edge of the ADC_1, then the second sampling edges of Φ_R coincide with the one for the second sub-ADC (Φ_2), and so on for all 4 sub-converters. This allows the digital back-end timing detection (DET) block to estimate the timing deviation based on the difference between two converters [2].

The additional reference ADC will increase power consumption and hardware overhead. In addition, it periodically changes the ADC input impedance and generates additional spurs.

B. Split TI ADC

To overcome the disadvantages of the additional reference ADC, it develops a split TI ADC [3]. Fig. 2. shows the basic idea, a TI ADC is split into two parts, with the same entire sampling rate but different interleaving channels. Similar to the TI ADC
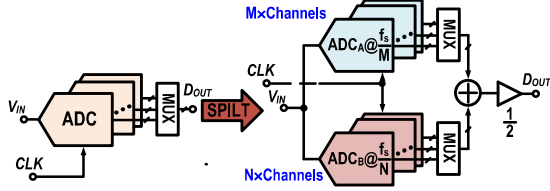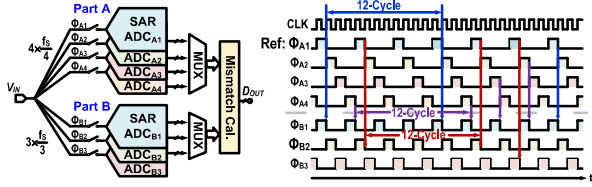
Figure 2. The split TI ADC architecture.

Figure 3. A 3/4-channel Split TI ADC: implementation and timing diagram.
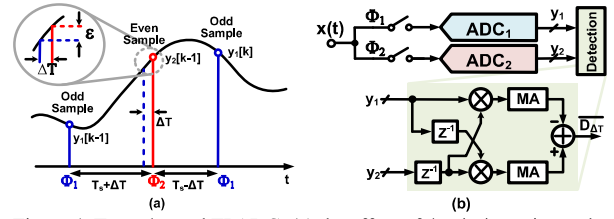

Figure 4. Two-channel TI ADC: (a) the effect of the timing mismatch, and (b) the detection topology based on autocorrelation function of the signal.

with reference converter structure, M and N must be mutual prime numbers to keep one of the sub-$ADC_{A(or\ B)}$ as the reference of sub-$ADC_{B(or\ A)}$.

Fig. 3. presents the implementation and timing diagram of a 3/4-channel split TI ADC. Each of the ADC_A and the ADC_B samples the input signal V_{in} at the falling edge of its sampling clock (Φ_{A1}-Φ_{A4}, Φ_{B1}-Φ_{B3}). Fig. 3. illustrates the sample edge of $ADC_{A1/A2/A3/A4}$ and $ADC_{B1/B2/B3}$ will meet each other after every 12 clock periods. In this way, we can use the constantly changing method of the difference between the A and B channels to calibrate the timing mismatch.

III. BACKGROUND CALIBRATION BASED ON STATISTICAL INFORMATION OF THE INPUT SIGNAL

Except for the deterministic equalization method, there is also the other types of calibration technique, which based on statistical information of the input signal. In general, the method based on statistical information of the input signal can be divided into two categories.

A. Based on the Variance

Reference [4] proposed a flash-assisted TI-SAR ADC architecture, it consists of a flash ADC that operates at the full sampling rate of the overall TI ADC. Due to the timing mismatch, the flash ADC and the SAR sample different values of the input signal, it increases the variance of the code histogram. Using the window detector (WD) [5] replace the redundancy between flash ADC and TI SAR makes this variance-based detect method can be used in more general cases.

B. Based on the Autocorrelation Function

It can usually assume that the TI-ADC input signal $x(t)$ is a wide sense stationary (WSS) signal. Therefore, the autocorrelation function of the input signal $R(\tau) = E[x_k(t)x_k(t + \tau)]$ has nothing to do the time t.

For simplicity, we only consider two-channel TI ADCs here. We use the digital mixing technique evaluates two autocorrelation functions [6], one from the moving average (MA) of the product of $y_1[k - 1]$ and $y_2[k - 1]$ and the other from $y_2[k - 1]$ and $y_1[k]$, as shown in Fig. 4(b).

Therefore, for a small value of ΔT, it can evaluate the timing mismatch information $\overline{D_{\Delta T}}$ which is proportional to the derivative of ΔT and its autocorrelation function $R(\tau)$ at $\tau = T_s$.

According to the polarity information of the timing skew ΔT, [6] and [7] use an adjustable delay line in the sampling clock generator to advance or delay the adjustment of the sampling clock until the value of $\overline{D_{\Delta T}}$ can be ignored. Reference [8] developed this digital-mixing method, which allows fully digital background calibration of timing mismatch without any additional analog circuits.

IV. CONCLUSION

This paper reviews the state-of-the-art published background timing mismatch calibration for TI-ADCs with two main directions. The deterministic equalization method has low input signal requirements of TI-ADC. Moreover, it needs a few samples to achieve enough calibration accuracy. However, it requires structural changes like an additional reference converter or split the channels. The techniques based on statistical information of signal usually are not requiring structural changes. But it has a stringent requirement for the input signal.

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