Advances in Continuous-time MASH ΔΣ Modulators

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2021 IEEE 14th International Conference on ASIC (ASICON) | 978-1-6654-3867-4/21/$31.00 ©2021 IEEE | DOI: 10.1109/ASICON52560.2021.9620480

Abstract

The maximum clock frequency of oversampled continuous-time (CT) delta sigma modulators (DSM) has increased significantly over the past decade, showing larger bandwidth capacity than their discrete-time counter parts. On the other hand, under a large clock rate, Multi-stage Noise-shaping (MASH) DSMs could achieve higher noise-shaping order while keeping good stability, when compared with their single-loop counterparts. Therefore, CT MASH DSMs are more promising to explore the maximum clock rate, thus extending the achievable signal bandwidth. Nevertheless, the accuracy of the CT loop filter is not defined well, thus resulting in the severe quantization noise leakage. Besides, inter-stage interfacing is also problematic in CT MASHs. This paper outlines recent state-of-the-art innovative solutions addressing the leakage of quantization noise and inter-stage interfacing in the CT MASH DSMs. They include architectural innovations, the improvements in circuitry and digital calibrations in the back end.

1. Introduction

The constantly increasing demand for higher data rates in wireless communication systems translates into higher bandwidth requirements for Analog-to-Digital Converters (ADCs) that are used in the wireless receivers. Recent standards e.g. 5G New Radio (NR) have pushed ADCs' bandwidth towards over 200MHz and dynamic range (DR) larger than 70dB. Due to their resistive input and implicit anti-aliasing filtering, continuous time (CT) delta-sigma modulators (DSMs) have shown that they are more favorable for the wireless applications. Driven by this, referring to the publications, CT DSMs have shown aggressive increases in signal bandwidth in the last decade. This trend is the result of advances in CMOS technologies and innovative ways to use this technology.

On the other hand, owing to a restrained oversampling ratio (OSR) for wireless applications, it is significant that the DSM needs to increase noise-shaping order to meet the quantization noise (QN) requirement. However, the loop stability is a concern when it comes to high-order noise shaping. Multi-stage noise-shaping (MASH) CT DSM architecture provides an alternative to its single-loop (SL) counterpart. By cascading some inherently stable low-order delta-sigma loops, MASH DSMs allow an aggressive high-order noise-shaping while maintaining good stability. Nevertheless, the SL architecture is usually preferred over the MASH topology owing to the QN leakage inherently existing in CT MASH DSMs. Fig.1 shows a plot of signal-noise and distortion ratio (SNDR) versus bandwidth for state-of-the-art CT DSMs [1]. As can be obviously seen, the number of CT SL DSM publications are 3 times more than that of CT MASH DSMs. Nevertheless, note that the largest bandwidth up to 465MHz was achieved by the 1-2 CT MASH DSM, presented by Dong *et al* [2]. This reflects CT MASH DSMs are more promising to push bandwidth to a more aggressive value.

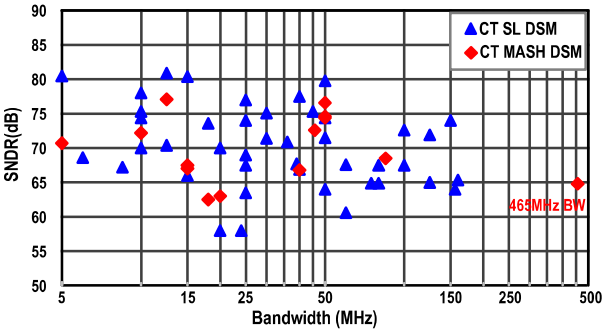

Figure 1. SNDR vs. bandwidth for state-of-the-art CT DSMs

This paper aims to give an overview of state-of-the-art CT MASH DSMs, reviewing their innovative techniques addressing issues related to CT MASH architectures, highlighting their benefits and drawbacks, as well as the discussions on future visions. The rest of this paper is organized as follows. Section 2 presents fundamental issues involved in CT MASH DSMs. Section 3 outlines the advanced techniques addressing the CT MASH fundamental issues, namely, architectural explorations, circuitry improvements and innovative calibrations in the digital backend. Section 4 makes a discussion and concludes this paper.

978-1-6654-3867-4/21/$31.00 2021 IEEE

2. Fundamental issues in CT MASH DSMs

The CT operation allows to extend the signal bandwidth and achieve much better power efficiency of operational amplifiers (op-amps), when compared with its DT counterpart. However, the CT operations give rise to two fundamental issues in MASH architectures, as described in details next.

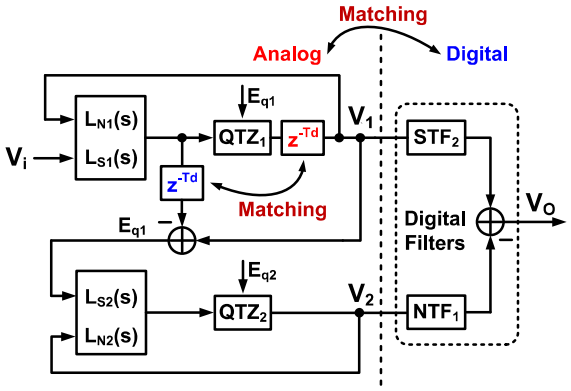

Figure 2. Block diagram of a dual-loop MASH.

2.1 Quantization noise leakage

As a basic element for CT loop filter, the coefficient of CT integrator is determined by analog RC time constant. However, such RC time constant is not so precisely defined over process variations. Thereby, it gives rise to the *mismatch* between the analog and digital filters, thus resulting in QN leakage. Although the calibration for RC time constant is a basic requirement for the CT loop stability, the calibration accuracy is usually not sufficient enough to mitigate QN leakage for high-resolution applications. Moreover, as the signal bandwidth increases, the effects of parasitic poles and zeros in the high frequency becomes more evident. It results in a much more complicated analog filter. Thereby, it is more difficult to evaluate an accurate analog filter and thus implement the digital calibration in the backend to mitigate the QN leakage.

2.2 Quantization noise extraction

Another issue exists in the CT implementation of MASH DSMs regarding the QN extraction of the first stage. The QN extraction in CT domain is not as simple as its DT counterpart [3]. The straightforward methodology is to implement the subtraction to extract the QN as its DT counterpart. However, the quantizer intrinsically comes with propagation delay whereas the input of the quantizer is a CT signal. To correctly extract the quantization error, as shown in Figure 2, a same delay must be generated intentionally for the continuous input of the first quantizer. Straightforwardly, a sample and hold circuitry can be employed to produce such delay. Nevertheless, it is not power friendly any more since it processes a full-scale signal while running at a high clock frequency.

3. Current State-of-the-art CT MASH DSMs

3.1 MASH architectural explorations

The aim of reducing the sensitivity to QN leakage for MASH architectures motivates designers to look for alternative architectures of MASH DSMs.

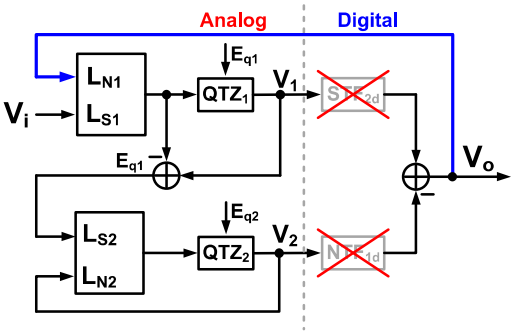

Figure 3. Block diagram of a dual-loop CT SMASH.

One of the well-known cases is the so-called *Sturdy* MASH (SMASH) DSM. The first DT SMASH DSM was proposed by Maghhari *et al* [4], and then further developed as CT implementations by Yoon *et al* [5]. As shown in Figure. 3, a dual-loop SMASH architecture is modified from the MASH. The overall output can be obtained from a direct subtraction of different stage outputs, without requiring a digital cancellation filter as in a traditional MASH topology. Moreover, the overall output is given back to the first loop such that the output of the second stage is further shaped by the noise transfer function (NTF_1) of the first stage. By implementing a unity-gain signal transfer function (STF) for the second stage, the QN of the first stage can be effectively eliminated. Yoon *et al* [5] and Qi *el al* [6] employed a first-order feedforward topology and zeroth-order stage to exhibit a unity-gain STF_2, respectively. However, it is noteworthy that the SMASH architecture is essentially a complicated SL architecture in disguise using a MASH 0-X quantizer. Thereby, it is still limited to the noise-shaping order enhancement as a general SL DSM. In other words, it does not benefit from architectural advantage of MASH in terms of loop stability.

Another trend for a relatively robust design of CT MASH DSMs is to employ 0-X MASH topology, where a pure multi-bit ADC (zeroth-order) is followed by a conventional DSM back-end stage, as conceptually shown in Figure 4. For 0-X topology, the matching requirement for analog and digital filters are not as high as a general X-Y MASH since the analog NTF_1 can be regarded as unity gain. Based on this topology, Dong *et al* [7] employed a pure feedforward topology for the second stage such that the QN of the first stage can be shaped by NTF_2 as the QN of the second stage. Thereby, this 0-3 CT MASH DSM is similar to a SMASH DSM, without using any digital cancellation filters except a digital adder. However, with the presence of QN of the

first stage in the final output, this 0-X CT MASH cannot effectively make use of an inter-stage gain to further suppress the QN of second stage. Note that the inter-stage gain is significantly useful for improving the resolution at low-OSR applications. Cenci *et al* [8] presented another 0-4 CT MASH DSM, where the QN of the first stage is eventually eliminated with using adjustable propagation delay and gain in the back-end. Thereby, a large inter-stage gain is effectively employed in this work. Nevertheless, the 0-X CT MASH works like a hybrid two-step/DSM architecture. Although it mitigates the analog-digital matching requirement for MASH, it does not benefit from the cascaded aggressive NTF shaping ability inherently presented by a general MASH topology.

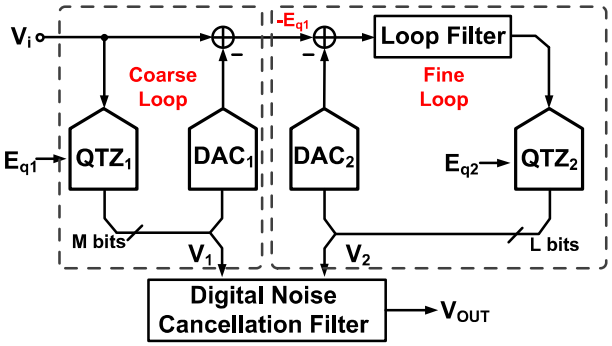

Figure 4. Block diagram of a 0-X CT MASH DSM.

3.2 Circuitry improvements

In addition to the problem of QN leakage, the connection between the stages of CT MASH DSMs is not as straightforward as that in its DT counterpart. 0-3 CT MASH [7] proposed to use an external coaxial cable to generate the analog delay, thus matching the propagation delay induced by the first coarse quantizer. Likewise, 3-1 CT SMASH [9] and 1-2 CT MASH [2] proposed to employ a RC low-pass filter and a lattice filter as an analog delay block, respectively. Nevertheless, since the inserted LPF attenuates the high-frequency component, the discrepancy between the LPF output and the output of the first quantizer gives rise to another STF peaking [9], which is not desirable in the wireless applications. Instead of a direct subtraction for QN extraction, Edward *et al* [10] presented a synthesis of 2-2 CT MASH from its original DT counterpart by using feedforward paths [10]. Moreover, this synthesis method with using feedforward paths minimizes the loading for the second stage and decreasing its signal swing without the presence of out-of-band peaking. Apart from the feedforward inter-stage connections, this work further employed high-gain multi-stage op-amps while using high-resolution RC time constant calibration, thus improving the analog-digital matching accuracy. Eventually, with combining the low OSR property [10], this work demonstrated a 50MHz bandwidth CT MASH with achieving 74.4dB SNDR while circumventing any external software calibrations.

3.3 Digital calibrations

The on-chip calibration of filters can efficiently mitigate the performance degradation due to the mismatch between analog and digital filter in CT MASH DSM. The conventional calibration is operated in analog domain [11], whose RC time constants of the analog filter are tuned using least-mean squares (LMS) engine automatically for analog-digital matching. However, the calibration fails relaxing the precision requirements of analog circuits and strong op-amps are still required. Also, analog calibration is severely limited in increasing its matching degree, which puts the limit to the high-resolution achievement.

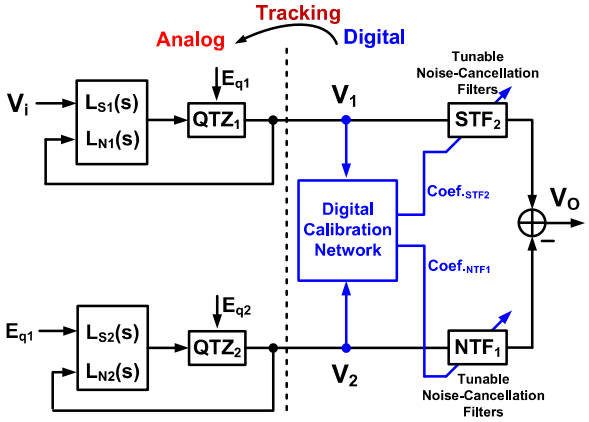

Figure 5. Block diagram of digital calibration applied in CT MASH DSMs

Consequently, it is common practice to move the calibration based on LMS algorithm to digital domain. The digital-noise-cancellation (DNC) filter coefficients are programable to track the transfer function of the analog core in digital calibration technique, as shown in Figure.5. Moreover, digital calibration behaves more flexible implements and more tolerance to non-ideal op-amps. A good example of CT MASH ADC [2] achieving 465MHz bandwidth in 28nm CMOS employs an off-chip foreground LMS digital calibration to derive fixed DNC filter coefficients which are held constant after the chip power-up determination. Nevertheless, the calibration is executed off-chip, and fails to track the variation of analog transfer function in real time due to the foreground operating mode. Thus, this calibration approach cannot cover the supply voltage and temperature corners.

On the other hand, the on-chip background calibration allows the digital filter coefficient tracking continuously, in contrast to foreground calibration. An adaptive DNC filter adopting cross-correlation (XCORR) method suitable for CT MASH DSM's analog loops [2] is

presented in [12]. The XCORR engine continuously calculates the transfer functions' coefficients of analog subloops and modifies it for the DNCF. It is verified that the XCORR-based adaptive DNCF achieves better noise cancellation even up to 10% supply variations. However, long calibration delay and incapable tracking over temporal variation are still barriers before practical uses.

Recently, Fukazawa et al. [13] proposed an on-chip digital background calibration using the LMS algorithm at the first time for the CT MASH DSM, which has successfully compensated nonidealities caused by rough low-gain op-amps and bandwidth's fluctuation related to process-voltage-temperature (PVT) variations. Particularly, the proposed multi-rate scheme, which splits LMS engines into low-rate digital backend from high-rate digital front end, reduces the inherently large power and area dissipation required by LMS algorithm under a high clock rate of data streams before decimation.

4. Discussion and Conclusion

With the help of deep nanometer process and innovative design approaches, CT DSMs have manifested themselves in achieving the maximum clock rate to the gigahertz range over the past several years. Plus, MASH topologies benefit from their aggressive noise-shaping capabilities for wideband applications, where only low values of OSR is available. Thereby, CT MASH DSMs show higher potential to push the bandwidth limit of DSM architecture while meeting the specific resolution requirement. However, CT MASH DSMs suffer from QN leakage as well as its extraction.

As a result of special architectural choices, both SMASH and 0-X MASH could significantly mitigate the sensitivity to QN leakage. However, the SMASH is not applicable to higher bandwidth as its global feedback branch is quite complicated. Likewise, the 0-X MASH does not obtain the noise-shaping contribution from the first stage, which somewhat conflicts the original intention using MASH topology. Instead, a general MASH architecture with employing low-order simple stages could potentially achieve a higher bandwidth. To address its QN leakage, the digital calibration in the back-end appears mandatory. Whereas, the calibration resolution still requires further improvement while its tracking ability in PVT variations also needs to be considered for practical uses. As for the QN correct extraction, inserting a passive LPF as an analog element can be employed as well as systematic synthesis by using feedforward paths.

Acknowledgments

This work was supported the National Key Research and Development Program of China under Grant 2019YFB2204500 and State Key Lab of ASIC and Systems of Fudan University under Grant 2021KF011.

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