A 95% Peak Efficiency Modified KY (Boost) Converter for IoT with Continuous Flying Capacitor Charging in DCM

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DC-DC converters are required to achieve high efficiency over wide loading range and compact size for IoT applications as shown in Fig. 1(a). However, many designs applied more than one control method to satisfy such requirements [1,2,4,5], which demands complex control system that involves mode selection subsystem, causing efficiency penalty and large chip area. The conventional boost converter has discontinuous output current, which degrades efficiency and output voltage ripple. As a hybrid converter with switched capacitor and inductor, the KY converter overcomes the above drawbacks. However, the charging time of the flying capacitor is seriously limited by the inner operation logic in discontinuous conduction mode (DCM) operation, resulting in small output loading capability and low efficiency.

A modified KY converter is proposed in this work with single control method achieving high efficiency over wide loading range and small silicon area. An additional power switch is inserted in series with the inductor, allowing a better charging of the flying capacitor that is not limited by the DCM period of the proposed converter. The Double-Clock-Time (DCT) control can handle sleep to standby mode, achieving ultra-low quiescent current [1], but not for a full load of hundred mA. We combine DCT control with the power switch adaptive sizing technique to achieve high efficiency and wide output current range (100,000x). A clocked-feedback resistor network (CFRN) is also proposed to further reduce the quiescent current and silicon area. The proposed KY converter is fabricated in a 65nm CMOS, with 0.158 mm^2, achieving 95% peak efficiency.

DC-DC converters usually operate in DCM in light-load condition. However, as shown in Fig. 1(b), (c) and Fig. 2(c) in the DCM operation, the flying capacitor C_f charging time of the KY converter is limited by the inductor demagnetization period (T_2) and DCM period (T_{DCM}), which degrades the output power capability and system stability. Therefore, a modified KY converter overcoming this problem is proposed as shown in Fig. 2(a). An additional power switch M_{P3} is inserted between node V_X and the power inductor L. In the T_{DCM}, M_{P3} turns off, and M_{P2} and M_{N2} remain on, as shown in Fig. 2(b), so that C_f charging time is increased from T_2 to T_2+T_{DCM}. Therefore, C_f can be fully charged in the modified KY converter, as shown in Fig. 2(c). The additional M_{P3} can also simplify the implementation of zero-current-detection (ZCD). In the conventional KY converter, when the reverse current happens, as there are two paths for the I_L to flow at node V_X, the conventional ZCD method based on the on-resistance of M_{P2} cannot detect zero current accurately. With the additional M_{P3}, we can simply detect the voltage polarity of M_{P3} to achieve ZCD and DCM operation precisely. Finally, the peak charging current I_{Cpk2} of the modified KY converter is smaller than the I_{Cpk1} of the conventional KY converter, as shown in Fig. 2(c). Therefore, the power loss caused by the C_f charging current is reduced in the proposed KY converter, resulting in enhanced power efficiency.

As is shown in Fig. 3, the proposed KY converter system contains a C_f, an L, an output capacitor C_{OUT}, power switches, a CFRN, a low power bandgap and current reference, a low dropout regulator (LDO), a DCT control block, a ZCD control block, an adaptive sizing control block, a non-overlap generator and a gate driver. The DCT control consists of a clocked comparator and double clock generators (a low power slow clock and a fast clock). The clocked comparator compares the sampled output voltage signal V_{FB_S} and V_{REF1} at the rising edge of CLK. When V_{FB_S} is smaller than V_{REF1}, V_{EN} is "high" which turns on the fast clock f_{fast} (@ 2.5 MHz). The slow clock (f_{slow}<300 kHz) determines the switching frequency, and the fast clock determines the on-time (pulse-width) of the power switch gate signal. One significant advantage of the DCT control is that the fast clock can also be regarded as an indirect current sensor sensing the load current. The fast clock operation times N is proportional to the loading current, which is to be discussed in details next.

Figure 4(a) shows the relationship among efficiency, loading current, and power switch size/width W. When the loading current increases, W should be increased to have high efficiency over a wide loading range. In the DCT control, the number of fast clock action times N is proportional to the loading current. Therefore, in this design, when N=1, only one power switch with size of W_1 is applied; when N=2, two power switches (W_1 and W_2) are applied; when N=3, three power switches (W_1, W_2 and W_3) are applied. After when the V_{EN3} signal is triggered on, it will be triggered off if N≤2 in the next switching period, as shown in Fig. 4(b). Notice that this technique does not consume additional static current.

In a power-efficient DC-DC converter, the quiescent current consumed in the feedback resistor network should be low, which leads to a large resistor and chip area. To reduce the resistor size, as shown in Fig. 4(c), (d), a CFRN is proposed. The clock comparator should compare V_{FB_s} and V_{REF1} every rising edge of f_{slow} to regulate output voltage. When V_{FB_s} is larger than V_{REF1}, V_{EN} is "low" and no action happens. Then S_{sample} should be "high" for a very short time (min_S_{sample}) to reduce current consumption. When V_{FB_s} is smaller than V_{REF1}, V_{EN} is "high" and the inductor is magnetized. Then S_{sample} is "high" as long as V_{EN}. Notice that a time delay T_D should be inserted between the clocked comparator signal CLK and S_{sample}. With this technique, 500x smaller resistor size can be achieved when V_{OUT} = 3 V and I_{FB} = 20 nA.

The design is fabricated in a 65 nm CMOS with chip area of 0.158 mm^2 (0.48 mm x 0.32 mm), as shown in Fig. 7. Fig. 5(a) shows the power efficiency vs. I_{Load} at different V_{OUT}. With f_{slow} = 150 kHz, the efficiency is >80% when I_{Load} varies from 30 µA to 100 mA at V_{OUT} = 3.1 V. The efficiency is >70% from I_{Load} ≥10 µA. The maximum efficiency is 95% when I_{Load} is 1 mA and V_{OUT} = 2.75V/3.1 V. Fig. 5 (b) shows V_X and V_Y waveforms, verifying that the C_f is charging in T_{DCM}. Fig. 5 (c) shows the load transient response when V_{IN} = 1.8 V, V_{OUT} = 2.4 V and f_{slow} = 150 kHz, with I_{Load} = 5 µA to 50 mA (10,000x). Fig. 6 shows the comparison table with the state-of-the-art DC-DC converters. This work achieves a load range coverage from 1 µA to 100 mA (100,000x), which indicates that the proposed KY DC-DC converter is suitable for IoT applications.

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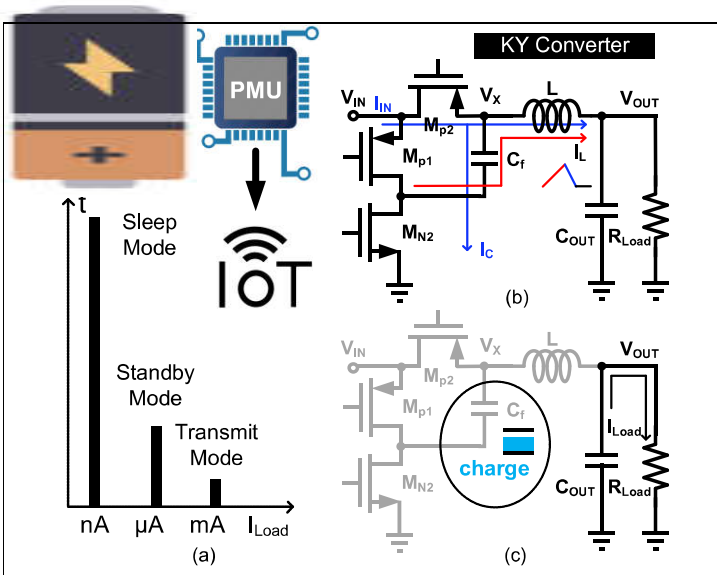


Fig. 1. (a) Typical IoT device current profile, (b) KY converter topology, and (c) KY converter operates at T_{DCM}.

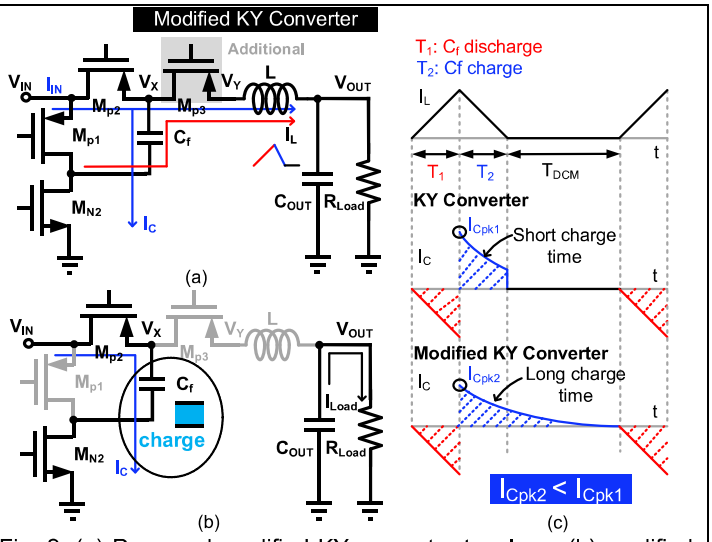


Fig. 2. (a) Proposed modified KY converter topology, (b) modified KY converter operates at T_{DCM}, and (c) I_L and I_C operation waveforms of KY and modified KY converters.

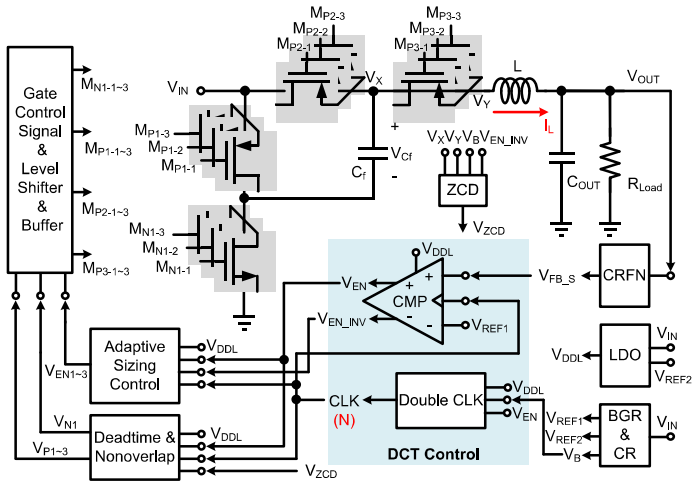
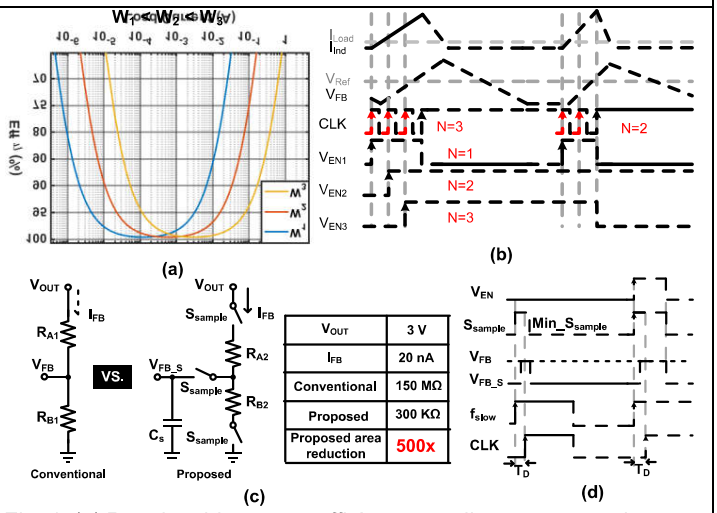


Fig. 3. System block diagram of the proposed KY converter.



V_{OUT}	3 V
I_{FB}	20 nA
Conventional	150 MΩ
Proposed	300 KΩ
Proposed area reduction	500x

Fig. 4. (a) Relationship among efficiency, loading current, and power switch size/width W, (b) DCT control operation waveforms for power switch adaptive sizing technique, (c) proposed CFRN technique, and (d) timing diagram of CFRN.

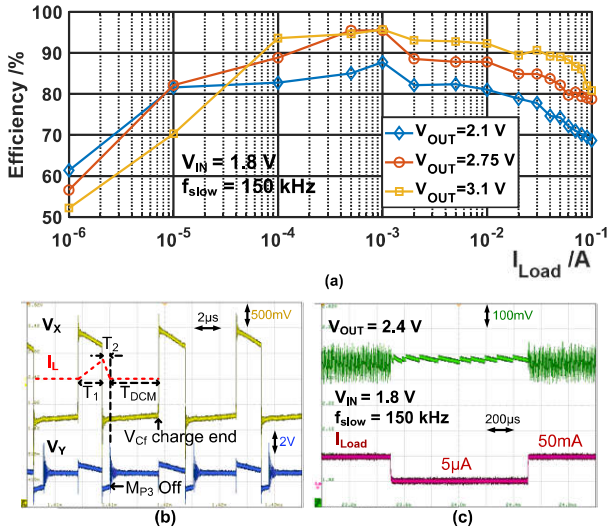


Fig. 5. Measured (a) efficiency versus I_{Load}, (b) V_X and V_Y waveforms, and (c) load transient response I_{Load} between 5μA and 50 mA.

	This work	[1]TCAS-I 2020	[2]ISSCC 2018	[3]CICC 2017	[4]JSSC 2016	[5]JSSC 2015
Process	65nm	180nm	28nm	180nm	180nm	180nm
Topology	KY (Boost)	Buck	Buck-Boost	Buck	Buck	Buck -Boost
Control Modes	DCT	DCT/ PWM	PFM/PWM/ SSM	Clocked Hysteresis	AM/PFM/ PWM	PSM/ PFM
No. of Modes	1	2	3	1	3	2
V_{IN} (V)	1.5-2.5	2.0-5.0	0.1-1.8	2.4-3.3	0.55-1	1.5-2.5
V_{OUT} (V)	2.1-3.1	0.8-3	0.4-1.4	1.5-1.6	0.35-0.5	1,1.8,3
L (μH)	4.7	2.2	10	4.7	4.7	10
C_{OUT}/C_f (μF)	9.4/2	4.7/-	1/-	1/-	4.7/-	10/-
I_{Load} (mA)	0.001-100	0.001-50	0.001-60	0.0005-10	0.0001-20	0.001-10
Efficiency (%)	93@ 10mA 70@ 10μA	93@ 10mA 86@ 10μA	83@ 10mA 76@ 10μA	87@ 10mA 88@ 10μA	92@ 10mA 79@ 10μA	70@ 10mA 82@ 10 μA
Peak_Eff (%)	95@ 1mA	95@ 5mA	89@ 30mA	90@ 1 μA	92@ 10mA	83@ 100μA
Active Area (mm^2)	0.158	0.5	0.490	0.71	0.64*	1*

*: estimated from the paper

Fig. 6. Comparison with the state-of-the-art DC-DC converters.

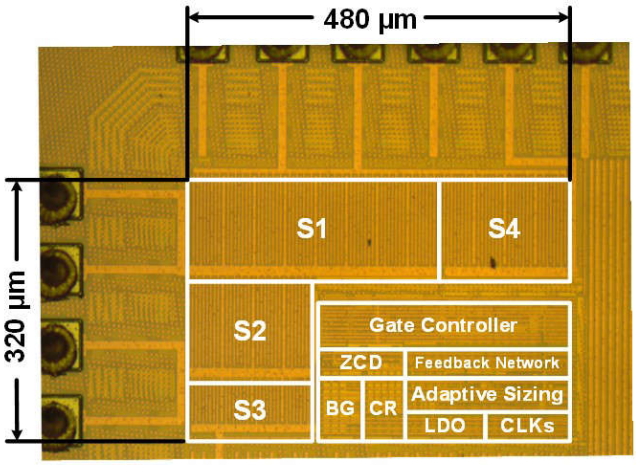


Fig. 7. Die micrograph.