Auto-Calibration Technique for Current-Based Bandgap Voltage Reference

Chi-Wa U[1], Man-Kay Law[1], Chi-Seng Lam[1], Rui P. Martins[1,2]

[1]University of Macau, Macao, China

[2]Universidade de Lisboa, Lisbon, Portugal

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For the industrial application, the bandgap voltage reference (BGR) requires calibration after fabrication to ensure accuracy [1-3] which may lead to expensive labor costs. Some BGRs in the literature were reported without trimming [4,5], however, their output voltages will drift due to device aging and stress [6]. The proposed auto-calibration technique can eliminate such a process thus saving costs. Furthermore, the β of the BJT is small in the advance process such that the variation of $\beta/(\beta+1)$ in $V_{EB}=(kT/q)ln[(I_E/I_S)\ \beta/(\beta+1)]$ has a great influence on V_{EB}, resulting in residual temperature coefficient (TC) variation after the conventional one-point trimming. This implies an error in the output, thus reduce stability and lifetime of the system.

Figure 1 shows the circuit diagram of the proposed auto-calibration technique and its operational waveforms. A conventional current-based BGR generates the reference (V_{REF}) and the calibrated (V_{CAL}) voltages. We uses a chopped comparator (CMP) to compare V_{REF} and V_{CAL} at room temperature (27°C) that produces the output V_{CMP} to activate the calibration engine. The calibration engine generates two sets of digital signals (C_{CTAT}<0:5> and C_{PTAT}<0:5>) to control the current digital-to-analog converter (IDAC) and produces the output current $mI_{PTAT}+nI_{CTAT}$ employed to bias R_{REF1}, so that V_{REF} tracks V_{CAL} iteratively. As an example, when $V_{REF}<V_{CAL}$, C_{PTAT}<0:5> increases by one and C_{CTAT}<0:5> reduces by one, that is m increases while n decreases, hence V_{REF} increases to follow V_{CAL}. The calibration engine operates complementarily when $V_{REF}>V_{CAL}$, and V_{REF} converges to V_{CAL} after multiple comparison cycles.

Figure 2 presents the circuit configuration of the current-based BGR with proposed auto-calibration technique. Two two-stage chopped amplifiers (A_1 and A_2) [i.e., $V_X=V_Y=V_{EB1}$] copy the complementary to absolute temperature (CTAT) voltage V_{EB1} to the node V_X and V_Y in order to generate the CTAT current $I_{CTAT}=(V_{EB1}/R_1)$ and the proportional to absolute temperature (PTAT) current $I_{PTAT}=[(V_{EB1}-V_{EB2})/R_2]=(kT/q)ln(N)/R_2$. Here, k is the Boltzmann constant, T is the temperature in Kevin, q is the electron charge and N=8 is the area ratio of Q_2 and Q_1. We use three basic single-stage differential amplifiers (A_3, A_4, and A_5) to control the on-resistances of M_{P7}, M_{P8}, M_{P9}, and M_{P10} such that V_{IDAC} and the drain voltages of M_{P1}, M_{P2}, and M_{P3} are equal to V_{REF}, thus eliminating channel length modulation in the current mirror. The I_{PTAT}, copied by M_{P4} to bias R_{CAL} allows the determination of $V_{CAL}=[(kT/q)ln(N)](R_{CAL}/R_2)$. As V_{CAL} depends on the physical constants and the ratio between resistors, it is insensitive to the process variation. Furthermore, an external enable signal (EN) activates this branch only when calibration is necessary to save power. M_{P5} and M_{P6} copy the CTAT and the PTAT current to bias R_{REF}, and the IDAC injects the trimming current mI_{PTAT} and nI_{CTAT} through M_{P10} to bias R_{REF1}, thus generating $V_{REF}=(mI_{PTAT}+nI_{CTAT})R_{REF1}+(I_{PTAT}+I_{CTAT})(R_{REF2}+R_{REF1})$.

Figure 3 presents the block diagram and key operational waveforms of the calibration engine. EN activates the oscillator that generates three clock signals (φ_{CMP}, φ_T, φ_P). When φ_{CMP} is high, the register updates V_{DIR} to V_{CMP}. When φ_P is high, it judges whether V_{DIR} is high or low to control the two accumulators (C_{CTAT}<0:5> and C_{PTAT}<0:5>) into plus or minus mode. The update of C_{CTAT}<0:5> and C_{PTAT}<0:5> happens when φ_T is high. If the accumulators are in plus mode, C_{PTAT}<0:5> increases by one and C_{CTAT}<0:5> reduces by one. If the accumulators are in minus mode, C_{PTAT}<0:5> reduces by one and C_{CTAT}<0:5> increases by one. Both C_{CTAT}<0:5> and C_{PTAT}<0:5> can vary from 0 to 63. Moreover, an external signal ($RESET$) can reset C_{PTAT}<0:5> to 32 and C_{CTAT}<0:5> to 31 such that half of the trimming bits are active.

Figure 4 displays the circuit of the IDAC, simulation results of $\beta/(\beta+1)$ of BJT and V_{REF} after PTAT trimming and the proposed auto-calibration technique under different process corners. Typically, the trimming of the PTAT voltage eliminates process variation [2]. However, as shown in Fig. 4, due to the variation of $\beta/(\beta+1)$ in V_{EB}, it is smaller at high temperature and is larger at low temperature in FF corner, and is larger at low temperature and smaller at high temperature in SS corner. After the conventional PTAT trimming, the $V_{REF,FF}$ becomes smaller at high temperature and larger at low temperature, while the $V_{REF,SS}$ becomes larger at high temperature and smaller at low temperature. In this case, the first-order TC of V_{REF} is large even when we apply a single-point PTAT trimming [3]. To relax this effect, we propose an IDAC where the width of the M_{IP0-5} (current mirror to copy I_{PTAT}) is 2 times larger than the width of M_{IC0-5} (current mirror to copy I_{CTAT}) in this design. For example, in the FF corner, when $V_{REF}<V_{CAL}$, C_{PTAT}<0:5> increases by one and C_{PTAT}<0:5> decreases by one, they activate two units of I_{PTAT} while disable a unit of I_{CTAT}; In SS corner when $V_{REF}>V_{CAL}$, C_{PTAT}<0:5> decreases by one and C_{PTAT}<0:5> increases by one, they disable two units of I_{PTAT} while activate a unit of I_{CTAT}. In this case, the $V_{REF,FF}$ becomes larger at high temperature and smaller at low temperature while $V_{REF,SS}$ obtains the opposite results, compared with the conventional trimming of the PTAT voltage. Consequently, we can relax the effect of the variation of $\beta/(\beta+1)$.

The design is fabricated in a 65nm CMOS process with chip area of 0.04 mm^2 (0.2 mm x 0.2 mm), as shown in Fig. 7. Figure 5 shows the measured V_{REF} across temperature (-40°C to 120°C) and V_{DD} (1.2V to 2.5V). Before trimming, the V_{REF} from -40°C to 120°C for 5 chips varies from 988.4mV to 1004.7mV, with 3σ inaccuracy ±1.91%. After applying the proposed auto-calibration technique, the V_{REF} varies from 996.5mV to 1001.6mV, with 3σ inaccuracy ±0.35%. The TC of the BGR varies from 20.6ppm/°C to 28.8ppm/°C and obtains an average TC value of 25.1ppm/°C. Fig. 5 shows the V_{REF} variation at 27°C, demonstrating a standard deviation of 0.61mV, corresponding to a 3σ/μ variation of 0.18%. The reference voltage increases by 1.64mV as the supply voltage increases by 1.3V, showing a line regulation of 0.126%/V. The TC of the BGR achieves a 3σ variation of approximately 13.34% at 1.2V V_{DD}. The current consumption of the BGR and IDAC is 810nA while the current consumption of the calibration engine is 1.37μA.

Figure 6 compares this work with the state-of-the-art current based BGRs. Compared to the BGRs with manual 1-point trimming [1], [2], the proposed BGR with auto-calibration technique achieves a comparable 3σ inaccuracy while obtains a much smaller current and area consumption. Compared to the BGR with manual 2-points trimming [3], although its TC is smaller, it requires 2-points trimming thus increasing costs inevitably. Also, the proposed BGR achieves a much smaller current consumption and better 3σ inaccuracy than [3]. Compared to the BGRs without trimming [4], [5], the proposed BGR obtains a much smaller 3σ inaccuracy. Although the TC of [4] is small, we achieve a much smaller current and area consumption. We also achieve a much smaller TC when compared with [5].

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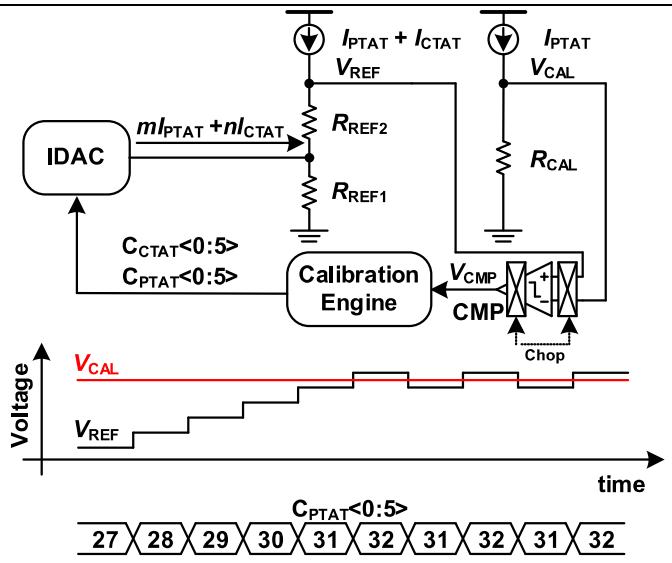

Fig. 1. Circuit diagram and operational waveforms of V_{REF}, V_{CAL} and C_{PTAT}<0:5> of the proposed auto-calibration technique.

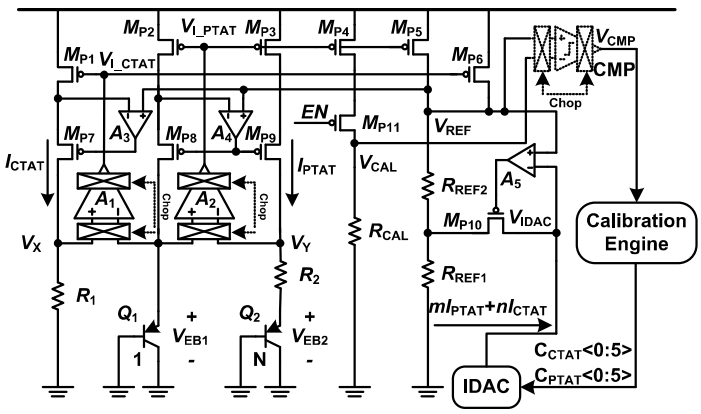

Fig. 2. Circuit configuration of the current-based BGR with proposed auto-calibration technique.

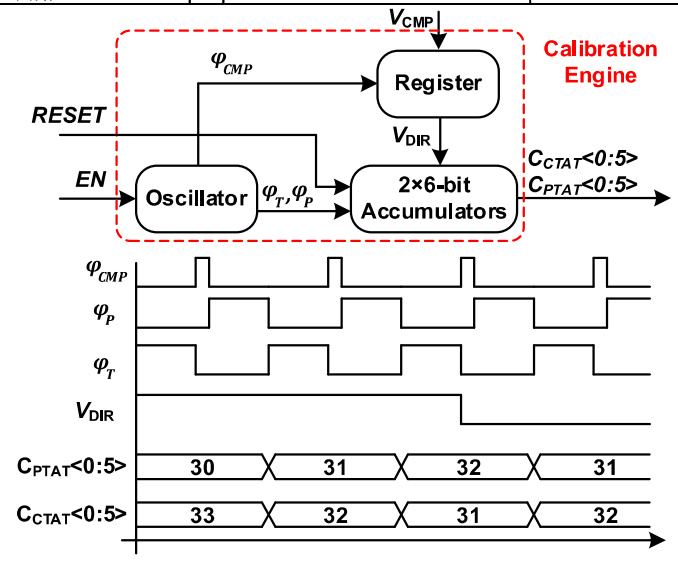

Fig. 3. Block diagram and key operational waveforms of the calibration engine.

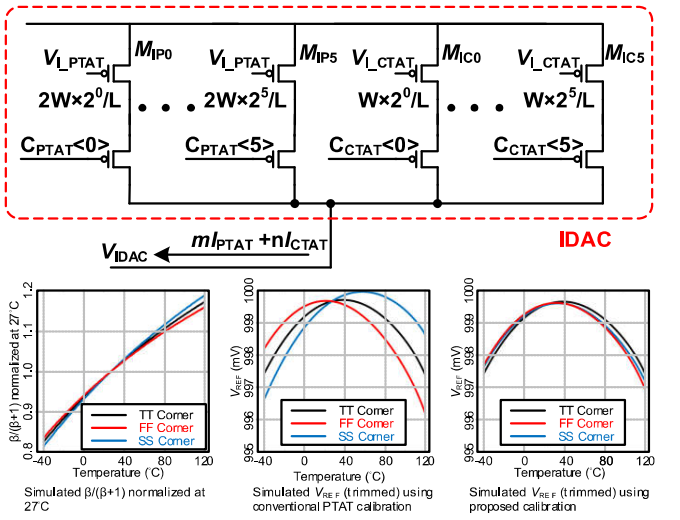

Fig. 4. Circuit of IDAC, simulation results of β/(β+1) of BJT and V_{REF} after PTAT trimming and the proposed auto-calibration technique under different process corners.

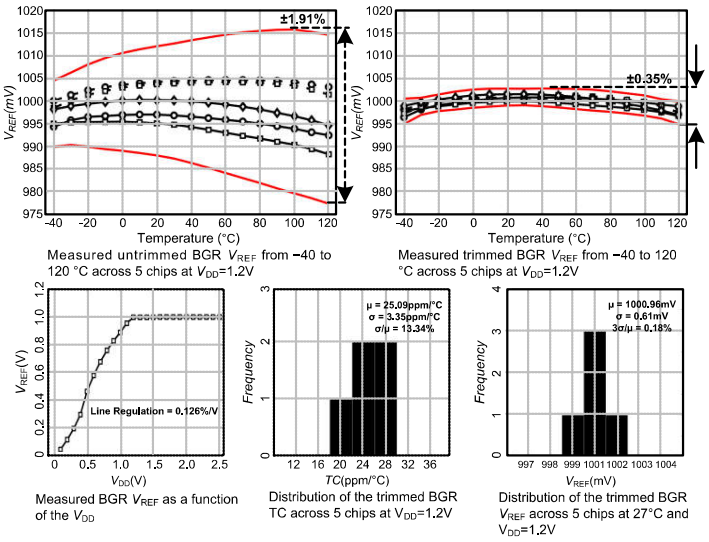

Fig. 5. Measurement results.

	This work	[1] JSSC'21	[4] JSSC'21	[3] JSSC'17	[5] JSSC'13	[2] JSSC'11
Technology	65nm	0.18μm	0.13μm	65nm	0.18μm	0.16μm
Supply Voltage (V)	1.2 – 2.5	1.8 ±10%	3.3	0.8 – 1.4	1.2 – 1.8	1.8 ±10%
Current Consumption (μA)	0.81	17	120	16.25	0.83	116
Average V_{REF} (mV)	1001.1#	1141.9#	1160	428*	1090	1087.5#
Trimming Method	Auto 1-point trim	Manual 1-point trim	Untrim	Manual 2-points trim	Untrim	Manual 1-point trim
3σ Inaccuracy @Entire Temp. Range (%)	±0.35#	(+0.02, -0.12)#	1.62	N.A.	N.A.	±0.15#
3σ Inaccuracy @Room Temp. (%)	0.18#	N.A.	N.A.	1.17*	2.21	N.A.
TC (ppm/°C)	20.6 – 28.8 (μ:25.1)#	3.2 – 5.5 (μ:4.3)#	5.8 – 13.5 (μ:8.75)	3.2 – 9.8 (μ:5.6)*	N.A. (μ:147)	5 – 12# (N.A.)
Curvature Correction	No	Yes	Yes	Yes	No	Yes
Temperature Range (°C)	-40 – 120	-40 – 125	-40 – 150	-40 – 125	-40 – 120	-40 – 125
PSRR	58 dB @DC	76 dB @DC	82 dB @10Hz	87dB @10Hz	62 dB @100Hz	74dB @DC
Active Area (mm²)	0.04	0.38	0.08	0.0104	0.0294	0.12

#1-point trimmed, *2-points trimmed

Fig. 6. Comparison of BGR metrics with other current-based BGRs.

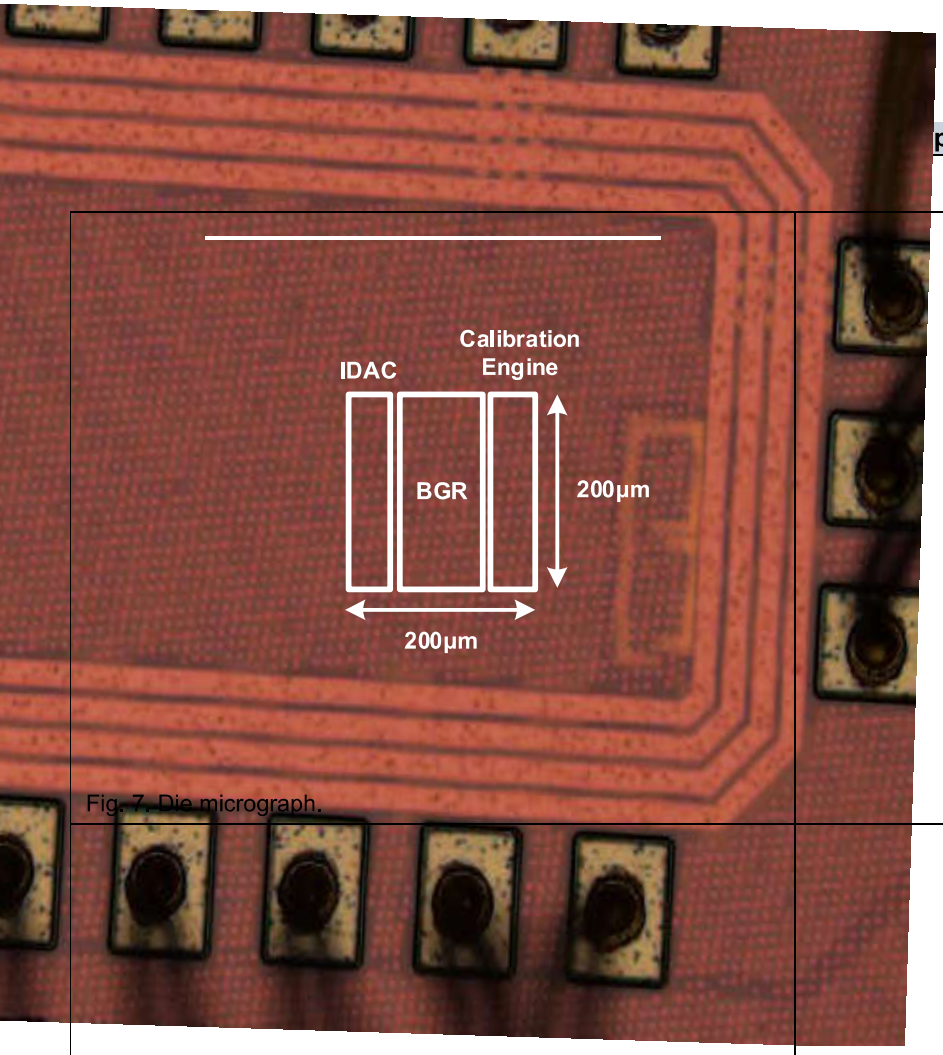

Fig. 7. Die micrograph.