

# A 0.45-V 3.3- $\mu$ W Resistor-Based Temperature Sensor Achieving 10mK Resolution in 65-nm CMOS

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**Abstract**—A 0.45-V resistor-based temperature sensor for energy-harvested Internet-of-Things device is presented. The sub-0.5-V operation is achieved by introducing a digital-intensive frequency-locked loop to convert the temperature-sensitive resistance to timing information. To overcome the high on-resistance of the transistors at sub-0.5 V, we apply gate-bulk-connected transistors to improve the on-resistance while safeguarding their leakages in the off-state. Simulated in a 65-nm CMOS process, the temperature sensor consumes 3.3  $\mu$ W at room temperature. With a 10-ms conversion time, the temperature sensor can achieve a resolution of 10 mK, resulting in a resolution FoM of 3.3 pJ·K<sup>2</sup>.

**Keywords**—CMOS, frequency-locked loop, Internet-of-Things (IoT), temperature sensor, thermistor, ultra-low-voltage.

## I. INTRODUCTION

The temperature sensor is a fundamental building block for a variety of electronic devices [1]. Especially for the Internet-of-Things (IoT) devices powered by energy-harvesting sources, it is desired to limit the power supply of the sensors to sub-0.5 V [2, 3], posing a substantial challenge for using the existing sensory circuit topologies.

The prevailing architecture for the temperature-sensing element is the bipolar-junction transistor (BJT) [4]. Yet, the emitter-base junction voltage under forward bias is  $\sim 0.5$  to 0.7 V for silicon. Hence, the BJT-based temperature sensor typically requires  $>0.85$  V to operate [4], being its limitation for sub-0.5 V applications. Alternatively, a dynamic threshold MOSFET can also be entailed [5]. As the threshold voltage downscales with the process, the minimum supply voltage ( $V_{DD}$ ) can follow. Still, it is challenge to operate the temperature sensor at sub-0.5 V.

The silicide diffusion resistor in the CMOS process is an alternative temperature-sensing element other than the BJT and MOSFET. As its resistance is temperature-sensitive, the temperature information can be measured by detecting the resistance alone. Unlike the BJT and MOSFET, there is no minimum  $V_{DD}$  requirement on the resistor. Thus, it is a promising candidate for sub-0.5 V temperature sensing. Typically, the resistance is detected by placing it in the RC-network of the oscillator/frequency-locked loop (FLL), as demonstrated in [6]. Since the oscillation is already a digital signal, additional analog-to-digital converter is averted to digitize the measurement. Still, in [6], due to its analog-intensive architecture, it entails a  $V_{DD}$  of 1 V, restricting it to be powered directly by the output of the energy harvester.

In this paper, we propose a 0.45-V resistor-based temperature sensor in 65 nm CMOS for energy-harvested IoT devices. It features a digital-intensive architecture to facilitate both technology downscaling and operation with a sub-0.5 V  $V_{DD}$ . It operates from  $-40$  to  $90^\circ\text{C}$  and achieves 10-mK resolution in 10-ms conversion time ( $t_{conv}$ ) while consuming 3.3  $\mu$ W, resulting in a resolution FoM of 3.3 pJ·K<sup>2</sup>.

## II. DESIGN AND IMPLEMENTATION

Fig. 1 manifests a simplified schematic of the proposed temperature sensor. It mainly consists of a temperature-sensitive

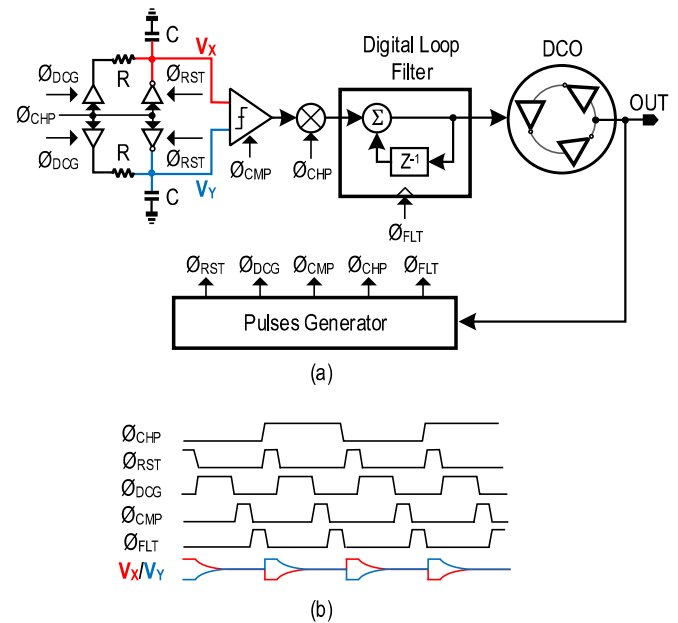


Fig. 1 (a) Schematic of the proposed resistor-based temperature sensor. (b) Timing diagram of the pulse sequences and the associated voltages on  $V_X$  and  $V_Y$ .

period-defining RC-network, a comparator, a digital loop filter, a pulse generator, and a digitally-controlled oscillator (DCO). The temperature information is extracted from the oscillation signal of the DCO, which frequency is locked by the FLL.

The resistance of the silicide diffusion resistor ( $R$ ) shows a 1<sup>st</sup>-order temperature coefficient (TC) of 2,300 ppm/K. We choose the silicide diffusion resistor attributed to its excellent linearity (2<sup>nd</sup>-order TC: 0.44 ppm/K<sup>2</sup>). In the reset phase ( $\phi_{RST}$ : logic high),  $V_X$  ( $V_Y$ ) is charged to  $V_{DD}$  (ground). Then, in the discharge phase ( $\phi_{DCG}$ : logic high),  $V_X$  ( $V_Y$ ) is discharged to ground ( $V_{DD}$ ), where the time constant is determined by  $RC$ . As  $R$  is temperature-sensitive and  $C$  (implemented as MOM capacitor) is relatively stable against temperature, the discharge rate and thus the period of the DCO within the FLL is commensurate with the temperature. In the comparison phase ( $\phi_{CMP}$ : logic high), the comparator compares  $V_X$  and  $V_Y$  and outputs a digital signal. Finally, in the data loading phase ( $\phi_{FLT}$ : logic high), the digital data is processed in the digital loop filter, which adjusts the digital words of the DCO and its frequency.

Tri-state logic gates are exploited to control the charging and discharging of the capacitors [Fig. 1(a)]. In the reset phase, the on-resistances of the switches should be low such that the capacitors charge to  $V_{DD}$ /ground swiftly. Hence, a bigger transistor is necessary. Contrarily, in the discharge phase where the outputs of the logic gates are Hi-Z, the leakage through the transistor should be minimized to enable accurate time constant, which in turn require a smaller transistor. This phenomenon is even definite in sub-0.5 V operation. To circumvent this tradeoff, we utilize gate-bulk connected transistors for the tri-state logic gates [Fig. 2(a) and (b)]. The gate-bulk connected transistor features a lower threshold voltage during the on-state, thus reducing the on-resistance. In contrast, during the off-state, it acts like regular transistors [Fig. 3(a) and (b)]. Hence, the effective width of the transistors can be reduced compared with regular transistors, and a lower leakage current can be attained.

The design of the DCO is paramount for the temperature sensor. Although the DCO's frequency is locked by the FLL, the

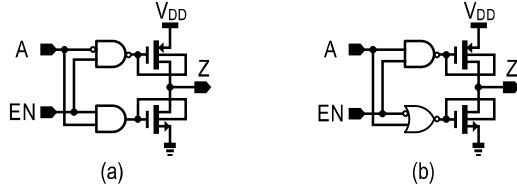


Fig. 2. Schematic of the tri-state logic gates with gate-bulk connected transistors used in the RC-network. (a) Tri-state inverter. (b) Tri-state buffer.

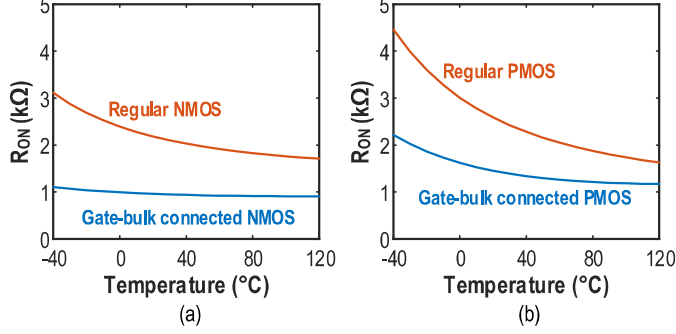


Fig. 3. On-resistances of the regular and gate-bulk connected (a) NMOS and (b) PMOS versus temperature.

frequency range of the DCO should be sufficient to cover the targeted oscillation frequency set by the RC-network. We used a 3-stage ring oscillator with digitally controlled capacitive loads to generate the desired oscillating signals. The digitally controlled capacitive load of each stage is implemented as 512 unary-coded MOS varactors. Their capacitances change according to the digital words from the loop filter.

### III. SIMULATION RESULTS

The proposed sub-0.5-V resistor-based temperature sensor was designed and simulated in CMOS 65-nm process. The power consumption at room temperature (25°C) is 3.3  $\mu$ W [Fig. 4(a)]. The power consumption is similar for temperature sensors implemented with gate-bulk connected transistors and regular transistors. Fig. 4(b) shows the output frequency versus temperature. Better linearity is achieved with the gate-bulk connected transistors as a smaller channel width can be used to reduce its leakage current at high temperature.

The frequency deviation against voltage variation is a crucial parameter for the temperature sensor. It indicates the accuracy and robustness of the sensor amid voltage variations. With a supply voltage variation from 0.4 to 0.5V, the frequency variation is decreased from 4%/V to 1.2%/V with the gate-bulk connected transistors, manifesting another advantage of the proposed technique.

A transient simulation with noise included is run to simulate the Allan deviation of the output frequency and analyze the resolution of the sensor of varying  $t_{\text{conv}}$ . The resolution of the temperature sensor is 10 mK with a  $t_{\text{conv}}$  of 10 ms (Fig. 5). For the resolution figure-of-merit (FoM) defined as  $\text{Power} \times t_{\text{conv}} \times \text{Resolution}^2$ , the FoM of the proposed temperature sensor is 3.3  $\text{pJ} \cdot \text{K}^2$ . Table I compares the performance with the prior art.

### IV. CONCLUSION

A sub-0.5-V temperature sensor for energy-harvested IoT devices is proposed. It features a resistor-based sensing element, a digital-intensive architecture and gate-bulk connected transistors for the tri-state logic gates to enable ultra-low-voltage operation. Thanks to the low  $V_{\text{DD}}$  of 0.45 V, it only consumes

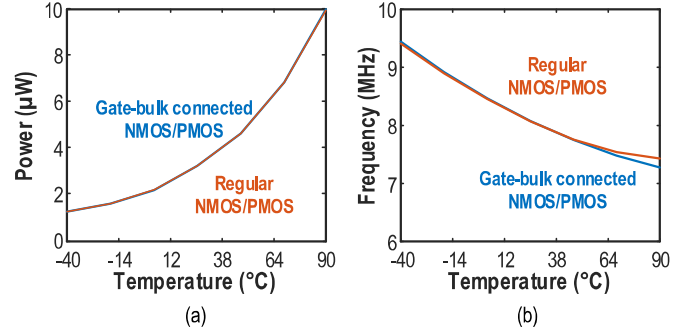


Fig. 4. (a) Power consumption and (b) FLL's output frequency of the temperature sensor with regular transistors and gate-bulk connected transistors.

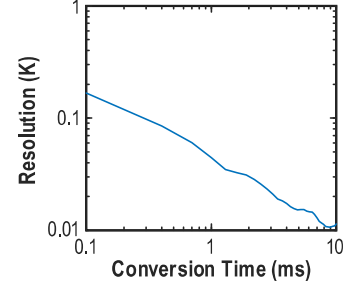


Fig. 5. The resolution of the temperature sensor versus  $t_{\text{conv}}$ .

Table I. Performance summary and comparison to state-of-the-art.

	This work*	A. Khashaba [6]	M. Eberlein [4]	K. Souri [5]
Sensing element	Resistor	Resistor	BJT	MOSFET
T-Range (°C)	-40 – 90	-30 – 90	-20 – 130	-55 – 125
Process (nm)	65	65	16	160
V <sub>DD</sub> (V)	0.4-0.5	0.95 – 1.2	0.85 – 1.0	1.6 – 2
Power ( $\mu$ W)	3.3	45	18	8.6
$t_{\text{conv}}$ (ms)	10	1	0.013	200
Resolution (mK)	10	1.43	300	33
FoM ( $\text{pJ} \cdot \text{K}^2$ )	3.3	0.092	20.7	1,873

\*Simulation results

3.3  $\mu$ W at room temperature and achieves a temperature resolution of 10 mK in 10 ms. The design is suitable for IoT devices where low-voltage and low-power operations are of utmost importance.

### ACKNOWLEDGMENT

This work is supported in part by the Research Committee (SRG2019-00188-IME) and the Macau Science and Technology Development Fund (SKL-AMSV(UM)-2020-2022).

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