RESEARCH ABSTRACTS

Power Management and Conditioning Circuits

A 0.5-V supply, 36nW bandgap reference with 42ppm/°C average temperature coefficient within -40°C to 120°C

Chi-Wa U, Wen-Liang Zeng, Man-Kay Law, Chi-Seng Lam, and Rui P. Martins

FEATURES

Low supply voltage (0.5V)

Low power consumption (36 nW)

Wide Operating temperature range (-40 – 120°C)

Switched capacitor circuits

Silicon verified in TSMC 65 nm CMOS

DESCRIPTION

This work presents a switched capacitor network (SCN)-based bandgap voltage reference (BGR) circuit with a wide temperature range, high precision, low supply voltage and low power consumption, which is suitable for IoT device application. The proposed BGR employs a 2x charge pump (CP) with an adjusted capacitor ratio to minimize the ripple to supply the V_{EB} generator, which can relax V_{DD} from 0.9V to 0.5V.A proportional to absolute temperature (PTAT) current source is proposed to bias the PNP BJT in order to reduce the nonlinearity of V_{EB}, thus improving the TC and extending the temperature range of the BGR. Moreover, a voltage divider SCN with low leakage consideration to form the complementary to absolute temperature (CTAT) voltage is designed to reduce the nonlinearity of its coefficient thus benefit for improving the TC and extending the temperature range, while a series-parallel SCN with adjusted clock swing to form the PTAT voltage is designed to improve the line regulation of the BGR. Also, four kinds of second-order effect that affect the TC of the coefficient of CTAT and PTAT voltage are studied. According to the analysis and simulation result, it can be eliminated during the design process.

The proposed SCN-based BGR was implemented in a 65nm process and occupied a chip area of 0.18 × 0.29 mm², which has an average temperature coefficient (TC) of 42 ppm/°C at 0.5V supply within − 40 °C to 120 °C. The line regulation is 3.2mV/V or 0.64%/V from 0.5V to 1V. Based on 6-chip test result, it shows a 3σ /μ variation of 3.08% before trimming, while 0.36% after trimming.

Benchmarking with the prior art, this work succeeds in extending the operating temperature range of the BJT-based BGR under a low supply voltage as well as achieved a small TC while remains a small power consumption.

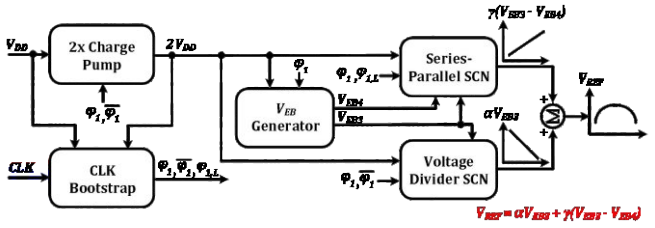


Fig. 1. Architecture of proposed BGR circuit

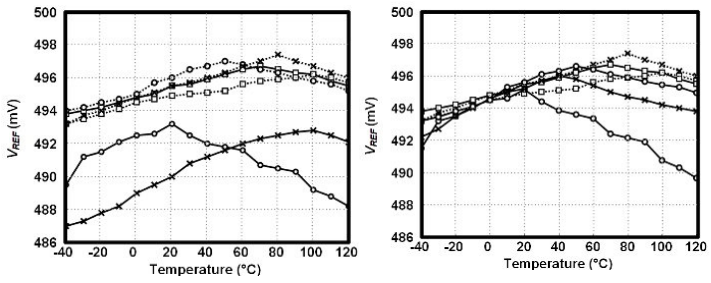


Fig. 2. The measured (a) untrimmed, (b) trimmed V_{REF} from -40 to 120 °C.

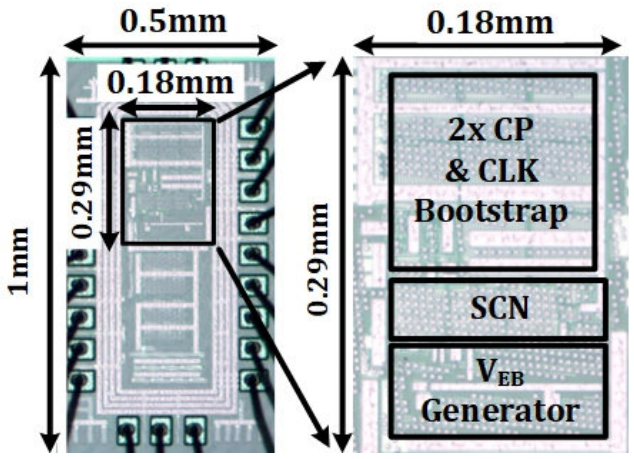


Fig. 3. Chip micrograph.

Publication(s)

[1] C.-W. U, W.-L. Zeng, M.-K. Law, C.-S. Lam, R. P. Martins, “A 0.5-V supply, 36nW bandgap reference with 42ppm/°C average temperature coefficient within -40°C to 120°C,” IEEE Transactions on Circuits and Systems I - Regular Papers, vol. 67, no. 11, pp. 3656 – 3669, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 220-MHz Bondwire-Based Fully-Integrated KY Converter with Fast Transient Response under DCM Operation

Wen-Liang Zeng, Chi-Seng Lam, Sai-Weng Sin, Franco Maloberti, Man-Chung Wong, and Rui P. Martins

FEATURES

Fully integrated, bond-wire inductor

Hybrid DC-DC converter topology (KY converter)

High efficiency and fast transient response

Silicon verified in ST 65 nm CMOS

DESCRIPTION

This design is a 220 MHz PWM fully integrated KY DC-DC step-up converter utilizing bondwire as power inductor, with discontinuous conduction mode (DCM) calibration control as shown in Fig. 1. This is the first DCM closed-loop PWM controller for the KY converter, including 1) its parameter design; 2) a DCM resulting in large voltage ripple and Right-Half-Plane Zero (RHPZ) in the power stage transfer function. KY converter comprises a switched-capacitor charge pump converter and a buck converter, and combines the advantages of both converters and exhibits the characteristics of non-pulsating output current, low output voltage ripple and no RHPZ.

Fabricated in 65-nm CMOS, the designed KY converter core occupies 0.93 mm² (shown in Fig. 2) and achieves an output conversion range of 1.5 V to 2.0 V from a 1.2 V input. The measured peak efficiency is 75.2 %@97.5 mW as shown in Fig. 3. With a 500 ps rising/falling time of the load current step (56 mA), the undershoot/overshoot is 245/205 mV at 146/140 ns recovery time, which is competitive with the state-of-the-art boost converters.

This work succeeds in developing the KY converter in integrated circuit design, which has great potential in IoT applications.

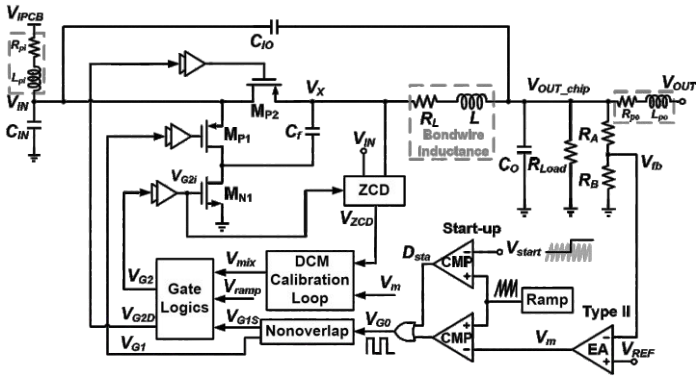


Fig. 1. System block diagram of the proposed fully integrated KY converter under DCM operation.

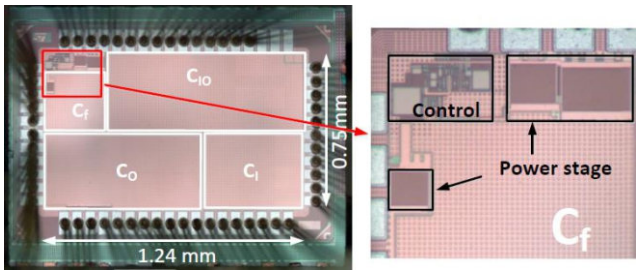


Fig. 2. Chip micrograph.

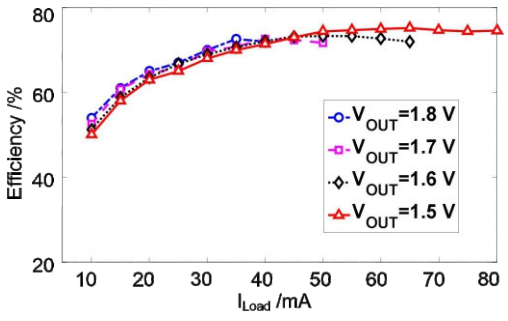


Fig. 3. Measurement power efficiency of the proposed KY converter for V_{IN} = 1.2 V and V_{OUT} = 1.5, 1.6, 1.7, 1.8 V under different load current.

Publication(s)

[1] W.-L. Zeng, C.-S. Lam, S.-W. Sin, F. Maloberti, M.-C. Wong, R. P. Martins, "A 220-MHz Bondwire-Based Fully-Integrated KY Converter with Fast Transient Response under DCM Operation", IEEE Transactions on Circuits and Systems I - Regular Papers, vol. 65, no. 11, pp. 3984 – 3995, Nov. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter with Seamless Mode Selection for IoT Application

Wen-Liang Zeng, Yuan Ren, Chi-Seng Lam, Sai-Weng Sin, Weng-Keong Che, Ran Ding, and Rui P. Martins

FEATURES

Low power consumption, 470 nA quiescent current

High efficiency, 92.7%/94.7%

Wide input voltage range from 2 V to 5 V

Wide load current range from 10 µA to 50 mA

2 control modes (DCT+PWM)

Silicon verified in SMIC 180 nm CMOS

DESCRIPTION

An ultra-low quiescent current dual-mode buck converter system is designed for IoT application, which includes a double clock time (DCT) and a pulse-width-modulation (PWM) control modes as shown in Fig. 1(a). The proposed DCT mode can reduce the conversion loss over a wide loading range from nA-to-mA and achieve seamless mode transition from DCT to PWM control. This converter achieves a peak efficiency of 92.7%/94.7% in DCT/ PWM and >80% efficiency from 10 µA to 50 mA (5000x), with a wide input voltage from 2 V to 5 V as shown in Fig. 1(b). A quiescent current of 470 nA including bandgap voltage reference and internal oscillator is achieved. The DCT-to-PWM mode selection mechanism achieves an undershoot of 80 mV at 11 µs recovery time when load current jumps from 6.67 µA to 50 mA.

The prototype is fabricated in a 0.18µm CMOS with 5 V thick oxide option, and the active area is 1x1.1 mm² with PAD-ring included, as shown in Fig. 2. Due to the proposed DCT control mode and low power DCT-to-PWM mode selection circuit, the converter achieves an I_q = 470 nA at V_{IN} = 2.0 V and V_{OUT} = 0.8 V.

This work achieves a comparable I_q and efficiency with the state-of-the-art DC-DC converters and similar product.

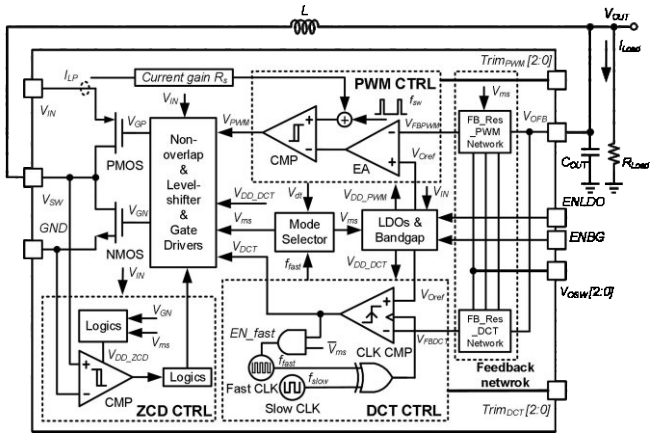


Fig. 1. System block diagram of the proposed DCT/PWM buck converter.

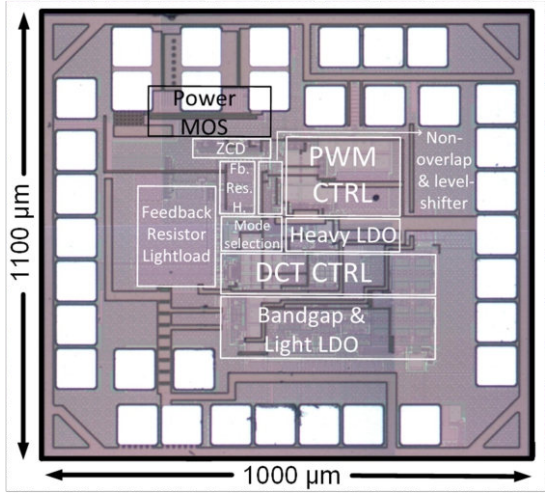


Fig. 2. Chip micrograph.

Publication(s)

[1] W.-L. Zeng, Y. Ren, C.-S. Lam, S.-W. Sin, W.-K. Che, R. Ding, R. P. Martins, "A 470nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter with Seamless Mode Transition for IoT Application", IEEE Transactions on Circuits and Systems I - Regular Papers, vol. 67, no. 11, pp. 4085 – 4098, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Allwinner Technology Co., Ltd.

A Deadbeat Current Controller of LC-Hybrid Active Power Filter for Power Quality Improvement

Wai-Kit Sou, Wai-Hei Choi, Chi-Wa Chao, Chi-Seng Lam, Cheng Gong, Chi-Kong Wong, and Man-Chung Wong

FEATURES

Fast dynamic response

Small steady-state error

Low output current ripples

DESCRIPTION

Compared with the conventional active power filter (APF), the LC-coupling hybrid active power filter (LC-HAPF) has a distinct characteristics of low DC-link operating voltage, which can lower the system and operational costs.

Conventional hysteresis PWM controller, adaptive hysteresis PWM controller, proportional-integral (PI) and proportional-resonant (PR) controller have been developed in succession for the LC-HAPF. However, they suffer from different drawbacks, such as varying frequency, large steady-state error, poor disturbance rejection, thus affecting the component design and compensation performance of LC-HAPF

This work proposes a deadbeat current controller for the LC-HAPF. The key concept of this controller is to find out the duty ratio of the switching devices in every fixed switching period based on the LC-HAPF system parameters, sampling period, sensed instantaneous load voltage, compensation current and coupling capacitor voltage signals. Moreover, the mathematical modeling, stability issue and controller's parameter design are also given and discussed.

Comparing to the existing controller of the LC-HAPF, the proposed deadbeat current controller can track with the reference compensation current with low steady-state error and fast dynamic response. Moreover, it can lead LC-HAPF to be operating at a fixed switching frequency with low output current ripples, that reducing the size of the filtering circuit.

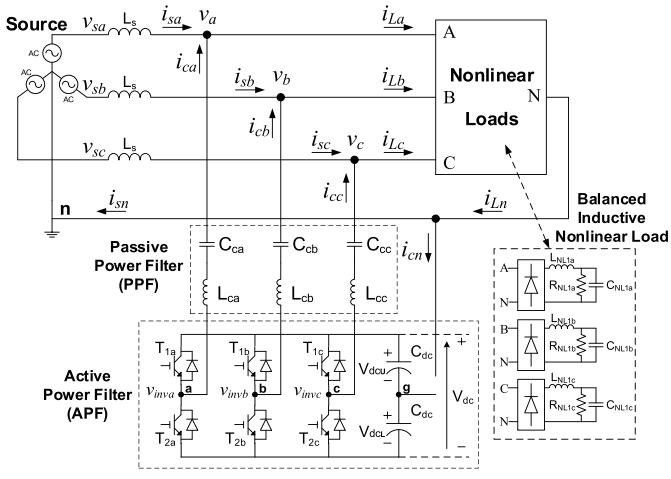


Fig. 1. System configuration of a three-phase four-wire center-split LC-HAPF.

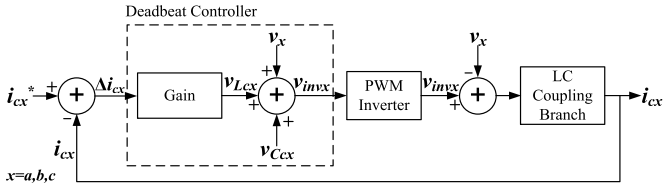


Fig. 2. Control block diagram of deadbeat current controller.

Publication(s)

[1] W.-K. Sou, W.-H. Choi, C.-W. Chao, C.-S. Lam, C. Gong, C.-K. Wong, M.-C. Wong, "A Deadbeat Current Controller of LC-Hybrid Active Power Filter for Power Quality Improvement," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 4, pp. 3891-3905, Dec. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A SAR-ADC-Assisted DC-DC Buck Converter with Fast Transient Recovery

Wen-Liang Zeng, Edoardo Bonizzoni, Chi-Wa U, Chi-Seng Lam, Sai-Weng Sin, U-Fat Chio, Franco Maloberti, and Rui P. Martins

FEATURES

Bond-wire inductor

Fast transient recovery

Low power SAR ADC included

Silicon verified in ST 65 nm CMOS

DESCRIPTION

The system block diagram of a successive-approximation-register (SAR) analog-to-digital converter (ADC) assisted DC-DC buck converter is proposed in in Fig. 1, which operates in discontinuous conduction mode (DCM) and achieves fast load transient recovery characteristics. The power inductor of the buck converter uses the bond-wire inductance. During the load transient, the dynamic low-power SAR ADC samples the converter's undershoot/overshoot output voltage and controls the programmable current pump circuit to charge/discharge the output capacitor, thus speeding up and smoothing the load transient response.

The chip fabricated in a 65-nm CMOS technology occupies an area of 1 mm² as shown in Fig. 2. The converter, switching at 100 MHZ, achieves a peak power efficiency of 81% when V_{IN} = 1.2 V, V_{OUT} = 1 V and I_{Load} = 50 mA. When the load current steps from 2 mA to 50 mA,the measured undershoot/overshoot voltage is 101/92 mV, and the recovery time is 175/406 ns.

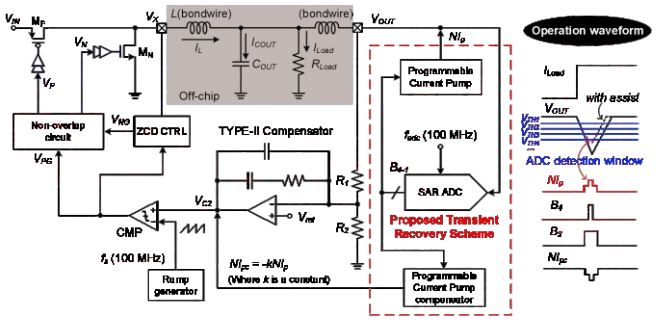


Fig. 1. System block diagram and conceptual waveforms of the proposed buck converter with the SAR assisted transient recovery scheme.

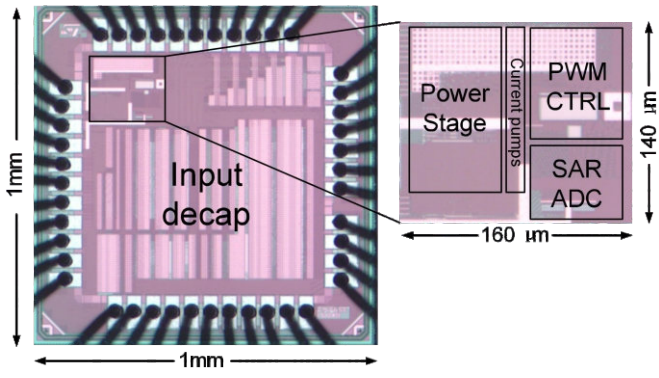


Fig. 2. Chip micrograph.

Publication(s)

[1] W.-L. Zeng, E. Bonizzoni, C.-W. U, C.-S. Lam, S.-W. Sin, U-F. Chio, F. Maloberti, and R. P. Martins, "A SAR-ADC-Assisted DC-DC Buck Converter with Fast Transient Recovery", IEEE Transactions on Circuits and Systems II - Express Briefs, vol. 67, no. 9, pp. 1669 – 1673, Sept. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging

Zhicong Huang, Chi-Seng Lam, Pui-In Mak, Rui P. Martins, Siu-Chung Wong, and Chi K. Tse

FEATURES

Single-stage IPT converter

Constant-power (CP) output

Load impedance matching (High charging efficiency)

Fixed operating frequency

Non-communication-based control

Zero voltage switching

DESCRIPTION

In general, it is challenging for an inductive power transfer (IPT) converter to achieve the required output for constant-power (CP) charging and maintain the maximum efficiency throughout the charging process while permitting fixed operating frequency, soft switching, no extra cascading converter, and no wireless feedback communication. Aimed at filling the gap of wireless CP charging, this work explores a single-stage IPT converter operating as a wireless CP and maximum-efficiency battery charger. By maintaining a constant output power rather than providing a constant output current throughout the dominant stage of battery charging, the IPT converter can make the utmost of its power capability, thus having a faster charging rate.

The proposed single-stage IPT converter adopts series–series compensation and includes a switch-controlled capacitor (SCC) and a semi-active rectifier (SAR) in the secondary side. Manipulating the SCC and the SAR to emulate the optimum impedance of the resonator and the load, we propose a novel operation approach combining the merits of load-independent transfer characteristic and load impedance matching, to achieve a simple solution to CP charging and maximum efficiency throughout the charging process. Since the control scheme is based on fixed operating frequency and secondary-side real-time regulation, no wireless feedback communication is needed for the control, and all power switches realize Zero voltage switching.

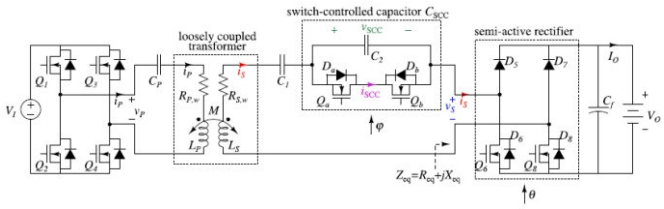


Fig. 1. Schematics of the proposed wireless CP charging system.

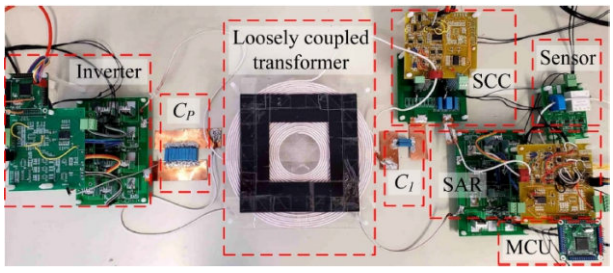


Fig. 2. Experimental Prototype of the proposed CP charging system.

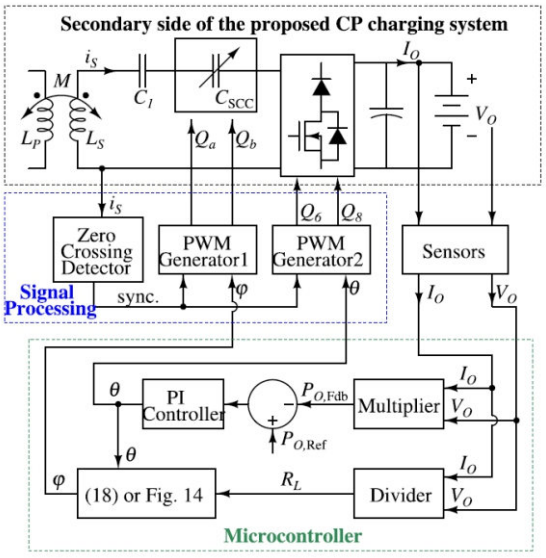


Fig. 3. Secondary load impedance matching control diagram of the proposed CP charging system.

Publication(s)

[1] Z. Huang, C.-S. Lam, P.-I. Mak, R. P. Martins, S.-C. Wong and C. K. Tse, "A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging," IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 8973-8984, Sept. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Adaptive Thyristor Controlled LC – HAPF for Reactive Power and Current Harmonics Compensation with Switching Loss Reduction

Chi-Seng Lam, Lei Wang, Sut-Ian Ho, and Man-Chung Wong

FEATURES

A simplified minimum V_{dc} calculation for thyristor controlled LC-coupling hybrid active power filter

Reduce a large number of calculation steps

Adaptive DC-link voltage controller for TCLC-HAPF in obtaining low switching loss & noise

DESCRIPTION

An adaptive DC-link voltage controlled thyristor controlled LC-coupling hybrid active power filter (TCLC-HAPF) is proposed for reducing switching loss, switching noise and enhancing the compensating performance. Unfortunately, the TCLC-HAPF has both controllable active TCLC part and active inverter part, thus the conventional minimum DC-link voltage calculation methods for active power filter (APF) and LC-coupling hybridactive power filter (LC-HAPF) cannot be directly applied to the TCLC-HAPF. Moreover, the aforementioned DC-link voltage calculation methods were developed based on the Fast Fourier Transform (FFT), which makes the calculation complex.

This work also presents a simplified minimum DC-link voltage calculation method for TCLC-HAPF reactive power and current harmonics compensation, which can significantly reduce the large amount of the calculation steps by using the FFT method. After that, an adaptive DC-link voltage controller for the TCLC-HAPF is developed to dynamically keep its operating at its minimum DC-link voltage level to reducing its switching loss and switching noise. Representative experimental results are given to verify the proposed simplified DC-link voltage calculation method and the adaptive DC-link voltage control method of TCLC-HAPF.

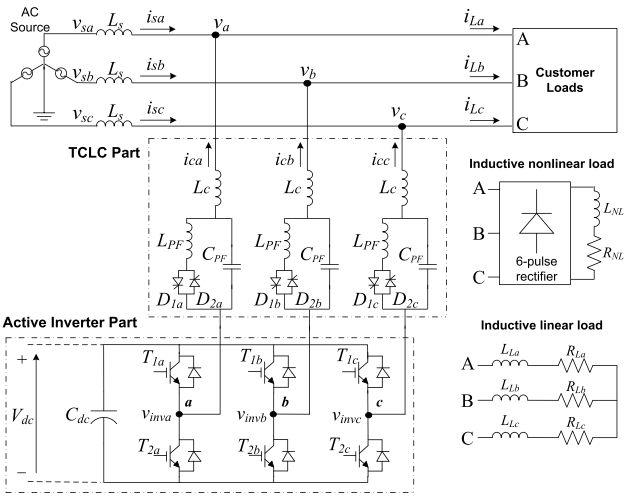


Fig. 1. Circuit configuration of a three-phase three -wire TCLC-HAPF

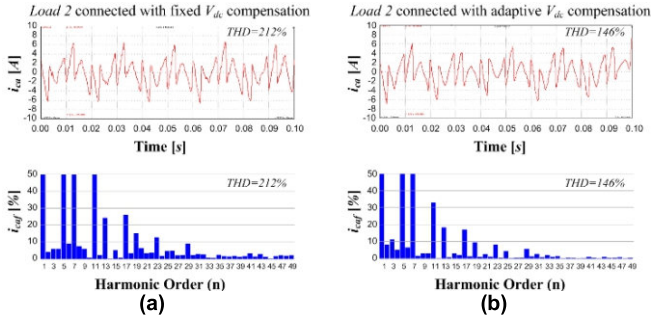


Fig. 2. Experimental i_{ca} and its frequency spectrum with: (a) fixed V_{dc}=60V and (b) adaptive V_{dc} control for Load 2.

Case:	Power Loss [W]	
	Fixed $V_{dc} = 60V$	Adaptive V_{dc}
Load 1	*141W*	*117W ($V_{dc} = 30V$), ↓17%*
Load 2	*147W*	*120W ($V_{dc} = 40V$), ↓18%*

Table 1. Experimental VSI power loss between fixed and adaptive V_{dc} controlled TCLC-HAPF

Publication(s)

[1] C.-S. Lam, L. Wang, S.-I. Ho, M.-C. Wong, "Adaptive Thyristor Controlled LC – Hybrid Active Power Filter for Reactive Power and Current Harmonics Compensation with Switching Loss Reduction," IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7577 – 7590, Oct. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Analysis, Control and Design of Hybrid Grid-Connected Inverter for Renewable Energy Generation with Power Quality Conditioning

Lei Wang, Chi-Seng Lam, and Man-Chung Wong

FEATURES

A full-bridge three-phase DC/AC inverter in series with a thyristor controlled LC filter

Wide operational range

Low DC-link voltage

DESCRIPTION

A new type DC/AC inverter named: hybrid-coupling grid-connected inverter (HGCI) for Photovoltaic (PV) active power generation with power quality conditioning is proposed, which consists of a full-bridge three-phase DC/AC inverter coupling to the power grid in series with a thyristor controlled LC (TCLC) filter. Compared with the conventional inductive-coupling grid-connected inverter (IGCI) and capacitive-coupling grid-connected inverter (CGCI), the proposed HGCI has distinct characteristics of wide operational range and low DC-link operating voltage. Based on these prominent characteristics, the system cost and operational cost can be reduced. Moreover, it can transfer the active power and compensate reactive power, unbalanced power and harmonic power simultaneously. In this paper, the analysis of the structure, parameter design and control method of the HGCI are proposed and presented. Finally, simulation and experimental results are provided to verify the effectiveness and performance of the proposed HGCI in comparison with the IGCI and CGCI.

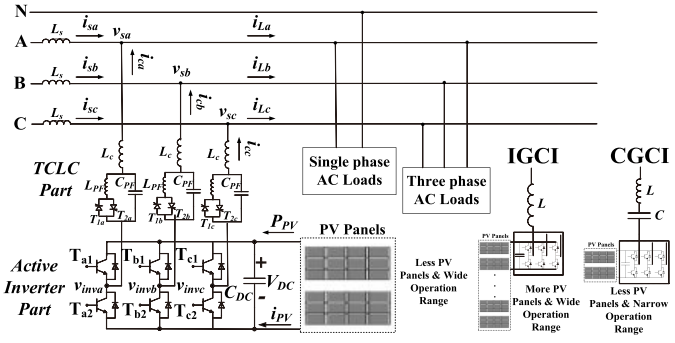
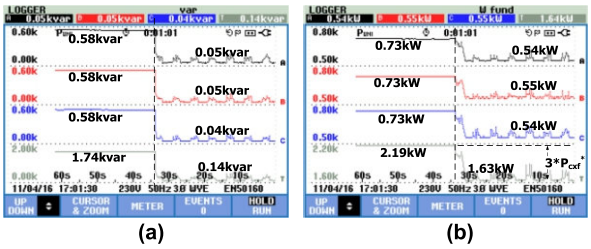


Fig. 1. The structure of the IGCI, CGCI and the proposed HGCI for PV active power injection with power quality conditioning.



(a) (b)

Fig. 3. Dynamic balanced inductive loads compensation by using the HGCI: (a) Q_{sxf} (reactive power compensation) and (b) P_{sxf} (active power injection).

Fig. 2. Experimental setup of the 110V-10A HGCI experimental prototype.

Publication(s)

[1] L. Wang, C.-S. Lam, M.-C. Wong, "Analysis, control, and design of a hybrid grid-connected inverter for renewable energy generation with power quality conditioning", IEEE Transactions on Power Electronics, vol. 33, no. 8, pp. 6755 – 6768, Aug. 2018

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter

Zhicong Huang, Zhijian Fang, Chi-Seng Lam, Pui-In Mak, and Rui P. Martins

FEATURES

Load-independent-voltage outputs with ZPA input

Efficiency enhancement

Optimization of the compensation capacitance cost

DESCRIPTION

Load-independent output with zero-phase angle (ZPA) input is desirable in wireless inductive power transfer (IPT) converters for effective power delivery, but it usually greatly relies on the parameters of the loosely coupled transformer, normally fixed or constrained by space. However, customizable outputs cannot be readily achieved unless a new transformer is redesigned. Thus, in this work, a cost-effective compensation design is elaborated to achieve customizable LIV outputs with ZPA input and optimized power efficiency for the S/SP IPT converter. Parameters of three compensation capacitors of a S/SP IPT converter were indicated by a single factor μ, which simplifies the analysis of the relationships among compensation parameters, customizable LIV outputs with ZPA input, power efficiency, and overall compensation capacitance cost. Critical values of μ ensuring load impedance matching for optimized efficiency, achieving minimum overall compensation capacitance and limiting overall compensation capacitance for effective cost were respectively derived for guiding the design.

Compared with a conventional design, the proposed design provides custom ranges of LIV outputs in both a weak and a relatively strong coupling condition, with over 5.9% and 5% efficiency improvement, respectively. The overall compensation capacitance can also be reduced by up to 37% and 21.5%, respectively.

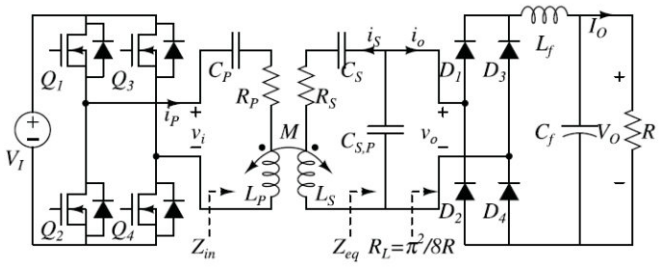


Fig. 1. (a) Schematics and (b) equivalent circuit model of the S/SP IPT converter.

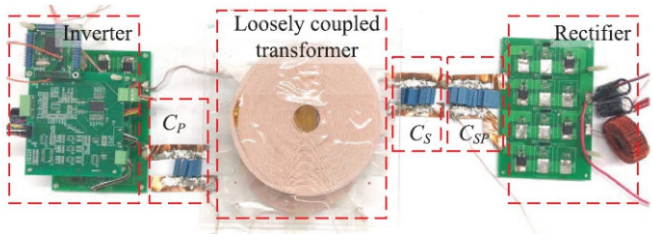


Fig. 2. Experimental Prototype of the S/SP IPT converter.

Publication(s)

[1] Z. Huang, Z. Fang, C. -S. Lam, P. -I. Mak and R. P. Martins, "Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter," IEEE Transactions on Industrial Electronics, vol. 67, no. 12, pp. 10356-10365, Dec. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Effects of Parasitic Resistances on Magnetically Coupled Impedance-Source Networks

Xiangfei Kong, Chi-Kong Wong, and Chi-Seng Lam

FEATURES

Magnetically coupled impedance-source networks

Generalized equivalent circuit model

Voltage gain under parasitic resistances

DESCRIPTION

Magnetically coupled impedance-source networks can achieve a higher voltage gain with smaller shoot-through duty ratio in comparison with the conventional impedance-source networks without coupled inductors. However, the practical voltage gain is seriously affected by the parasitic resistances in passive components and power devices, which is necessary to be investigated. This work derives and analyzes the effects of parasitic resistances on the voltage gain of magnetically coupled impedance-source networks under three different scenarios: 1) different resistance ratio between parasitic resistances and output equivalent resistance, 2) different shoot-through duty ratio and 3) different winding ratio.

First of all, a generalized equivalent circuit model considering parasitic resistances for the three typical magnetically coupled impedance-source networks – Trans-Z-source, Γ-source and Y-source networks are proposed. Based on it, the effects of parasitic resistances on the voltage gain is mathematically derived and discussed under the aforementioned three different scenarios. And the maximum voltage gain under the consideration of the three resistance ratios simultaneously is also derived. Finally, representative simulation and experimental results are provided to verify the proposed generalized equivalent circuit models, the corresponding mathematical derivations, and the effects of the parasitic resistances on the magnetically coupled impedance-source networks.

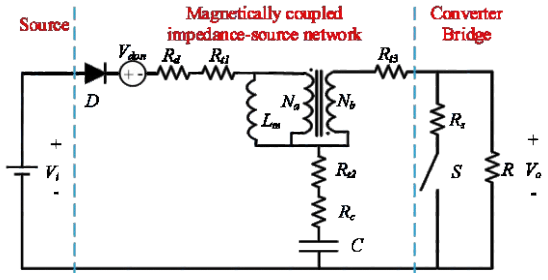


Fig. 1. Equivalent circuit model of magnetically coupled impedance-source converter under parasitic resistances condition

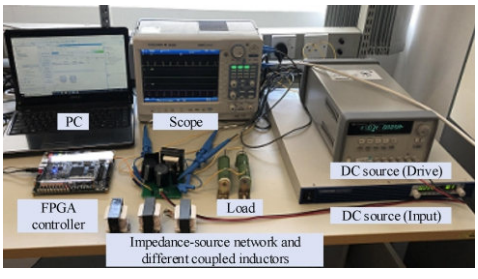


Fig. 2. Experimental prototype of the magnetically coupled impedance-source converter

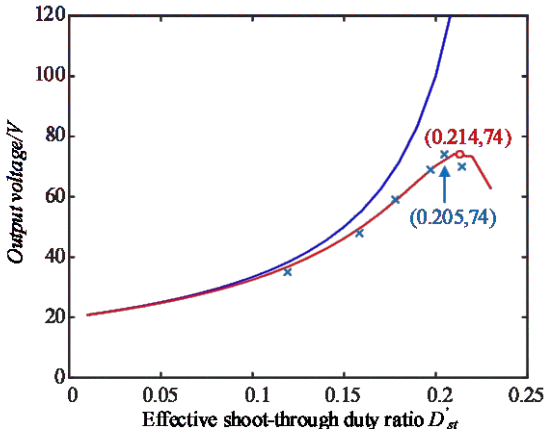


Fig. 3. Comparison of idea lossless, theoretical and experimental results of Trans-Z-source network with N_1:N_2=36:12

Publication(s)

[1] X. Kong, C.-K. Wong, Chi-Seng Lam, "Effects of Parasitic Resistances on Magnetically Coupled Impedance-Source Networks," IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9171 – 9183, Sept. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Hybrid Boost Converter With Cross-Connected Flying Capacitors

Mo Huang, Yan Lu, Tingxu Hu, and Rui P. Martins

FEATURES

Hybrid DC-DC boost converter

Good efficiency for > 4 conversion ratio

Flying capacitors soft charging

Halved output voltage ripple

Cascade bootstrap

Silicon verified in AMS 0.35-µm CMOS

DESCRIPTION

It is a hybrid DC-DC boost converter suitable for high conversion ratio (CR) applications. The performance and area are advanced in fivefold: 1) the topology halves the stress of most power switches, reducing the dynamic power loss and area; 2) the high CR is achieved with doubled pulse width of the gate control signals, allowing a higher switching frequency; 3) the inductor current ripple is reduced from the halved switching node voltage swing and increased switching frequency, then a high DCR (or small-volume) inductor can be used; 4) the flying capacitors (Cfly) are soft charged, allowing to use a small Cfly value. This significantly reduces the Cfly volume under a high voltage application. 5) the cascade bootstrap scheme reuses the bootstrap capacitor between two working phases.

Fabricated in 0.35-µm CMOS, the converter measures 93.5% power conversion efficiency (PCE) at CR = 4.5. The Cfly value is reduced to 0.47µF from soft charging. And a 3010-package inductor with 166-mΩ DCR is used. The cascade bootstrap reduces halves the large bootstrap capacitor. The active area is 0.86 mm^2.

Benchmarking with the prior art, this work succeeds in enhancing the PCE under a high CR. Additionally, it significantly reduces the volume of the inductors and Cflys. Moreover, it doubles the pulse width of the gate control signals, suitable for a high-CR application. Finally, it reduces the silicon area.

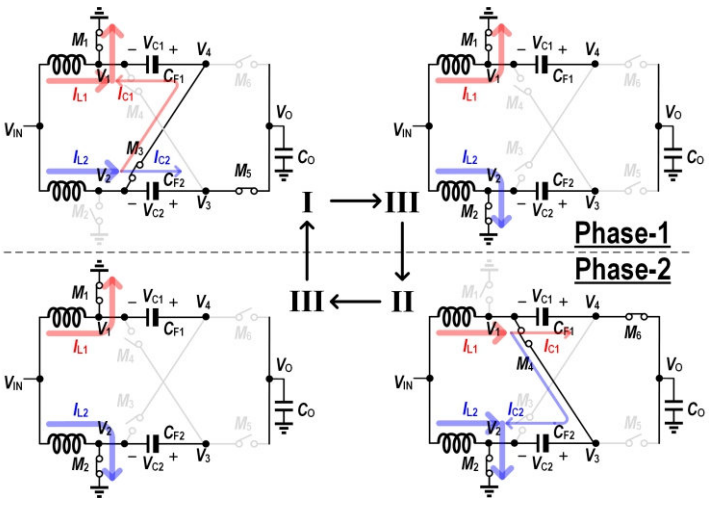


Fig. 1. Proposed convertor working principle.

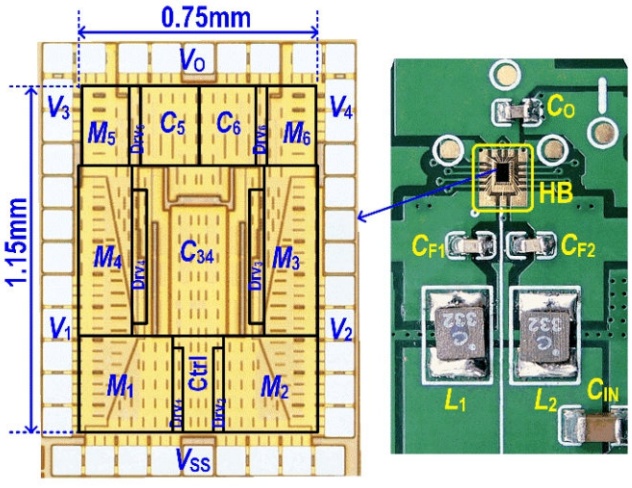


Fig. 2. Chip and PCB photos.

Publication(s)

[1] M. Huang, Y. Lu, T. Hu, and R. P. Martins, “A Hybrid Boost Converter With Cross-Connected Flying Capacitors,” IEEE Journal of Solid-State Circuits, vol. 56, no. 7, pp. 2102–2112, Jul. 2021.

[2] M. Huang, Y. Lu, and R. P. Martins, “A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5,” IEEE International Solid -State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 198–200, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Natural Science Foundation of China

An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction

Mo Huang, Yan Lu, and Rui P. Martins

FEATURES

Hybrid Low dropout regulator

Analog-proportional digital-integral control

Improved PSR up to 1MHz

Reduced output voltage ripple

Silicon verified in TSMC 65-nm CMOS

DESCRIPTION

It is a hybrid low dropout regulator (LDO) that uses analog-proportional digital-integral control. The slow, discontinuous digital-integral control provides a high DC loop gain under a low supply voltage (Vin). The analog proportional control achieves better performances in threefold: 1) it allows a fast, continuous transient response without increasing the power consumption significantly; 2) it compensates the limit cycle oscillation (LCO) from the discontinuous sampling; 3) it is the only solution to suppress the continuous power supply noise and thus improves the power supply rejection (PSR). The flip voltage follower (FVF) analog part is used, suitable for a low-Vin operation. A replica analog loop is added to further improve the PSR by 6dB. The replica loop also ensures the proportion of the output current shared by the digital control, improving the output voltage accuracy.

Fabricated in 65-nm CMOS, the LDO measures a 0.37ps FoM of speed. The 1-MHz PSR is −22dB under 0.6Vin and 0.1Vdropout. The output LCO is reduced to 3mV at a light load and almost unobservable at a heavy load. The active area is 0.04 mm².

Benchmarking with the prior art, this work succeeds in achieving a comparable high-frequency PSR under a lower supply Vin and Vdropout. Additionally, it responds fast without significantly increasing the power consumption. Finally, it reduces the silicon area.

(a)

(b)

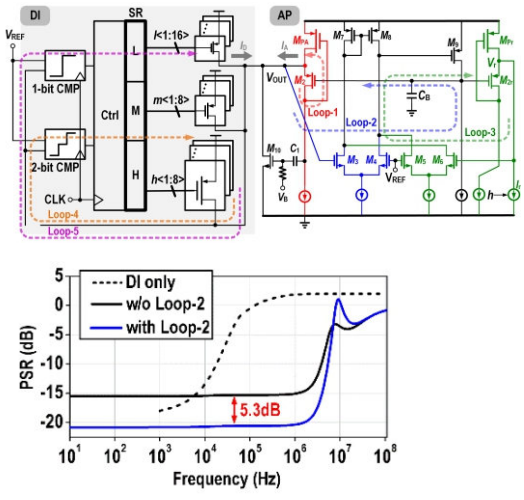


Fig. 1. (a) Schematic of the proposed LDO, and (b) PSR improvement from the replica loop.

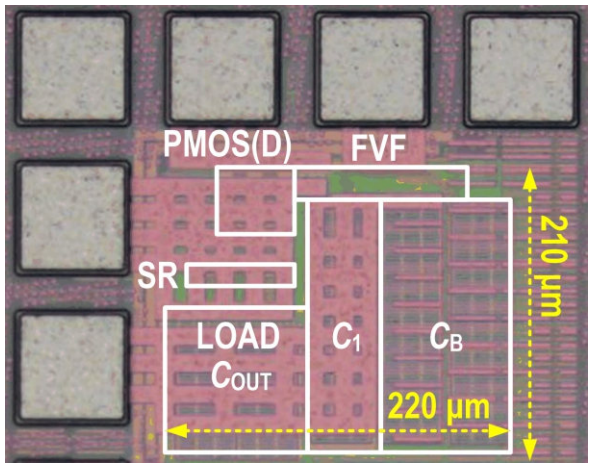


Fig. 2. Chip microphotograph.

Publication(s)

[1] M. Huang, Y. Lu, and R. P. Martins, "An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction," IEEE Journal of Solid-State Circuits, vol. 55, no. 6, pp. 1637–1650, Jun. 2020.

[2] M. Huang and Y. Lu, "An Analog-Proportional Digital-Integral Multi-Loop Digital LDO with Fast Response, Improved PSR and Zero Minimum Load Current," in 2019 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2019.

Sponsorship

Natural Science Foundation of China, Research Committee of University of Macau

An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery

U-Fat Chio, Kuo-Chih Wen, Sai-Weng Sin, Chi-Seng Lam, Yan Lu, Franco Maloberti and R.P. Martins

FEATURES

VCO-based SC 15-phase DC-DC converter

Two embedded transient-enhancement techniques (SFM & MCW)

15-phase interleaved converter

Fast transient response time/ load recovery

Silicon verified in 65 nm CMOS

DESCRIPTION

It presents a fully integrated VCO-based switched-capacitor (SC) 15-phase DC-DC converter in 65 nm CMOS. We propose two transient-enhancement techniques: Segmented Frequency Modulation (SFM) and Multiphase Co-Work control (MCW) to reduce the latency of the VCO-based control loop and shorten the SC DC-DC converter's transient response time.

The SFM can improve the heavy-to-light load transient by dynamically increasing the charge pump discharge current by 9 times, while the MCW can enhance the light-to-heavy load recovery by synchronously combining three interleaved flying capacitors together during the transient state. We designed the 15-phase interleaved converter to support an output voltage of 1 V from a 2.4 V input supply, delivering up to 138 mA of load current, which takes only 25/29 ns for output voltage recovering to the steady state from heavy-to-light/light-to-heavy load transients, respectively.

A prototype was then implemented in 65 nm CMOS. It obtains a peak efficiency of 82.8 % and keeps the efficiency above 80 % from 31 mA to the maximum load current. The SC DC-DC converter chip occupies 0.61 mm², and its output power density is 240 mW/mm². From light-to-heavy and heavy-to-light load transients, the converter can also reach a fast recovery speed of 5.1 mA/ns and 4.38 mA/ns, respectively, reflecting a state-of-the-art transient recovery performance.

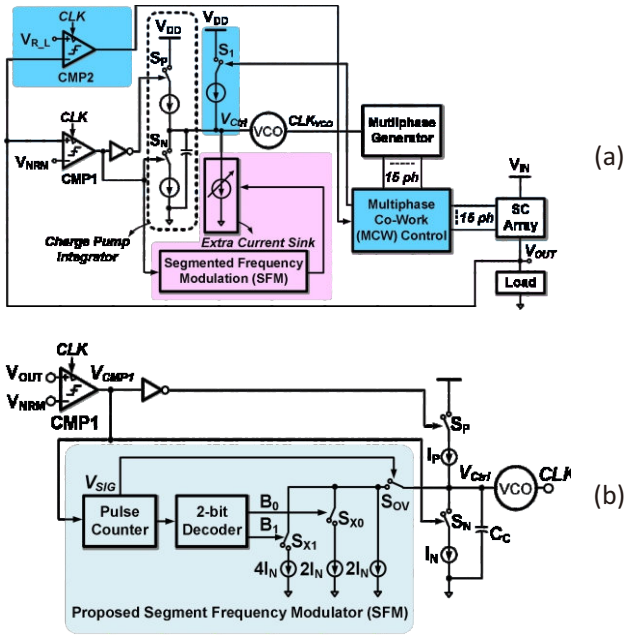


Fig. 1. Block diagram of the proposed Incremental ADC at (a) Linear-Phase and (b) Exponential-Phase.

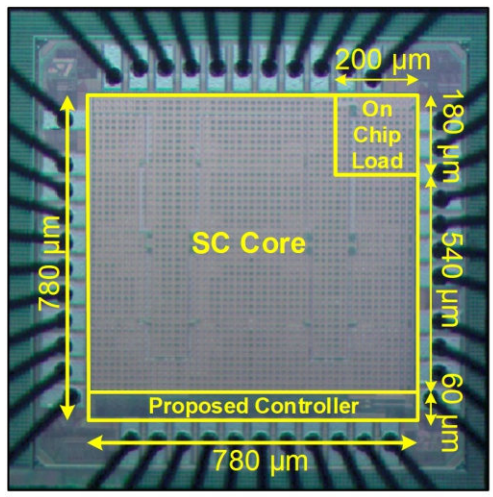


Fig. 2. Chip micrograph.

Publication(s)

[1] U.-F. Chio, K.-C. Wen, S.-W. Sin, C.-S. Lam, Y. Lu, F. Maloberti, and R. P. Martins, "An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery," 2018 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2018, pp. 31-32.

[2] U.-F. Chio, K.-C. Wen, S.-W. Sin, C.-S. Lam, Y. Lu, F. Maloberti, and R. P. Martins, "An Integrated DC–DC Converter With Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery," in IEEE Journal of Solid-State Circuits, vol. 54, no. 10, pp. 2637-2648, Oct. 2019 (Invited Special Issue of A-SSCC).

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was supported by the Research Committee of the University of Macau and Macao Science and Technology Development Fund SKL-AMSV-2017-2019 (DP), SKL/AMS-VLSI/SSW/FST and SKL/AMS-VLSI/WMC/FST under Grant 120/2016/A3.

A Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Displays

Fangyu Mao, Yan Lu, Edoardo Bonizzoni, Filippo Boera, Mo Huang, Franco Maloberti, and Rui P Martins

FEATURES

For AMOLED display driver

Single-inductor bipolar-output DC-DC

Hybrid power conversion

Floating negative output for small positive ripple

3.5W maximum output power

Silicon verified in 0.35µm CMOS

DESCRIPTION

This work is a hybrid single-inductor bipolar-output (SIBO) DC-DC converter for active-matrix organic light-emitting diode (AMOLED) displays, which are relatively more sensitive to the supply noise on the positive supply. Firstly, to improve the display quality we adopt a floating negative output configuration to migrate all the switching ripples into the negative output, achieving a near-zero voltage ripple on the positive output. Secondly, we design low-power shunt regulators, which only deal with a small portion of the output ripple, to regulate the positive output voltage further, improving the load transient response. Besides, the hybrid topology and the proposed cross-coupled bootstrap-based level-shifter, with a dual-PMOS inverter buffer, only uses standard CMOS devices without deep-N-well, reducing the chip area and cost.

The proposed converter, implemented in 0.35-µm CMOS with 5-V devices, operates at 1 MHz, leading to a measured positive output voltage ripple lower than 1 mV (all conditions). It achieves a measured 3-mV undershoot voltage and, an unnoticeable overshoot voltage on the positive output, when the output current varies between 30 mA and 350 mA. The measured peak power efficiency is 89.3% at 1.1-W output power. The maximum output power is 3.5W.

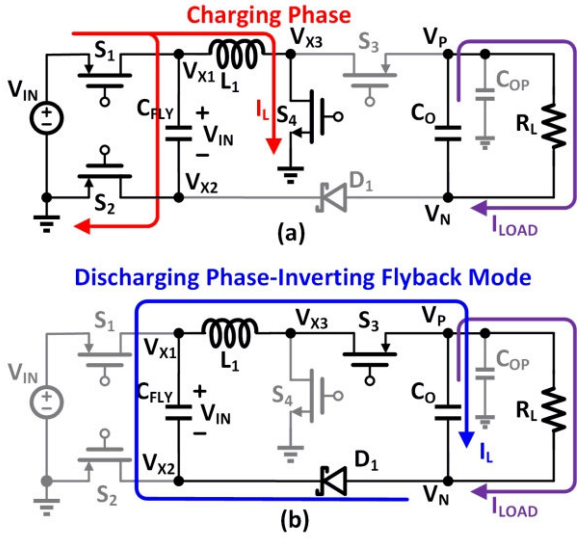


Fig. 1. (a) The charging and (b) the discharging phase of the proposed SIBO converter.

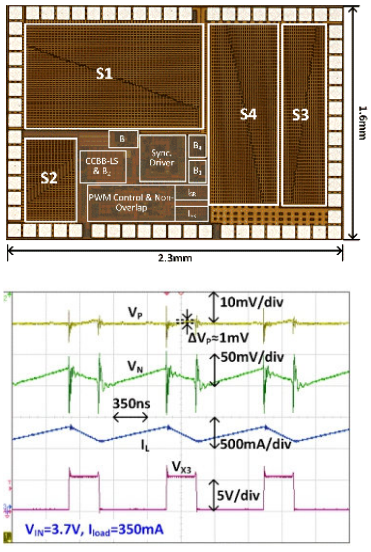


Fig. 2. Chip micrograph, and measured voltage and current waveforms.

Publication(s)

[1] F. Mao et al., "A Hybrid Single-Inductor Bipolar-Output DC-DC Converter With Floating Negative Output for AMOLED Displays," IEEE Journal of Solid-State Circuits, early access online.

[2] F. Mao et al., "A Power-Efficient Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Displays," in IEEE Custom Integrated Circuits Conference (CICC), Mar. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Single-Stage Dual-Output Regulating Rectifier with Hysteretic Current-Wave Modulation

Jie Lin, Yan Lu, Chenchang Zhan, and R. P. Martins

FEATURES

For fully wireless devices
Single-stage regulating rectifier
Dual output without additional power MOSFET
Fast response with hysteretic current-wave modulation
6.78 MHz resonant frequency
Silicon verified in 0.18µm CMOS

DESCRIPTION

This work is a 6.78-MHz single-stage dual-output regulating rectifier for miniaturizing the true-wireless devices. The proposed rectifier topology realizes AC-DC power conversion and dual-output voltage regulation simultaneously in one single stage, using only four on-chip power transistors, thereby reducing chip area and off-chip components, and improving the system power conversion efficiency. We integrate high voltage (HV) and low voltage (LV) transistors in the proposed dual-output rectifier for HV and LV output voltages, respectively. The proposed two independent three-level current-wave modulation (CWM) controllers realize voltage conversion and regulation for each output independently, with instant transient response and no cross-regulation problem.

The proposed dual-output regulating rectifier, fabricated in 0.18-µm CMOS using 1.8/3.3-V devices, can deliver a total maximum power of 1.02 W at the dual-output voltages of 1.8 V and 3.3 V. The circuit achieves a measured peak efficiency of 91.9 % with an instant load-transient response for a load current step between 20 mA and 200 mA. The cross-regulation between the dual-output voltages is unnoticeable.

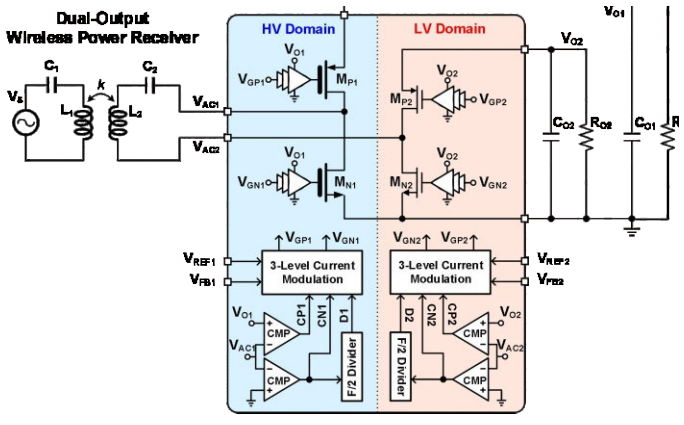


Fig. 1. A wireless power receiver with the proposed dual-output rectifier.

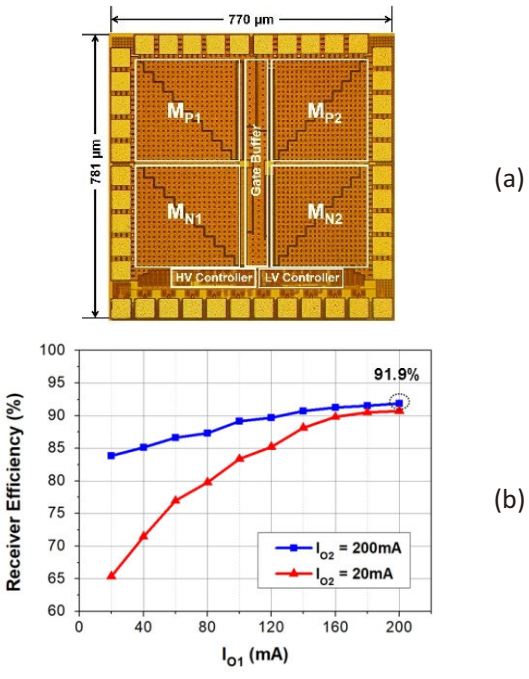


Fig. 2. (a) Chip micrograph, and (b) measured efficiency.

Publication(s)

[1] J. Lin, Y. Lu, C. Zhan, and R. P. Martins, "A Single-Stage Dual-Output Regulating Rectifier with Hysteretic Current-Wave Modulation," IEEE Journal of Solid-State Circuits, early access online.

[2] J. Lin, C. Zhan, and Y. Lu, "A 6.78-MHz Single-Stage Wireless Power Receiver with Ultra-Fast Transient Response Using Hysteretic Control and Multi-Level Current-Wave Modulation," IEEE Transactions on Power Electronics, vol. 36, no. 9, pp. 9918–9926, Sep. 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Shenzhen STI Fund.

A VHF Wide-Input Range CMOS Passive Rectifier with Active Bias Tuning

Xiaofei Li, Fangyu Mao, Yan Lu, and Rui P. Martins

FEATURES

RF wireless power transfer

Passive rectifier with active bias tuning

Average maximum efficiency of 64.4%

Silicon verified in 65nm CMOS

DESCRIPTION

Tiny implantable medical devices in mm-size demand advanced wireless power solutions that operate at hundreds of MHz, and mainly use passive rectifiers for AC-DC power conversion. A conventional cross-connected (CC) rectifier can operate with high frequency and low input voltage, but only achieves good efficiencies in a very narrow input power range, due to the shoot-through and reverse currents. This work presents a CMOS passive rectifier with active bias tuning (ABT), allowing a widely extended input range with high power conversion efficiency. In addition, we compensate the process, voltage, and temperature variations with the ABT scheme that leads to a robust design for very high frequency (VHF) operation. Meanwhile, we propose a peak V_{OUT} searching scheme to indicate the charging or discharging directions for the ABT. We obtain a bias voltage balancing among stacked rectifier stages with a switched-capacitor network.

The proposed rectifier is fabricated in a 65-nm CMOS process. Measurement results of three chips show that the proposed rectifier improves the PCE over a wide input range, with an average maximum PCE of 64.4%.

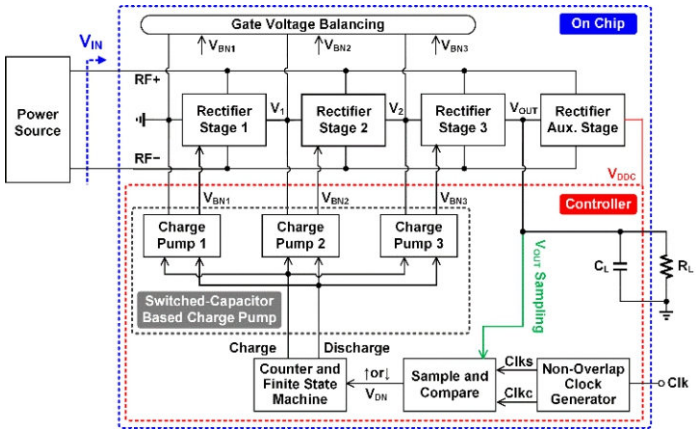


Fig. 1. System overview of the proposed rectifier with active bias tuning.

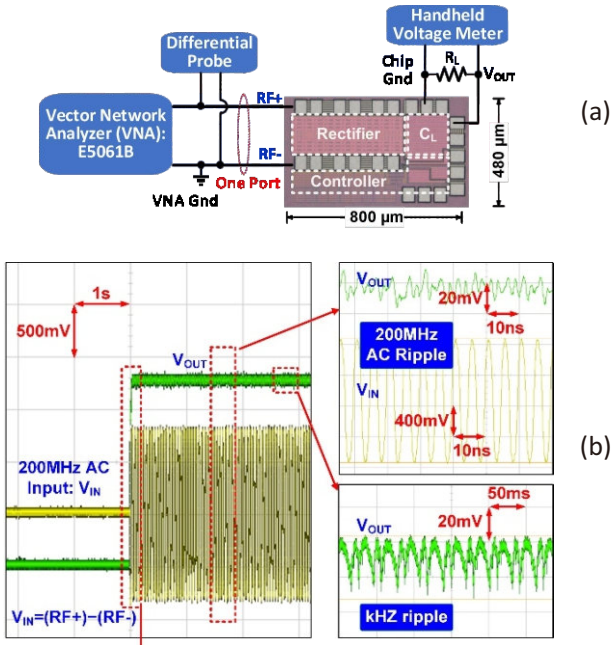


Fig. 2. Chip micrograph, and measured input and output voltage waveforms.

Publication(s)

[1] X. Li, F. Mao, Y. Lu, and R. P. Martins, "A VHF Wide-Input Range CMOS Passive Rectifier With Active Bias Tuning," IEEE Journal of Solid-State Circuits, vol. 55, no. 10, pp. 2629–2638, Oct. 2020.

[2] X. Li, F. Mao, P. Yeon, Y. Lu, M. Ghovanloo, and R. P. Martins, "A 200-MHz Wide Input Range CMOS Passive Rectifier with Active Bias Tunning," in IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2019, pp. 245–246.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

An NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28-nm CMOS

Xiaofei Ma, Yan Lu*, Qiang Li, Wing-Hung Ki, and Rui P. Martins

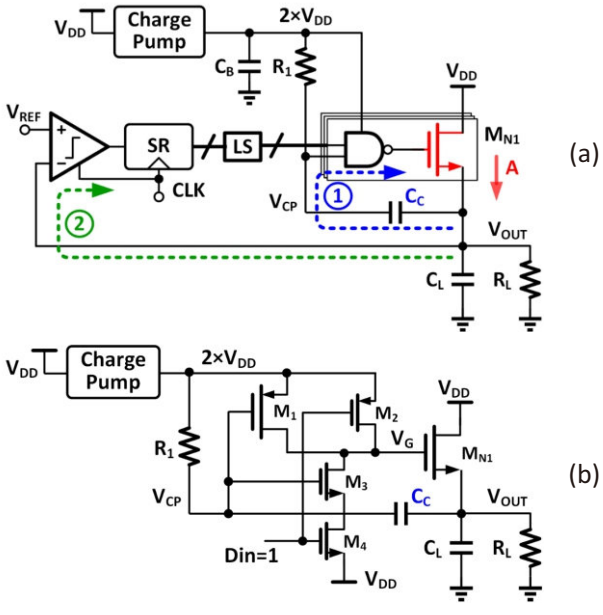
FEATURES

Analog-assisted digital control
NMOS low-dropout regulator
Output-capacitor free
<1μA quiescent current
Silicon verified in 28nm CMOS

DESCRIPTION

This work is an NMOS digital low-dropout regulator (LDO) with fast transient response and ultra-low quiescent current, to provide a tunable power supply for near-threshold voltage computing circuits in internet-of-things (IoT) devices. An LDO with an NMOS power transistor can enjoy the intrinsic fast transient response of the source-follower-like power stage, contributing to the proportional (P) part of the control loop. A shift-register-based digital control serves as an excellent candidate for the integral (I) part of the control loop. In addition, we propose a NAND-gate-based high-pass analog path (NAP) as the derivative (D) part of the loop, making the whole control scheme a complete PID control, therefore, achieving a fast transient response.

We fabricated two versions of the prototype chip, one with a 30-pF on-chip load capacitor and a fast-transient on-chip load, and the other with no load capacitor, in 28-nm CMOS. The proposed NMOS digital LDO with NAP can handle the load transient of 160 mA/ns with 810-nA quiescent current, achieving 117-mV voltage undershoot. With the proposed techniques, we can achieve nearly two orders of better FoM when comparing it to the state-of-the-art works.



(a)

(b)

Fig. 1. (a) The proposed NMOS DLDO with NAND-based high-pass analog path, and (b) the Schematic of NAP.

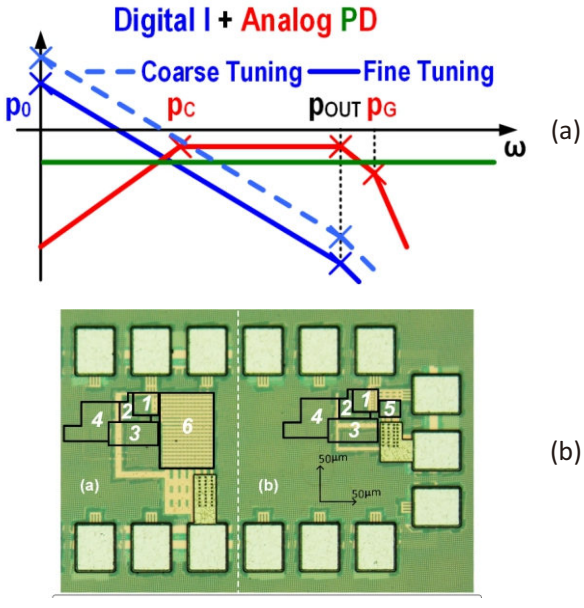


Fig. 2. The frequency responses of the loops, and the die photo of the two proposed design.

Publication(s)

[1] X. Ma, Y. Lu, Q. Li, W.-H. Ki, and R. P. Martins, "An NMOS Digital LDO With NAND-Based Analog-Assisted Loop in 28-nm CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 11, pp. 4041–4052, Nov. 2020.

[2] X. Ma, Y. Lu, R. P. Martins, and Q. Li, "A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2018, pp. 306–308.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.