RESEARCH ABSTRACTS

Energy Harvesting and Sensing Circuits

A 0.22-to-2.4V-Input Fine-Grained Fully Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Achieving 84.1% Peak Efficiency at 13.2mW/mm²

Yang Jiang, Man-Kay Law, Pui-In Mak, Rui P. Martins

FEATURES

- Systematic algorithmic voltage feed-in topology for flexible rational VCR generation
- Efficient fully integrated SC DC-DC boost conversion
- Optimal conduction and reduced parasitic loss
- Total 24 VCRs at 84.1% η_{peak} and 13.4mW/mm²
- Silicon verified in standard 180 nm CMOS

DESCRIPTION

The work proposed an algorithmic voltage-feed-in (AVFI) topology capable of systematic generation of any arbitrary buck-boost rational ratio with optimal conduction loss while achieving reduced topology level parasitic loss among the state-of-the-art works. By disengaging the existing topology-level restrictions, we develop a cell-level implementation using the extracted Dickson cell (DSC) and charge-path-folding cell (QFC) to minimize the power stage parasitic loss, exhibiting a Dickson-like switching pattern. The proposed partitionable main cell (MC) and auxiliary cell (AC) architecture achieves fined-grained voltage conversion ratio (FVCR) reconfiguration with optimal power cell utilization and reduced control complexity.

Implemented in 65nm bulk CMOS, the fully integrated switched-capacitor power converter (SCPC) using 10 MCs and 10 ACs executes a total of 24 VCRs (11 buck and 13 boost) with wide-range efficient buck-boost operations through the proposed reference-selective bootstrapping driver (RSBD). Based on the AVFI topology, the chip prototype reaches a measured peak efficiency of 84.1% at a power density of 13.4 mW/mm² over a wide range of input (0.22-to-2.4V) and output (0.85-to-1.2V).

Benchmarking with the prior art, this work achieves a significant power density improvement except from those using special processes. It also demonstrates an increased number of VCRs and a higher peak efficiency, as well as an improved power density by >13× when compared with the state-of-the-art buck-boost SCPCs.

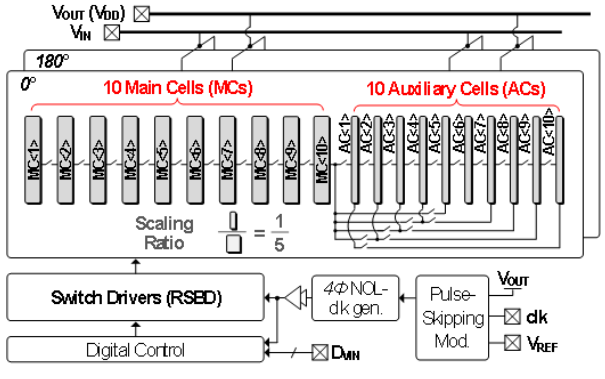

Fig. 1. System overview of the implemented ASP SC boost converter.

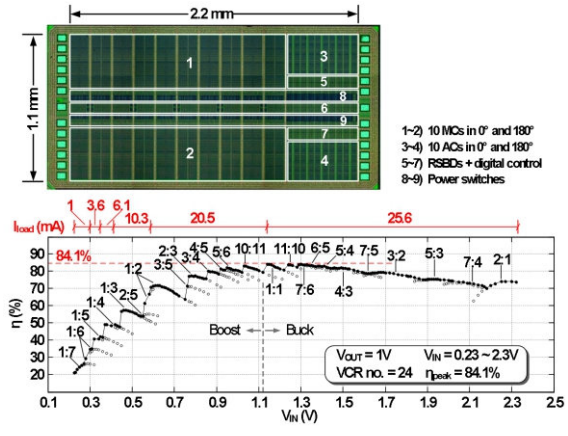

Fig. 2. Chip micrograph and measured efficiency at VOUT=1V over a wide V_{IN} range.

Publication(s)

[1] Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck-Boost Switched-Capacitor DC-DC Converters," IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3455-3469, Dec. 2018.

[2] Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "A 0.22-to-2.4V-Input Fine-Grained Fully-Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Archiving 84.1% Peak Efficiency at 13.2mW/mm²," IEEE International Solid-State Circuit Conference (ISSCC), Digest of Technical Papers, pp. 422-423, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 1.7mm² Inductor-less Fully-Integrated Capacitive-Flip Rectifier (CFR) for Piezoelectric Energy Harvesting with 483% Power Extraction Improvement

Zhiyuan Chen, Yang Jiang, Man-Kay Law, Pui-In Mak, Xiaoyang Zeng, Rui P. Martins

FEATURES

Efficient energy extraction using FCR

Fully-Integrated PEH Interface with no off-chip Inductor

7-phase operation with reconfiguration capacitor array

Wide input power adaptation

Loss optimization among phase offset, incomplete charge transfer and reduced conduction time

Silicon verified in standard 180 nm 1.8/3.3/6V CMOS

DESCRIPTION

The work presents a fully-integrated piezoelectric energy harvesting interface without external components. Instead of relying on bulky external inductors with high quality factor as in the conventional parallel-synchronized-switch harvesting-on-inductor (P-SSHI) approach, we propose a flipping-capacitor rectifier (FCR) topology to achieve voltage inversion of the piezoelectric energy harvester (PEH) through a reconfigurable capacitor array. This fundamentally preserves a fully-integrated solution without inductors while achieving a high energy extraction capability. Measurement results from FCR1 using discrete components shows an output power enhancement of up to 3.4x, which is close to the theoretical prediction.

We fabricated also a 7-phase FCR3 with 4 MIM capacitors and 21 switches using a 0.18-µm 1.8/3.3/6V CMOS process, occupying an active area of ~1.7 mm². Additionally, we implemented an active rectifier based on a common-gate comparator with phase alignment to ensure high speed operation while minimizing the diode voltage drop. A phase generate-and-combine circuit eliminates redundant switching activities.

Benchmarking with the prior art, this work reports the first PEH interface that exhibits a high MOPIR (4.83x) and high voltage flipping efficnecy (η_F) of 0.85 in a compact area with zero external components.

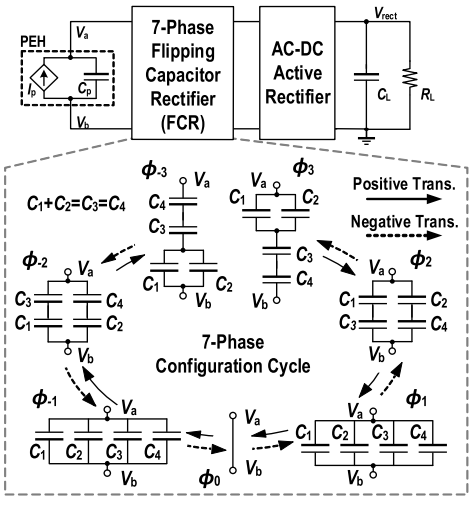

Fig. 1. System overview of the proposed 7-phase FCR piezoelectric energy harvesting interface.

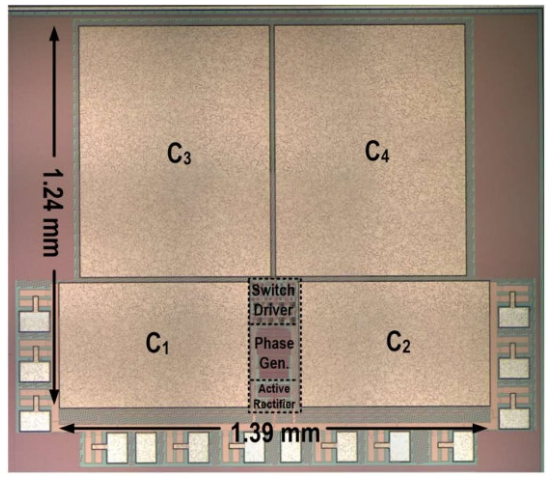

Fig. 2. Chip micrograph.

Publication(s)

[1] Z. Chen, M. K. Law, P. I. Mak, X. Zeng and R. P. Martins, "Piezoelectric Energy Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier with Capacitor-Reuse for Input Power Adaptation," IEEE Journal of Solid-State Circuits, vol. 55, no. 8, pp. 2106-2117, Aug. 2020.

[2] Z. Chen, Y. Jiang, M.-K. Law, P.-I. Mak, X. Zeng, R. P. Martins, "A Piezoelectric Energy-Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier (FCR) and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 424-425, Feb. 2019. band TIA-Based PA Driver Achieving <-157.5dBc/Hz OB Noise" IEEE ISSCC Dig. Tech. Papers, pp. 172-174, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 4µm Diameter SPAD Using Less-doped N-Well Guard Ring in Baseline 65nm CMOS

Yang Jiang, Man-Kay Law, Pui-In Mak, Rui P. Martins

FEATURES

Small size SPAD in baseline 65nm CMOS

Low dark count @73cps/µm²@20℃

High fill factor @17.7%

High peak photon detection efficiency (PDE) @9.2%

Silicon verified in baseline 65 nm CMOS

DESCRIPTION

The work proposed a small size single photon avalanche diode (SPAD) in baseline 65nm CMOS suitable for low cost time-of-flight application with high spatial resolution. The realization in advanced CMOS process offers the possibility of reducing the footprint of in-pixel electronics. By exploiting the less-doped n-well region to surround the vertical p-well/deep-nwell multiplication region, the electric field at the SPAD periphery can be reduced without process modifications while avoiding premature lateral breakdown. Based on COMSOL simulation results, the electric field in guard ring region can be ~2× lower than that at the avalanche junction. Due to the highly doped deep n-well region, the high electric field can be restricted at the vertical p-well/deep n-well interface, achieving robust SPAD operation without premature lateral breakdown at a moderate excess bias voltage (V_{EB}).

Implemented in 65nm baseline CMOS, this work shows a measured DCR of 73cps/µm²@20℃ and V_{EB}=1V. The DCR drastically increases with V_{EB} > 2.2V due to the second breakdown at the edge, indicating the maximum V_{EB} to achieve safe SPAD operation. The PDE enhances when V_{EB} increases from 1V to 2V as a result of a larger avalanche triggering probability, with a peak of 9.2% at 480nm with V_{EB} = 2V. With a laser jitter of 80ps, the full-width half maximum (FWHM) response are 343ps, 286ps, 238ps at V_{EB} = 1V, 1.5V and 2V, respectively.

Benchmarking with the prior art, this work demonstrates a compact SPAD with a small device size and a low DCR in 65nm baseline CMOS. We can achieve a ~2.8× improvement in fill factor with a comparable device active area when compared with prior arts.

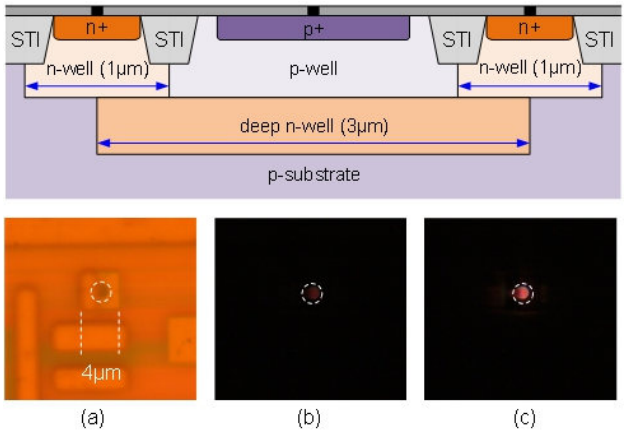

Fig. 1. Cross section of the proposed 4µm-diameter SPAD device in baseline 65nm CMOS, and (a) the chip micrograph together with the light emission test at (b) V_{EB}=1V and (c) V_{EB}=2.8V.

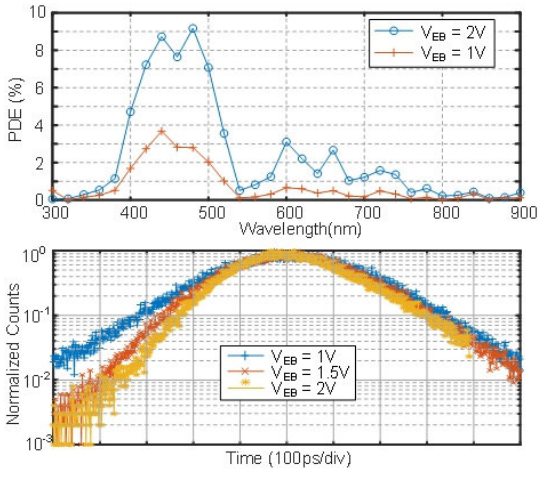

Fig. 2. Measured PDE against wavelength and timing jitter at different V_{EB}.

Publication(s)

[1] Xin Lu, Man-Kay Law, Yang Jiang, Xiaojin Zhao, Pui-In Mak and Rui P. Martins, "A 4µm Diameter SPAD Using Less-doped N-Well Guard Ring in Baseline 65nm CMOS," IEEE Transactions on Electron Devices, vol. 67, pp. 2223-2225, May 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Piezoelectric Energy-Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier (FCR) and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement

Zhiyuan Chen, Yang Jiang, Man-Kay Law, Pui-In Mak, Xiaoyang Zeng, Rui P. Martins

FEATURES

Efficient energy extraction using SPFCR

Output voltage control with MVCR SC DC-DC converter

Multi-phase operation with capacitor reuse

Wide input power adaptation

MPPT with fractional $V_{OC,FBR}$ to relax sustained voltage

Silicon verified in standard 180 nm 1.8/3.3/6V CMOS

DESCRIPTION

The work proposed split-phase flipping-capacitor rectifier (SPFCR) to strategically reconfigure capacitors into a selected set of extended and augmented phases to balance between the PEH energy extraction efficiency and implementation complexity. We can remove insignificant flipping phases through phase selection to relax the system implementation complexity without sacrificing the energy harvesting efficiency. The proposed SPFCR interface with phase selection can achieve a total of 21 flipping phases using only 4 capacitors. We also propose to reconfigure the 4 capacitors into a multiple voltage conversion ratio (MVCR) switched-capacitor DC-DC converter during the non-flipping period for improving the system input power (P_{in}) adaptation without extra passives. To avoid using the boosted SPFCR open circuit voltage ($V_{OC,SPFCR}$) for maximum power point tracking (MPPT), we further demonstrate the feasibility of using the fractional FBR open circuit voltage ($V_{OC,FBR}$) instead.

Fabricated in standard 180-nm 1.8/3.3/6V CMOS, this work demonstrates the successful 21-phase SPFCR operation with a high maximum output power improving rate (MOPIR) of 9.3× (@VD=0.12V), and up to 9× over a wide $P_{in,FBR}$ input power adaptation at V_{OUT}=2V. A pseudo-constant relationship between between $V_{mpp,SPFCR}$ and $2V_{OC,FBR}$ at different input power is also reported for MPPT operation.

Benchmarking with the prior art, this work achieves 21-phase operation using only 4 capacitors, and demonstrates a wide input power adaptation using the proposed capacitor-reuse MVCR SC DC-DC converter approach. Without using an excessively large external high Q inductor in the order of mH, this work reports a PEH interface that exhibits a high MOPIR with output voltage control and relaxed voltage tolerance requirement.

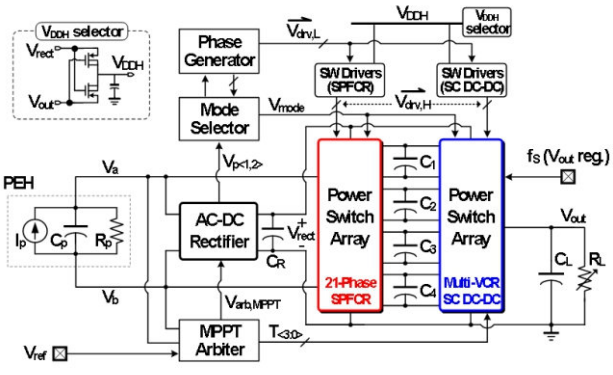

Fig. 1. System overview of the proposed SPFCR and capacitor reuse multiple-VCR SC DC-DC converter for piezoelectric energy harvesting.

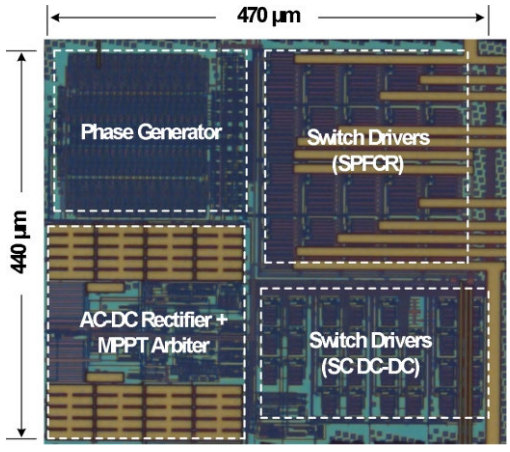

Fig. 2. Chip micrograph.

Publication(s)

[1] Z. Chen, M. K. Law, P. I. Mak, X. Zeng and R. P. Martins, "Piezoelectric Energy Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier with Capacitor-Reuse for Input Power Adaptation," IEEE Journal of Solid-State Circuits, vol. 55, no. 8, pp. 2106-2117, Aug. 2020.

[2] Z. Chen, Y. Jiang, M.-K. Law, P.-I. Mak, X. Zeng, R. P. Martins, "A Piezoelectric Energy-Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier (FCR) and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 424-425, Feb. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes for Biomedical Implant Applications

Zhiyuan Chen, Man-Kay Law, Pui-In Mak, Rui P. Martins

FEATURES

Ultra-compact single chip solution for implants

High efficiency on-chip solar energy harvesting

Parallel photodiode configurations

PDSC for startup time improvement

Systematic charge pump/solar cell area optimization

Silicon verified in standard 180 nm CMOS

DESCRIPTION

The work proposed an ultra-compact single-chip solar energy harvesting IC using on-chip solar cell for biomedical implant applications. By employing an on-chip charge pump with parallel connected photodiodes, a significant efficiency improvement can be achieved when compared with the conventional stacked photodiode approach to boost the harvested voltage while preserving a single-chip solution. A photodiode-assisted dual startup circuit (PDSC) is also proposed to improve the area efficiency and increase the system startup speed. By employing an auxiliary charge pump (AQP) using zero threshold voltage (ZVT) devices in parallel with the main charge pump, a low startup voltage of 0.25 V is obtained while minimizing the reversion loss. A 4Vin gate drive voltage is utilized to reduce the conduction loss. Systematic charge pump and solar cell area optimization is also introduced to improve the energy harvesting efficiency.

Fabricated in standard 180-nm 1.8/3.3/6V CMOS, this work occupies an active area of 1.54 mm^2. Measurement results show that the on-chip charge pump can achieve a maximum efficiency of 67%. With an incident power of 1.22 mW/cm^2 from a halogen light source, the proposed energy harvesting IC can deliver an output power of 1.65 µW at 64% charge pump efficiency.

Benchmarking with the prior art, the on-chip charge pump achieves the highest efficiency at low incident power levels (with an input voltage close to 0.3 V) which is expected in subdermal implant applications. Among existing single-chip solar energy harvesting solutions, this work demonstrates the highest energy harvesting efficiency (~3.5× improvement while generating a boosted output voltage for system use.

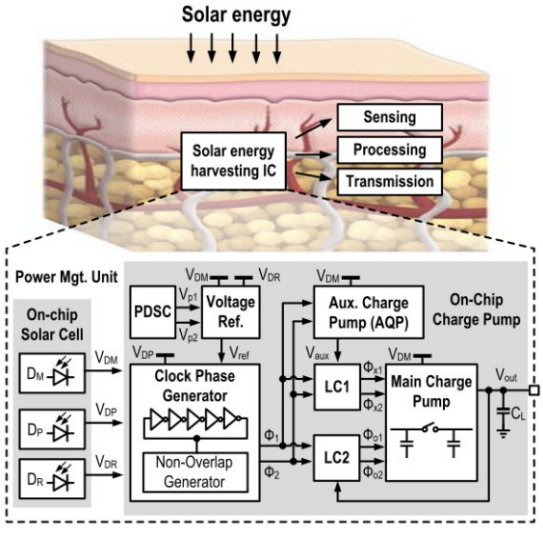

Fig. 1. System overview of the proposed single -chip solar energy harvesting IC.

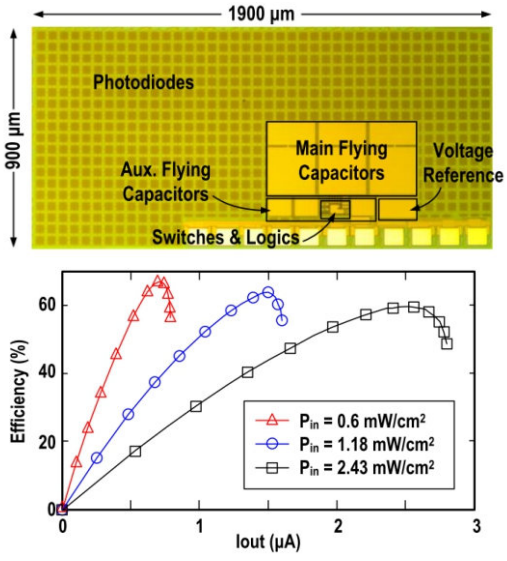

Fig. 2. Chip micrograph and measured efficiency under different incident power levels.

Publication(s)

[1] Z. Chen, M. K. Law, P. I. Mak and R. P. Martins, "A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes with a 67% Charge Pump Maximum Efficiency," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 1, pp. 44-53, Feb. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Algebraic Series-Parallel-Based Switched-Capacitor DC-DC Boost Converter with Wide Input Voltage Range and Enhanced Power Density

Yang Jiang, Man-Kay Law, Zhiyuan Chen, Pui-In Mak, Rui P. Martins

FEATURES

Systematic algebraic series-parallel topology for flexible rational VCR generation

Efficient fully integrated SC DC-DC boost conversion

Optimal conduction loss

Reduced parasitic loss

Silicon verified in standard 180 nm CMOS

DESCRIPTION

The work proposed an algebraic series-parallel (ASP) topology for fully integrated switched-capacitor (SC) DC-DC boost converters with flexible fractional voltage conversion ratios (VCRs). By elaborating the output voltage (VOUT) expression into a specific algebraic form, the proposed ASP can achieve improvements on both the charge sharing and bottom-plate-parasitic losses while maintaining the high topology and fractional VCR flexibility of conventional two-dimensional series-parallel (2DSP) converters. The proposed method consists of a generic ASP topology framework with systematic parameter determination for precise converter implementation, and can theoretically surpass the power conversion efficiency (PCE) of 2DSP converters.

Fabricated in 65nm bulk CMOS, we designed a fully integrated ASP-based SC rational boost converter by cascading with the Dickson topology, with a total of 7 rational VCRs to boost an input voltage of 0.25-to-1V to a 1V output. Delivering a maximum loading power of 20.4mW, the chip prototype achieves a peak efficiency of 80% at a power density of 22.7mW/mm².

Benchmarking with the prior art, this work with the other fully integrated SC boost converters, in both bulk CMOS and special processes. It can be observed that this work exhibits a higher power density while achieving a high number of VCR when compared with the existing designs in bulk CMOS.

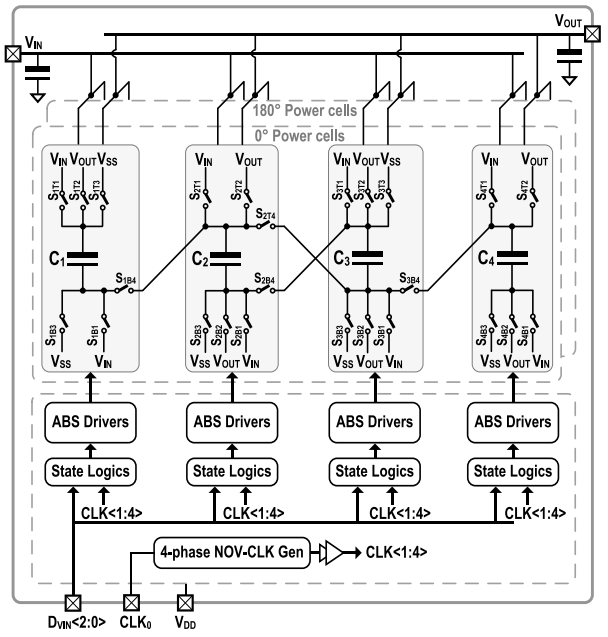

Fig. 1. System overview of the implemented ASP SC boost converter.

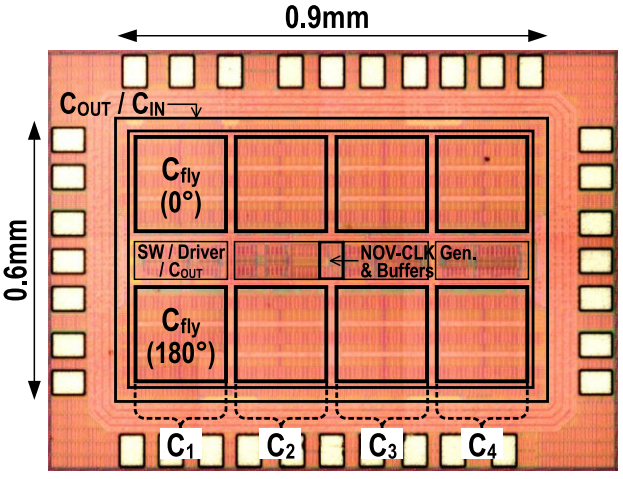

Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algebraic Series-Parallel-Based Switched-Capacitor DC-DC Boost Converter With Wide Input Voltage Range and Enhanced Power Density," IEEE Journal of Solid-State Circuits, vol. 54, no. 11, pp. 3118-3134, Nov. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau