RESEARCH ABSTRACTS

Analog and Mixed-Signal Circuits

A 0.35-V 5,200-µm² 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator

Ka-Meng Lei, Pui-In Mak, and Rui P. Martins

FEATURES

- Compact area of 5,200-µm²
- Ultra-low-voltage (0.35V) operation
- Novel asymmetric swing-boosted RC network
- Lowest energy efficiency (0.67 pJ/cycle) among the reported MHz-range relaxation oscillators

DESCRIPTION

For the crystal-less Internet-of-Things (IoT) node and wake-up receiver, low-power and fully integrated kHz-to-MHz clock sources with moderate frequency inaccuracy are pivotal to their operations. This projects develops a 2.1-MHz relaxation oscillator (RxO) for energy-harvesting Internet-of-Things (IoT) sensor nodes. The RxO features an asymmetric swing-boosted RC network and a dual-path comparator to surmount the challenges of sub-0.5-V operation while achieving temperature resilience. The former enables alternating the common-mode voltages at the output of the RC network to facilitate the sub-0.5-V operation, while the latter is outfitted with a delay generator for tracking the temperature-sensitive delay of the comparator.

Prototyped in 28-nm CMOS, the RxO occupies a tiny footprint of 5,200 µm². The power consumption is 1.4 µW at 0.35 V. The measured temperature stability is 158 ppm/°C (average of seven chips) over −20 ◦C–120 ◦C. It scores the best energy efficiency (667 fJ/cycle) among the reported MHz-range RxOs and has a figure-of-merit (181 dB) that compares favorably with the state-of-the-art, despite the ultra-low-voltage headroom and can settle within 3.6 µs after enabling the supply voltage.

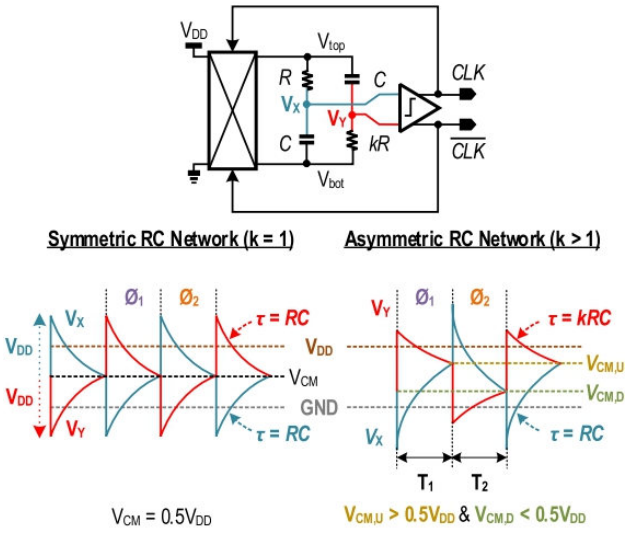

Fig. 1. Simplified schematic of the swing-boosted differential RxO and the design of k to maneuver VCM at different phases of operation.

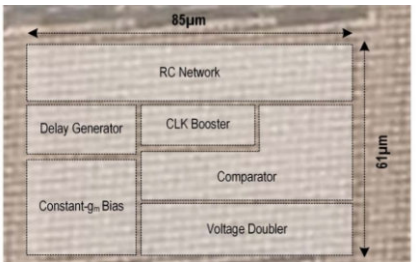

Fig. 2. Chip micrograph.

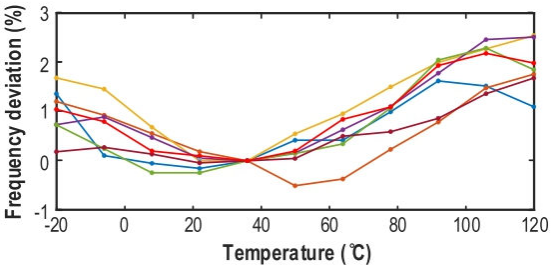

Fig. 3. Measured RxO's frequency stability versus temperature.

Publication(s)

[1] Ka-Meng Lei, Pui-In Mak, Rui P. Martins, "A 0.35-V 5,200-µm² 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator," IEEE Journal of Solid-State Circuits, Early Access, 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Regulation-Free Sub-0.5V 16/24MHz Crystal Oscillator for Energy-Harvesting BLE Radios with 14.2nJ Startup Energy and 31.8µW Steady-State Power

Ka-Meng Lei, Pui-In Mak, Man-Kay Law, and Rui P. Martins

FEATURES

Inductive multi-stage g_m for fast startup

Lowest operating voltage (0.35V) reported

Low startup energy of 14.2 nJ

Silicon verified in CMOS 65 nm process

DESCRIPTION

This project reports a regulation-free sub-0.5-V crystal oscillator (XO). The XO specifically designed for Bluetooth low-energy (BLE) radios aims for direct-powering by the harvested energy.

To secure its performance against process, voltage, and temperature (PVT) variations, while reducing its startup time and energy, we propose a dual-mode g_m scheme and a scalable self-reference chirp injection (SSCI) technique. The former employs an inductive multistage g_m to mitigate the crystal's stray capacitance during the startup, but a single-stage g_m in the steady state to preserve the phase noise (PN). For the latter (SSCI), we generate a scalable chirping sequence to kickstart the XO, avoiding trimming of the auxiliary oscillator.

The XO fabricated in 65-nm CMOS is measured with two common crystals (16/24 MHz) over a 0.3-to-0.5-V supply. At 24 MHz and 0.35 V, the startup time and energy of the XO are 400 µs and 14.2 nJ, respectively, while showing a steady-state power of 31.8 µW and a PN of −134 dBc/Hz at 1-kHz offset. The frequency stability is 14.1 ppm against temperature (−40 °C – 90 °C) and 17.9 ppm against voltage (0.3–0.5 V), both conform to the BLE standard (±50 ppm) with adequate margin.

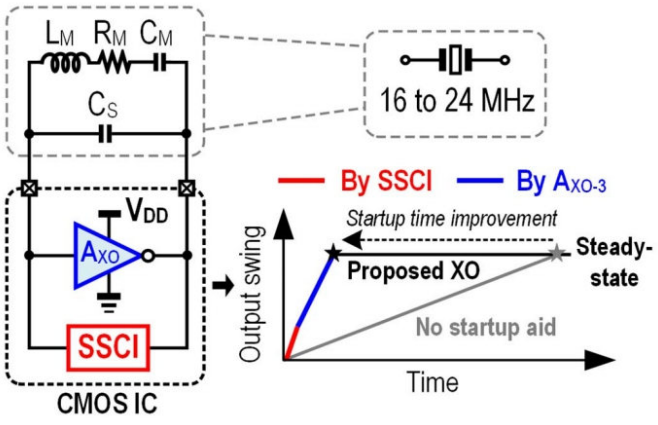

Fig. 1. Overview of the proposed XO and illustration of startup time improvement by two techniques: SSCI and inductive three-stage g_m.

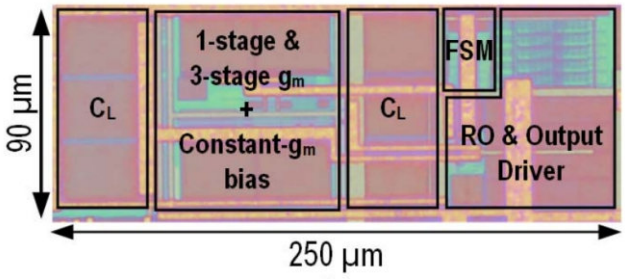

Fig. 2. Chip micrograph.

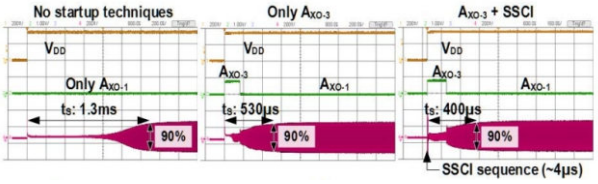

Fig. 3. Measured startup times with and without proposed techniques.

Publication(s)

[1] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A regulation-free sub-0.5-V 16-/24-MHz crystal oscillator with 14.2-nJ startup energy and 31.8-µW steady-state power," IEEE J. Solid-State Circuits, vol. 53, no. 9, pp. 2624-2635, Sept. 2018.

[2] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A regulation-free sub-0.5V 16/24MHz crystal oscillator for energy-harvesting BLE radios with 14.2nJ startup energy and 31.8µW steady-state power," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 52-53, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Startup time and energy-reduction techniques for crystal oscillators in the IoT era

Ka-Meng Lei, Pui-In Mak, and Rui P. Martins

FEATURES

Analyze startup time and energy reduction techniques for crystal oscillator

Classified into negative resistance boosting and energy injection

DESCRIPTION

Crystal oscillator (XO) is the *de facto* frequency reference of the modern wireless radios for its low power consumption, excellent phase noise (PN), and robustness against voltage and temperature variations. These essences come from the intrinsic high quality factor (Q ≈ 100,000) of the crystal. Yet, such a large Q also confines the startup time (t_s) of the XO. For example, a MHz-range XO takes a matter of milliseconds to reach the steady state. Long t_s was not a major concern for the conventional mobile devices, since the radio and XO are always on, or turned on for a long time compared with t_s. Facing the Internet-of-Things (IoT) era with massive wireless connectivity on objects, ultra-low-power (ULP) radios become crucial to extend the battery lifetime. Especially for the environmental monitoring, slow variation of ambient parameters (e.g., temperature and humidity) allows the use of duty-cycling to reduce the average power consumption. For instance, the Bluetooth Low Energy standard supports a 128-µs active mode every 1 s. During the sleep mode, the radio and XO are powered off, and long t_s can dominate the on-off latency of the radio. Also, the startup energy (E_S) of the XO limits the energy efficiency of the duty-cycled radio. As a result, recent efforts on XO for ULP IoT radios surge to improve both t_s and E_S.

In this Brief, we provide a mathematical treatment of the startup time of the crystal oscillator, and discuss the pros and cons of the recent startup time and energy-reduction techniques categorized as negative resistance boosting and energy injection.

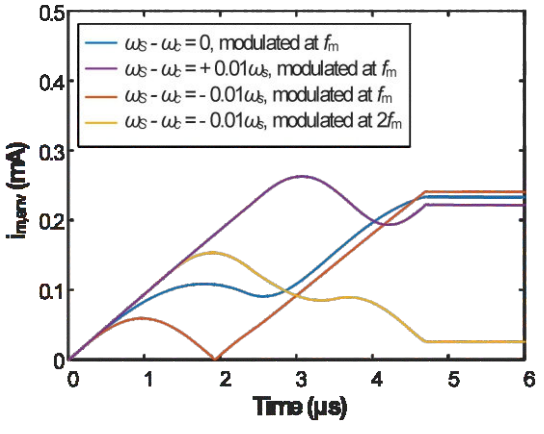

Fig. 1. The simulated $i_{M,env}$ of the 24MHz-crystal (L_M = 12 mH, C_M = 3.66 fF, R_M = 20 Ω) under different energy injection patterns and frequency mismatches (V_{INJ} = 1.2 V). The dithering signal modulated at f_m, which features a wider FWHM, guarantees a stable $i_{M,env}$ in the presence of frequency mismatch.

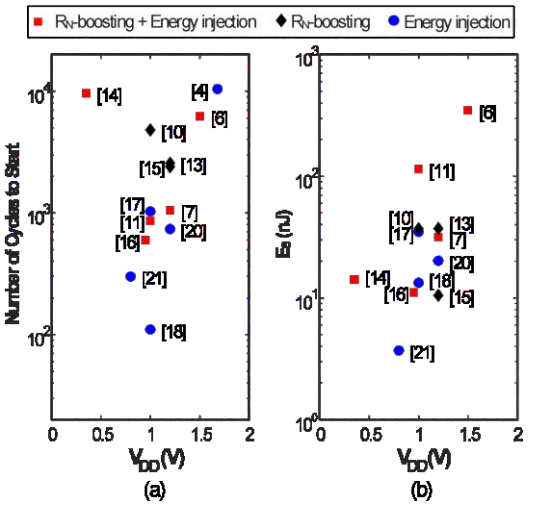

Fig. 2. Performance summary of recent XOs with t_s- and E_S-reduction techniques. (a) The number of cycles for the XO to start versus their V_{DD} (which limit the maximum V_{INJ}). (b) The E_S versus their V_{DD}.

Publication(s)

[1] Ka-Meng Lei, Pui-In Mak, Rui P. Martins, "Startup Time and Energy-Reduction Techniques for Crystal Oscillators in the IoT Era," IEEE Transactions on Circuits and Systems II, vol. 68, pp. 30-35, Jan. 2021.

Sponsorship

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A Low Jitter Ring-based PLL over PVT

Xiaofeng Yang, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Low jitter < 250fs
Ring-based PLL
Low power consumption, 4.1mW
PVT Robust
Phase Noise Cancellation
Silicon verified in 28 nm CMOS

DESCRIPTION

This paper presents a calibration-free and low-jitter phase-locked loop (PLL) with small performance degradation over PVT. We introduce an open-loop discrete-time phase noise cancellation (OPDTPNC) technique to achieve a wideband filtering and circuit inner-gain-tracking for PVT stabilization. The OPDTPNC is an effective phase realignment that enables a filtering bandwidth ~1/4 of the reference clock frequency. Besides, with the common structures and PVT tracking bias for sampler and corrector of the OPDTPNC, the prototype PLL maintains its low jitter under a wide range of PVT variations. Eventually, by cascading a Type-II PLL with the OPDTPNC, the proposed hybrid PLL attains the benefits of both Type-II PLL and injection-locked clock multiplier (ILCM). Fabricated in 28-nm CMOS with an active area of 0.023mm2 it consumes 4.1 mV from a 1 V supply with a reference spur of -63 dBc. The measured rms jitter of the 2.4 GHz PLL is 248 fs and 686 fs with and without OPDTPNC, respectively. When the temperature, supply and loop gain vary from 0 to 100℃, ±5%, and 6dB, respectively, the jitter performance only degrades less than 9%.

The proposed PLL with OPDTPNC, fabricated in 28nm CMOS, occupies an area of 0.023mm² The active area of the OPDTPNC block is 0.0016 mm2. The prototype PLL consumes a total of 4.1 mW, where the ring-VCO, PLL loop components and PNC consume 3.3 mW, 0.5 mW and 0.3 mW, respectively.

The measured phase noise of the reference clock and the 2.4 GHz output with and without the proposed PNC. We observe that the PNC circuit can suppress the phase noise significantly over a wide bandwidth. The integrated rms jitter of the PLL (10 KHz~100 MHz) is ~ 248 fs and 686 fs with and without the PNC, respectively; while the phase noise at 1 MHz frequency offset is -125.4 dBc/Hz and -109.3 dBc/Hz, respectively. The phase noise of the reference clock gets multiplied by 20·log(N), where N=16, and induces itself to the corrector's output directly without filtering. Therefore, the PN performance of the reference clock dominates the PLL clock at low and high frequency, which is similar to other PLLs based on the phase realignment scheme. There are closed-in spurs caused by the supply ripples as the RVCO is single-ended. Nevertheless, the proposed PNC also suppresses them due to the fast gain inner tracking mechanism. The measured reference spur with PNC is -63 dBc at 150 MHz offset frequency, while it is -62 dBc without PNC, both dominated by the supply cross-talk between the output buffer and reference clock buffer. We also measured the prototype PLL with different reference clock frequencies, and the integrated jitter is 234 fsrms with 156.25 MHz reference clock frequency.

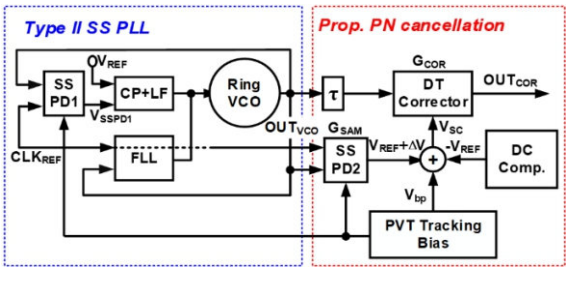

Fig. 1. Overall PLL Architecture.

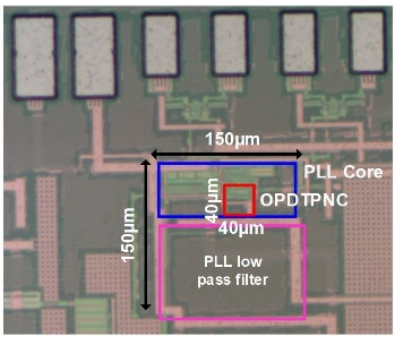

Fig. 2. Chip micrograph.

Publication(s)

[1] X. Yang, C. Chan, Y. Zhu and R. P. Martins, "A -246 dB Jitter-FoM 2.4 GHz Calibration-free Ring-Oscillator Achieving 9% Jitter Variation over PVT" in IEEE Int. Solid-State Circuits Conf. Dig. (ISSCC) Tech. Papers, pp. 260–261, Feb. 2019.

[2] X. Yang, C. -H. Chan, Y. Zhu and R. P. Martins, "A Calibration-Free Ring-Oscillator PLL With Gain Tracking Achieving 9% Jitter Variation Over PVT," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 11, pp. 3753-3763, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.