RESEARCH ABSTRACTS

Sub-GHz to GHz ADCs

A GHz Sampling Rate Multi-bit PVT Robust SAR ADC

Chi-Hang Chan, Yan Zhu, Wai-Hong Zhang, Seng-Pan U and Rui P. Martins

FEATURES

Sampling Rate > 2.4Hz
Low power consumption, 5mW
Lowe input capacitance, 64fF
Background offset calibration
Stable SNDR up to Nyquist input
Silicon verified in 28 nm CMOS

DESCRIPTION

This paper presents a 2x time-interleaved 7-bit 2.4 GS/s 1-then-2b/cycle SAR ADC in 28nm CMOS. The Process-Voltage-Temperature (PVT) sensitivity of a multi-bit SAR architecture has been improved by the proposed 1-then-2b/cycle scheme with background offset calibration. With the Pre-charge Reduction Scheme (PRS), the traditional large switching energy and time consuming pre-charge operation have been removed, which simultaneously enables a simple control logic without the need of a Vcm voltage. Besides, a background offset calibration is implemented on-chip which does not involve any which does not involve any extra phase or calibration input signal. Its operation is well embedded within the 1-then-2b/cycle architecture, thus leading to a very minimal modification of the ADC core. With an improved fringing DAC structure and a high-speed dynamic logic circuit, a single channel ADC can work at 1.2 GS/s under a 0.9V supply. Using two ways time-interleaving, the prototype samples at 2.4 GHz and consumes 5 mW power including the on-chip background offset calibration.

The ADC realized in a 28 nm 1P9M CMOS process. The active area is 0.043 mm² including the on-chip background offset calibration. The input capacitance is around 64 fF including parasitics but without considering the input routing, PAD and ESD devices. The SNDR under a wide range of temperature, supply and common-mode voltage variations with low frequency input. The chip with worst performance is #3 while it is still able to keep a SNDR above 35 dB from -40 to 125℃. When running at around 2 GS/s, the SNDR of the chip #3 stays above 38 dB in a ±10% supply and common-mode voltage variations. Comparing this work with the state-of-the-art ADCs, it achieves a good energy efficiency with the necessary calibration on-chip.

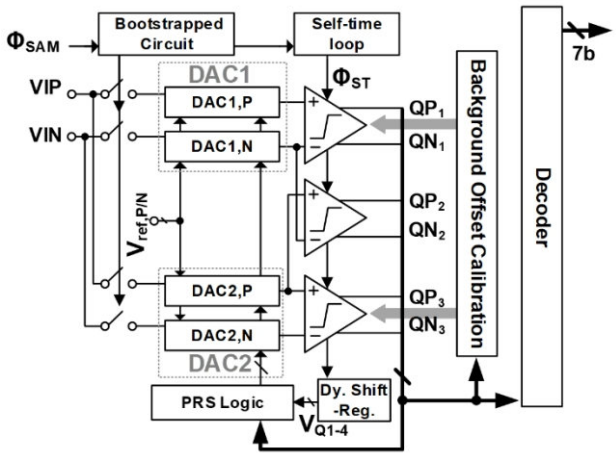

Fig. 1. Overall ADC Architecture.

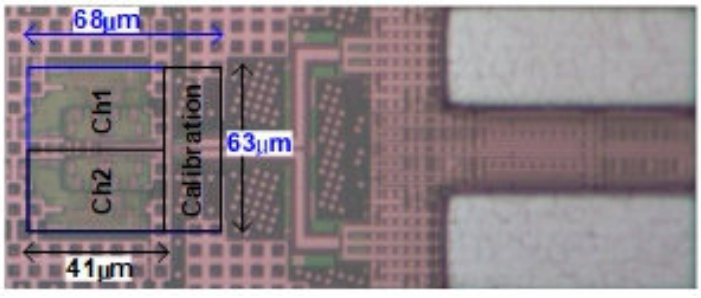

Fig. 2. Chip micrograph.

Publication(s)

[1] C. H. Chan, Y. Zhu, I. M. Ho, W. H. Zhang, S. P. U and R. P. Martins, “A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with background offset calibration, ” in International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, pp. 282-283, Feb. 2017.

[2] C. Chan, Y. Zhu, W. Zhang, S. U and R. P. Martins, "A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration," in IEEE Journal of Solid-State Circuits, vol. 53, no. 3, pp. 850-860, March 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A High-speed TDC-based ADC

Minglei Zhang, Yan Zhu, Chi-Hang Chan and Rui P. Martins

FEATURES

Sampling rate > 10GHz
TDC-ADC
Low power consumption, <50mW
On-chip calibration and low BER
Large ERBW
Silicon verified in 65 nm CMOS

DESCRIPTION

This paper presents an 8-bit time-domain analog-to-digital converter (ADC) that achieves 10 GS/s by aggregating only four time-interleaved channels. It also experiences less than 3.0-dB signal-to-noise and distortion ratio (SNDR) drop at an 18-GHz input frequency from a DC input due to its small input capacitance and inherent voltage-to-time converter (VTC)-based sub-channel buffer. A 16× time interpolation-based time-to-digital converter (TDC) resolves in two steps while allows both the inter-stage gain and the quantization step to be free from calibration over PVT variations. Furthermore, through a timing-extended residue transfer scheme, the metastability error rate is suppressed to <10-8. Fabricated in a 65-nm CMOS process, the prototype ADC achieves a 40.1-dB SNDR for a Nyquist input signal at 10 GS/s while consuming 50.8 mW from a 1.0-V power supply, yielding a Walden figure-of-merit of 61.5 fJ/conversion-step.

The prototype 8-bit 10-GS/s time-domain ADC was fabricated in a 1P9M 65-nm CMOS process. The chip die micrograph with an active area of 0.095 mm2. The chip die is bonded on a printed circuit board with <0.5-mm critical bonding wires. High-speed ADC measurement strategy with input amplitude and phase monitor is adopted in this work. The ADC has a power supply of 1.0 V with separated supply domains for different blocks and a large decoupling capacitance to reduce the crosstalk among supplies. For the most critical situation where all blocks share the same supply trace with 1-nH bonding wire and 200-pF decoupling capacitance, simulation results show that the ADC SNDRs reduces from 52.3 dB to 48.9 dB and 45.6 dB at the LF and Nyquist inputs, respectively, excluding the noise and random quantization mismatch. One-time foreground calibration is applied to remove the offset of VTCs for better dynamic range performance. The gain, remaining offset, and time skew between different channels are removed in the background together with the residue transfer offset, while the calibration is enabled occasionally to track the slow drift of the ambient temperature and supply voltage. No calibration related to the time quantization steps and inter-stage gain is applied, benefiting from the 16× interpolation-based two-stage architecture.

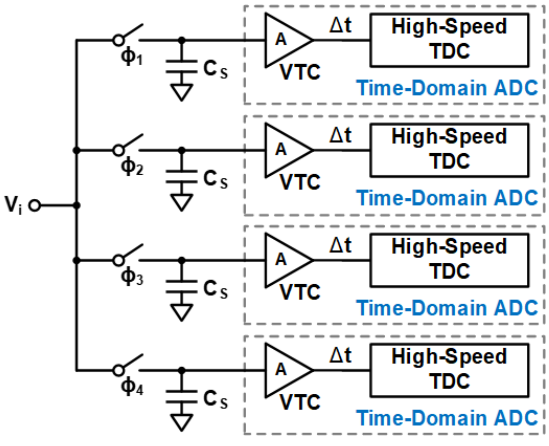

Fig. 1. Overall ADC Architecture and timing

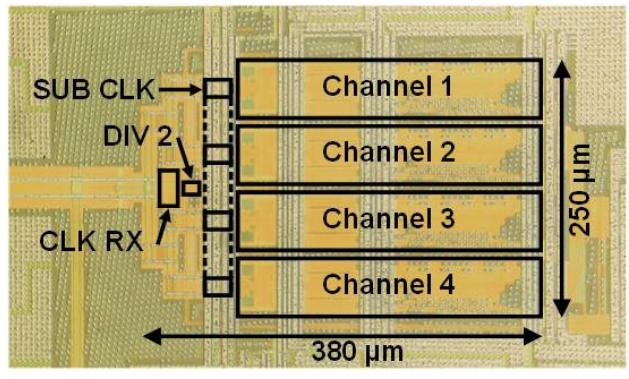

Fig. 2. Chip micrograph.

Publication(s)

[1] M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 4× interleaved 10GS/s 8b time-domain ADC with 16× interpolation-based inter-stage gain achieving >37.5dB SNDR at 18GHz input," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2020, pp. 252-253.

[2] M. Zhang, Y. Zhu, C. H. Chan, and R. P. Martins, "An 8-bit 10-GS/s 16× interpolation-based time-domain ADC with <1.5-ps uncalibrated quantization steps," IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3225-3235, Dec. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Single Channel GHz Sampling Rate Fully Dynamic Pipeline ADC

Zihao Zheng, Lai Wei, Jorge Lagos, Ewout Martens, Yan Zhu, Chi-Hang Chan, Jan Craninckx and Rui P. Martins

FEATURES

Sampling Rate > 3.3GHz
Single Channel Fastest Pipeline
Low power consumption, 5.5mW
On-chip calibrations
Fully dynamic power
Silicon verified in 28 nm CMOS

DESCRIPTION

This paper presents a single-channel 3.3 GS/s 6b pipelined ADC which features a post-amplification residue generation (PARG) scheme, linearized dynamic amplifier and on-chip calibration to achieve a high-speed, low-power, and compact prototype. The PARG scheme allows the quantization and amplification to run in parallel for a fast pipelining operation. The 6b ADC consists of 6 pipelined stages with 6 comparators and 5 amplifiers in total. Such small number of hardware reduces the overhead from the calibration and enables fully on-chip implementation. By further sharing the calibration hardware between the offset and gain calibration, the ADC with on-chip calibration only occupies 0.0166 mm² in 28 nm CMOS. With a linearized dynamic amplifier for the residue amplification, the ADC achieves 34 dB SNDR with a Nyquist input with 3.3 GS/s, consuming 5.5 mW and yielding a 40.02 fJ/conversion-step Walden FoM.

The ADC is fabricated in 28 nm CMOS, with ~40 fF input capacitance (excluding ESD) and occupies an active area of 0.0166 mm² (132 µm x 126 µm), including on-chip calibration. The input swing of the prototype is 400mVpp-diff to adopt the PARG scheme. During measurements, the on-chip calibration is performed at the foreground and the calibration counter values are frozen throughout all conditions. The measured output spectrum (decimated by 225) at 3.3 GS/s for an input near Nyquist (1.649 GHz), with and without calibration. Before the calibration, the 2nd and 3rd harmonic dominate the SFDR and greatly limit the achievable SNDR. The mismatches between differential circuits cause mainly the second harmonic, while the offset and gain error results in the third harmonic. These harmonics are reduced once the calibration is done, and the SFDR is improved by 5 dB. The measured DNL and INL before calibration are +1.48 / -1 LSB and +1.08 / -1.68 LSB, and after calibration are +1.08 / -0.85 LSB and +1.11 / -1.044 LSB respectively.

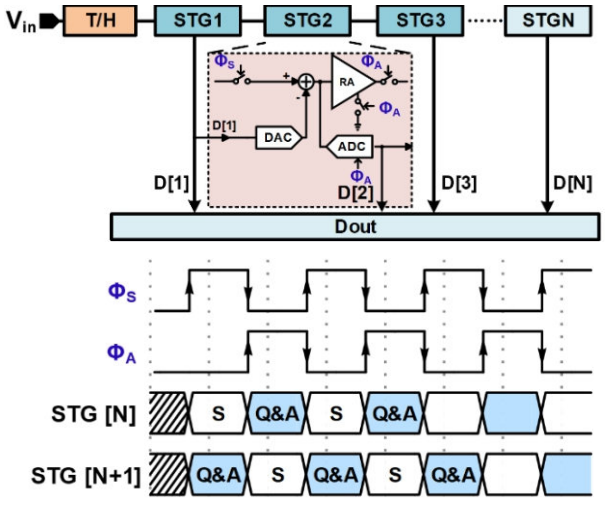

Fig. 1. Overall ADC Architecture and timing.

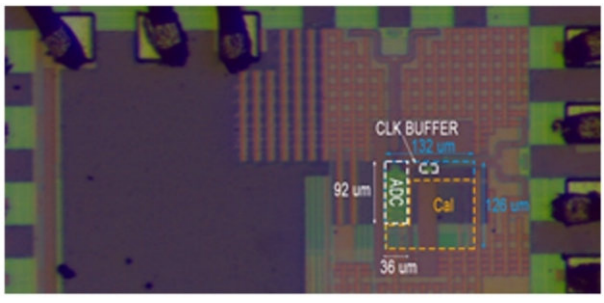

Fig. 2. Chip micrograph.

Publication(s)

[1] Z. Zheng et al., "16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 254-256.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 1.6GS/s 12.2mW 7/8-way Split Time-Interleaved SAR ADC achieving 54.2-dB SNDR with Digital Background Timing Mismatch Calibration

Mingqiang Guo, Jiaji Mao, Sai-Weng Sin, Hegong Wei, and Rui P. Martins

FEATURES

Novel Architecture: Split Time-Interleaved ADC

Relative prime Number Channels: 7/8 Way

Digital Background Timing Mismatch Calibration

High-speed: 1.6GS/s Sampling Rate

Wide-band:2.5-GHz effective resolution bandwidth

Low power consumption, 12.2 mW

Silicon verified in 28 nm CMOS

DESCRIPTION

It presents a split time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with digital background timing-skew mismatch calibration. It divides a TI-SAR ADC into two split parts with the same overall sampling rate but different numbers of TI channels. Benefitting from the proposed split TI topology, the timing skew calibration convergence speed is fast without any extra analog circuits. The input impedance of the overall TI-ADC remains unchanged, which is essential for the preceding driving stage in a high-speed application.

We designed a prototype 7/8-way split TI-ADC implemented in 28nm CMOS. After a digital background timing skew calibration, it reaches a 54.2 dB SNDR and 67.1 dB SFDR with a near Nyquist rate input signal and a 2.5GHz effective resolution bandwidth (ERBW). Furthermore, the power consumption of ADC core (mismatch calibration off-chip) is 12.2mW running at 1.6GS/s, leading to a Walden FOM of 18.2fJ/conv.-step and a Schreier FOM of 162.4dB, respectively.

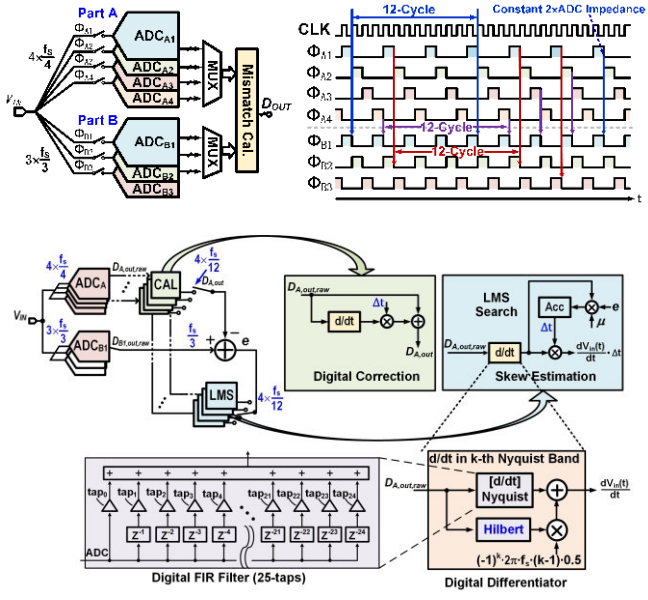

Fig. 1. The architecture and timing skew mismatch calibration of a 3/4-way split TI ADC

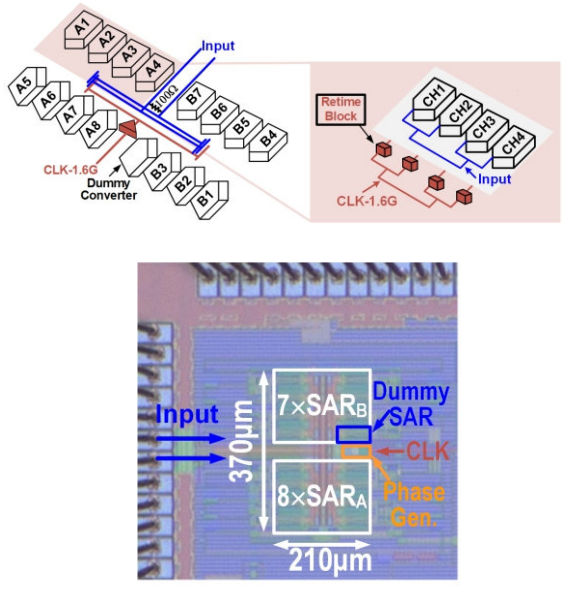

Fig. 2. Block diagram and chip micrograph of 7/8-way split TI ADC.

Publication(s)

[1] M. Guo, J. Mao, S. -W. Sin, H. Wei and R. P. Martins, "A 10b 1.6GS/s 12.2mW 7/8-way Split Time-interleaved SAR ADC with Digital Background Mismatch Calibration," 2019 IEEE Custom Integrated Circuits Conference (CICC), 2019, pp. 1-4.

[2] M. Guo, J. Mao, S. Sin, H. Wei and R. P. Martins, "A 1.6-GS/s 12.2-mW Seven-/Eight-Way Split Time-Interleaved SAR ADC Achieving 54.2-dB SNDR With Digital Background Timing Mismatch Calibration," IEEE Journal of Solid-State Circuits, vol. 55, no. 3, pp. 693-705, March 2020 (Invited Special Issue of CICC).

Sponsorship

Macau Science & Technology Fund (Ref: SKL-AMSV-2017-2019(DP)), Research Grants of University of Macau (Ref: MYRG2018-00204-AMSV).

A 5 GS/s 29 mW Interleaved SAR ADC Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications

Mingqiang Guo, Jiaji Mao, Sai-Weng Sin, Hegong Wei, and Rui P. Martins

FEATURES

Fully Digital Background Timing Mismatch Calibration

High-speed: 5GS/s Sampling Rate

Wide-band:4-GHz effective resolution bandwidth

Low power consumption, 29 mW

Silicon verified in 28 nm CMOS

DESCRIPTION

It presents a 16-channel 5 GS/s time-interleaved (TI) SAR ADC for a direct-sampling receiver that employs a digital-mixing background timing mismatch calibration to compensate for timing-skew errors. It uses a first-order approximation to obtain the derivative of the autocorrelation of the input signal, subsequently used to evaluate the explicit amount of the timing-skew. Therefore, this allows a digital background calibration of the timing-skew, avoiding extra analog circuits. The proposed 16-channel TI ADC uses a splitting-combined monotonic DAC switching method for the individual SAR channel to achieve a trade-off of simple switching and small common-mode voltage variation of the comparator.

The prototype is implemented in a 28 nm CMOS, reaches a 48.5/47.8 dB SNDR with an input signal of 2.38/4.0 GHz after the proposed background timing mismatch calibration, respectively. Furthermore, the ADC core's power consumption is 29 mW sampling at 5 GS/s, with a Walden FoM of 26.7 fJ/conv.-step and a Schreier FoM of 157.9 dB.

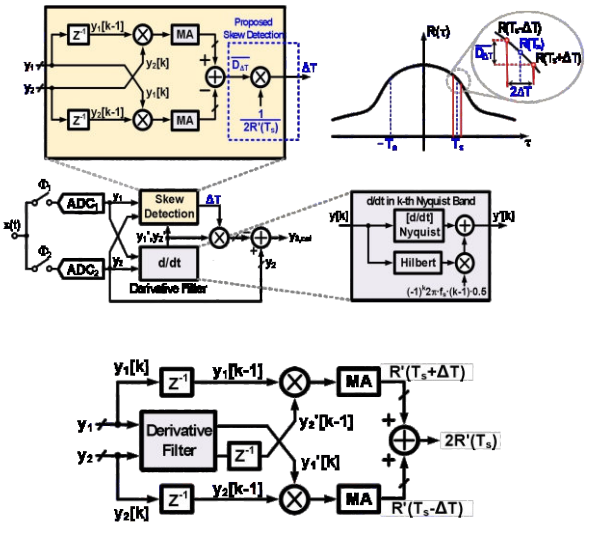

Fig. 1. Proposed fully digital timing mismatch topology based on digital-mixing.

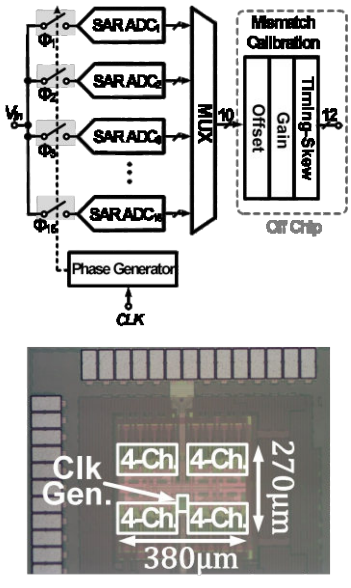

Fig. 2. Block diagram and chip micrograph f 16-way TI ADC.

Publication(s)

[1] M. Guo, J. Mao, S. -W. Sin, H. Wei and R. P. Martins, "A 29mW 5GS/s Time-interleaved SAR ADC achieving 48.5dB SNDR With Fully-Digital Timing-Skew Calibration Based on Digital-Mixing," 2019 Symposium on VLSI Circuits, 2019, pp. C76-C77.

[2] M. Guo, J. Mao, S. -W. Sin, H. Wei and R. P. Martins, "A 5 GS/s 29 mW Interleaved SAR ADC With 48.5 dB SNDR Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications," IEEE Access, vol. 8, pp. 138944-138954, 2020.

Sponsorship

National Key R&D Program of China (File no. 2019YFB1310000), Macau Science and Technology Development Fund (FDCT, File no. SKL-AMSV(UM)-2020-2022), Research Committee of University of Macau (File no. MYRG2017-00192 -FST & MYRG2018-00204-AMSV).

A 3-stage GHz Sampling Rate Fully Dynamic Pipeline ADC

Wenning Jiang, Yan Zhu, Minglei Zhang, Chi-Hang Chan and Rui P. Martins

FEATURES

Sampling Rate > 1GHz
Single Channel Pipeline-SAR
Low power consumption, 7.6mW
VT Robust
Linearized fully-settled dynamic amplifier
Silicon verified in 28 nm CMOS

DESCRIPTION

A temperature-stabilized 12-bit single-channel SAR-assisted pipelined ADC running at 1 GS/s with Nyquist SNDR above 60 dB is presented. The ADC employs a 3-stage (4b-4b-6b) SAR-assisted pipeline hybrid architecture to achieve an attractive energy efficiency along with an extended sampling rate. A high-linearity open-loop Gm-R-based residue amplifier (RA) with both complete-settled and dynamic features improves the residue amplification efficiency and speed, while reducing the gain variation over a temperature drift. The inter-stage gain variation over the temperature is compensated through complementary temperature coefficients from the inner devices of the RA. Furthermore, a cascade amplification topology in the backend RA alleviates the effect of the input parasitic capacitance to its front-end capacitor DAC (CDAC), thus leading to a small CDAC size to accelerate amplification and conversion. The prototype ADC was fabricated in a 28-nm CMOS process and consumes 7.6 mW from a 1 V power supply at 1 GS/s.

The prototype ADC was fabricated in a 28-nm CMOS process, occupying a core area of 0.0091 mm². The ADC powered by a 1 V supply exhibits a 1.2 Vpp-diff full scale range. Due to the unskilled layout, the L-DAC suffers from some mismatch and a bit weight calibration is adopted in the measurement. The first 4b codes are corrected with integer bit weight one-time, and the bit weight array is fixed to different samples. Besides, the one-time calibration to the comparators offset (histogram-based detection in the measurement), RAs gain is done in the foreground. The measured DNL and INL are +0.47/-0.39 LSB and +1.87/-2.21 LSB, respectively. For a low input frequency of 140.63 MHz, the measured SNDR and SFDR are 61.4 dB and 74.6 dB, respectively, and the noise performance (SNR) is limited by the input buffer. For the near Nyquist input frequency of 495.19 MHz, the measured SNDR keeps 60 dB and the SFDR keeps 74.6 dB. The ADC achieves above 9b ENOB even with the input frequency raised up to 1.2 GHz, and the estimated clock jitter (~200 fs) degrades the dynamic performance when the input signal exceeds 1 GHz. The ADC keeps around 59 dB SNDR under 1.1 GS/s.

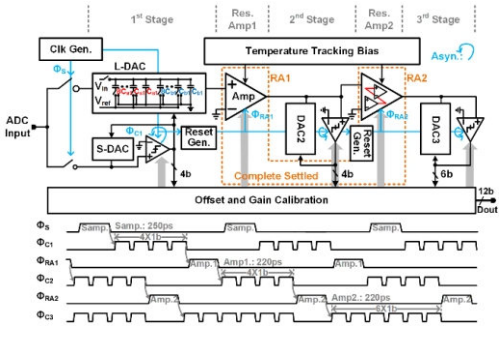

Fig. 1. Overall ADC Architecture and timing.

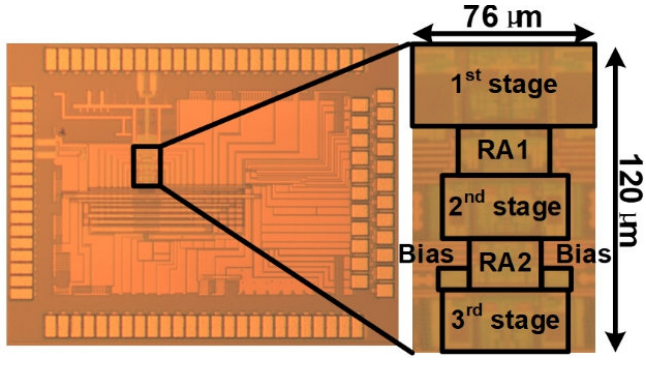

Fig. 2. Chip micrograph.

Publication(s)

[1] W. Jiang, Y. Zhu, M. Zhang, C. Chan and R. P. Martins, "3.2 A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 60-62, Feb. 2019.

[2] W. Jiang, Y. Zhu, M. Zhang, C. Chan and R. P. Martins, "A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier," in IEEE Journal of Solid-State Circuits, vol. 55, no. 2, pp. 322-332, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.