RESEARCH ABSTRACTS

High Speed ADCs

A Wideband Continuous-time Sigma Delta Modulator

Wei Wang, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Bandwidth > 100MHz

Continuous-time sigma delta modulator

Low power consumption, 16.3mW

Preliminary sample and quantization technique

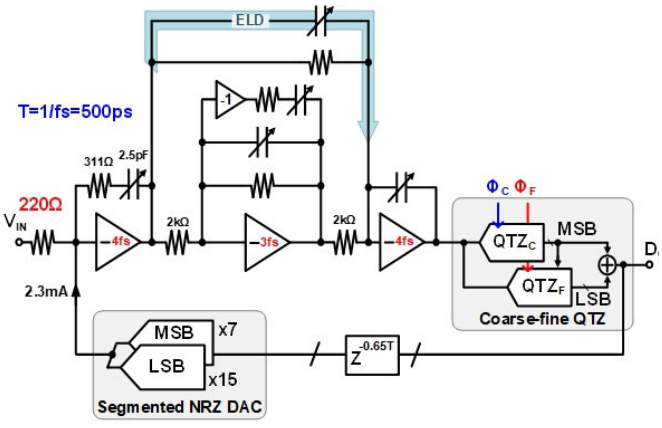
SAR ADC as quantizer

Silicon verified in 28 nm CMOS

DESCRIPTION

This paper reports a 4th-order 100 MHz bandwidth continuous-time (CT) delta-sigma modulator in 28 nm CMOS. A preliminary sampling and quantization (PSQ) technique is presented, which allows almost a full utilization of the clock period for the quantization to extend the available conversion time of the backend quantizer under a 0.65 ELD coefficient. With the PSQ, both the sampling and quantization of the backend quantizer are split into 2-step, coarse and fine, similar to the subranging architecture to save power. The quantizer runs at 2 GHz achieving 7-bit (1b error correction) with only 1.4 mW power. By adding a feedforward ELD compensation path in the cascade of integrators of the CIFF topology, only one DAC is necessary in this design. The modulator attains a signal bandwidth of 100 MHz with 72.6 dB SNDR while only consuming 16.3 mW from 1.1 V and 1.5 V power supplies. The prototype has a dynamic range of 76.3 dB and a Schreier FoM of 174.2 dB with an active area of 0.019 mm^2.

The CT ΔΣ modulator is realized in 28 nm CMOS has an active area of 0.19 mm^2. The power supply of the QTZ is 1.1V and the NRZ DAC is with 1.5V supply for the low noise considerations. The other parts are working under a 1V supply. The sampling frequency of the modulator is 2 GHz with 10 OSR. The 0.65Ts ELD and 0.25Ts are realized by inverters' delay which vary under PVT. In this design, we make only the fine sampling instant tunable for the best speed performance. The bandwidth is 100MHz. The output spectrum of the modulator with a -2 dBFS, 1.4Vpp single-tone signal at ~18 MHz input frequency. The SNDR, SNR and spurious-free dynamic range (SFDR) are 72.6 dB, 73.2 dB and 83.6 dB, respectively after the DAC mismatch calibration. The 80 dB/decade spectral slope validates the 4th-order noise shaping realized by the SAB and two conventional integrators.



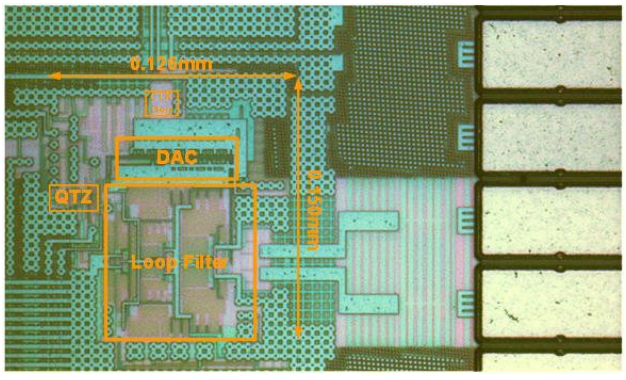


Fig. 2. Chip micrograph.

Publication(s)

[1] W. Wang, C. Chan, Y. Zhu and R. P. Martins, "20.7 A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM with Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 340-342.

[2] W. Wang, C. Chan, Y. Zhu and R. P. Martins, "A 100-MHz BW 72.6-dB-SNDR CT ΔΣ Modulator Utilizing Preliminary Sampling and Quantization," in IEEE Journal of Solid-State Circuits, vol. 55, no. 6, pp. 1588-1598, June 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT),Research Committee of University of Macau.

A Wideband Dynamic Amplifier Reused NS Pipeline-SAR ADC

Yan Song, Yan Zhu, Chi-Hang Chan and Rui P. Martins

FEATURES

Bandwidth > 40MHz

Noise-Shaping Pipeline-SAR

Low power consumption, 2.56mW

Flip around error feedback Noise-shaping

Dynamic amplifier reused

Silicon verified in 28 nm CMOS

DESCRIPTION

This article presents a successive approximation register (SAR)-assisted noise-shaping (NS) pipeline analog-to-digital converter (ADC) incorporating various techniques to improve its bandwidth (BW), energy efficiency as well as robustness. A multiple-input dynamic amplifier is utilized for both residue amplification and error feedback (EF) summation, thus realizing a 1st-order NS with low power consumption. An additional residue feed-forward (FF) path is introduced in the 2nd stage SAR ADC to compensate for the NTF deterioration caused by the gain mismatch in the multiple-input pairs of the dynamic amplifier. The partial interleaving 1st stage breaks the speed bottleneck of conventional 3-phase timing arrangement, which significantly enhances the overall ADC's speed and sampling performance. Besides, a coarse SAR ADC is introduced to further speed up the conversion with low power, while simultaneously enabling the enclosure of the data-weighted-averaging (DWA) on the DAC without a speed penalty. Finally, a low-cost inter-stage offset calibration is proposed that aligns the offset voltages among stages in the background without requiring an extra phase.

The ADC prototype fabricated in 28-nm CMOS process occupies an active area of 0.016mm^2.The pseudo-random noise generator, DWA, and inter-stage offset calibration logic account for only 1%, 1.3%, 1% of the total ADC's area, respectively. The ADC operates at the sampling rate of 600 MHz and achieves a BW up to 40 MHz at an OSR = 7.5. The measured FFT spectrum when the DWA is disabled. The actual pole of the NTF in this sample is estimated to be 0.6, which is affected by the mismatch variations, as discussed in Section III B. Under such condition, the FF NS path can still contribute an extra 4-dB SQNR which compensates the NTF deterioration originated from the α variation. The measured 32768-point FFT spectrum with a 2 MHz, -0.4 dBFS sinusoidal input signal at different calibration configurations. With all calibrations enabled, the prototype reaches a peak SNDR and spurious-free-dynamic-range (SFDR) of 75.2 dB and 87.1 dB, respectively. The residual DAC mismatches and the non-linearity from the dynamic amplifier impose the remaining harmonics.

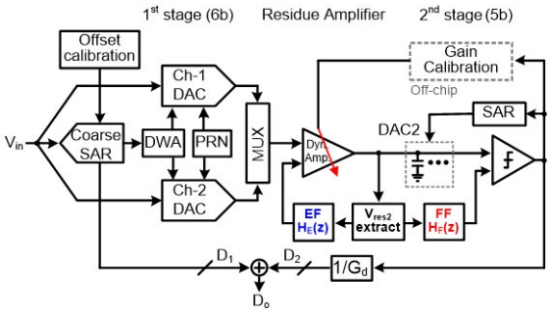


Fig. 1. Overall ADC Architecture and timing

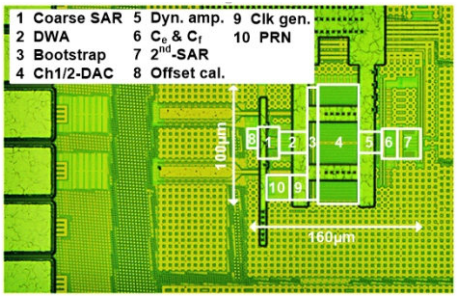


Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Song, Y. Zhu, C. H. Chan and R. P. Martins, "9.6 A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 164-166.

[2] Y. Song, Y. Zhu, C. -H. Chan and R. P. Martins, "A 40-MHz Bandwidth 75-dB SNDR Partial-Interleaving SAR-Assisted Noise -Shaping Pipeline ADC," in IEEE Journal of Solid-State Circuits, vol. 56, no. 6, pp. 1772-1783, June 2021

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 14-bit Split-Pipeline ADC with Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current

Jiaji Mao, Mingqiang Guo, Sai-Weng Sin, and Rui P. Martins

FEATURES

High-speed: 100MS/s Sampling Rate

High-resolution: 14-bit

Low power consumption: Optimizes duty-cycle ratio

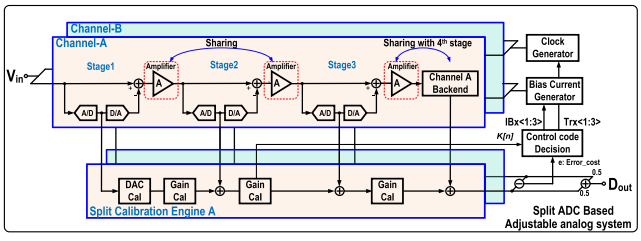
Background Calibration: Inter-stage gain (that includes settling) error

Silicon verified in 65 nm CMOS

DESCRIPTION

It presents a 14-bit split-pipeline opamp-sharing ADC, with background calibration that optimizes duty-cycle ratio and amplifier power consumption in the sharedopamp. Based on the interstage gain (that includes settling) error estimated by the split ADC calibration engine, the clock duty-cycle ratio and the bias current are adjusted to achieve better dynamic settling and resolution trade-offs.

Operating at 100MS/s with a 9-MHz input signal, the ADC achieves 46.5dB of Signal-to-Noise-and-Distortion Ratio (SNDR), and 59.6dB of Spurious-Free Dynamic Range (SFDR) before calibration, and after calibration, it improves to 71.7dB of SNDR and 84.4dB of SFDR, respectively. The ADC maintains an SNDR over 68.5dB within the full Nyquist bandwidth consuming 32mW of power, which yields a Walden Figure-of-Merit (FoM) of 147.2 fJ/conversion-step and a Schreier FoM of 160.4dB.



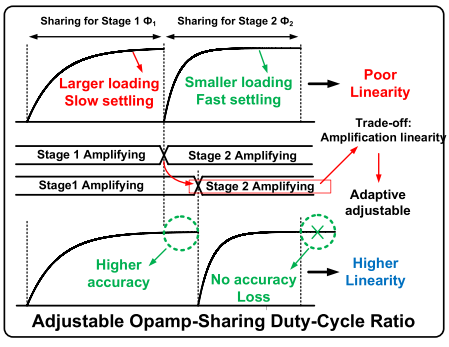


Fig. 1. The architecture split-pipeline ADC with self-adjustable opamp-sharing duty-cycle ratio.

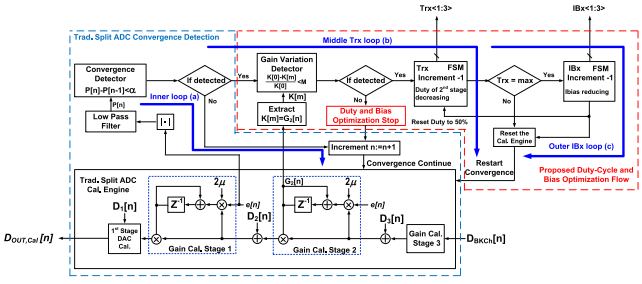


Fig. 2. The flow chart of the calibration algorithm.

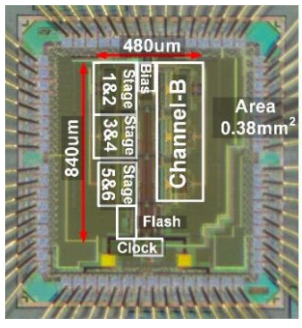


Fig. 3. Block diagram and chip micrograph of 7/8-way split TI ADC.

Publication(s)

[1] J. Mao, M. Guo, S. Sin and R. P. Martins, "A 14 bit Split Pipeline ADC with self-adjusted opamp-sharing duty cycle," IEEE ISSCC Student Research Preview, Feb. 2018.

[2] J. Mao, M. Guo, S. Sin and R. P. Martins, "A 14-Bit Split-Pipeline ADC With Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 10, pp. 1380-1384, Oct. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT, File no. 055/2012/A2), Research Committee of University of Macau (File no.: MYRG2017-00192-FST).

LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter with Ripple Calibration

Hanyu Wang, Sai-Weng Sin, Chi-Seng Lam, Franco Maloberti and R.P. Martins

FEATURES

First integrates on-chip DC-DC converter with the ADC, without the use of any LDOs

On-chip Boost DC-DC (power efficiency of 78.6%)

10-bit 500MS/s pipelined ADC

Ripple calibration technique

Silicon verified in 65 nm CMOS

DESCRIPTION

It presents a compact power management solution for a pipeline ADC, employing only a switching-mode power converter. By directly powering the ADC using a boost DC-DC converter, the power delivery network (PDN) exhibits an overall-high power efficiency. The proposed foreground ADC calibration calibrates the ripple error induced from the power converter, which obviates the need for well-regulated supply and reference voltage offered by low-efficiency linear low-dropout regulators (LDOs).

This chip integrates the boost DC-DC converter and the pipelined ADC with an external power inductor. Due to the periodic switching operation, the voltage ripple from the DC-DC converter is also periodic, which makes it feasible to sense and calibrate such errors. Nevertheless, ADC with rippled reference is unable to detect the ripple voltage directly. Thus, the backend ADC demands a clean DC reference source. This work reconfigures the ADC's first stage to a ripple-free sample-and-hold amplifier with a gain of four in the calibrating phase to generate a DC voltage V_CAL for backend ADC, finally implements a clean calibration reference in the foreground to achieve the ripple calibration purpose.

This 65-nm CMOS prototype occupies 2.34-mm² of total active area (9.4%-ADC, 2.6%-power controller and switches, and 88%-output capacitance). In the measurement, the boost converter, switching at 31.25MHz, converts a 0.5V input to 1.2V and delivers 22.8mW of power to the pipeline ADC. The boost DC-DC converter supplies all voltage domains, including analog/digital power supply and reference. The resulting overall system power efficiency is 78.6%. Sampled at 500MS/s, the ADC achieves a signal-to-noise and distortion ratio (SNDR) of 34.7/39.9dB without/with the ripple calibration for an input frequency of 177MHz, respectively.

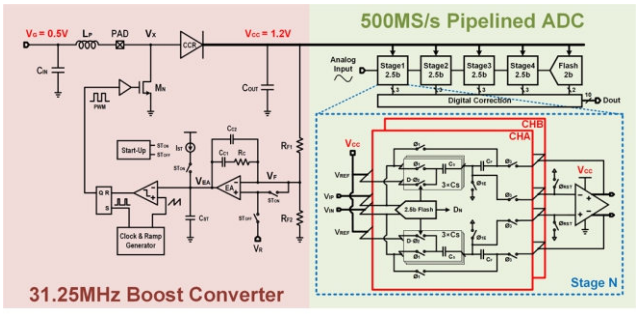


Fig. 1. Overview of the system architecture: the boost converter directly powers all pipelined ADC voltage domains, including power supply and reference voltage.

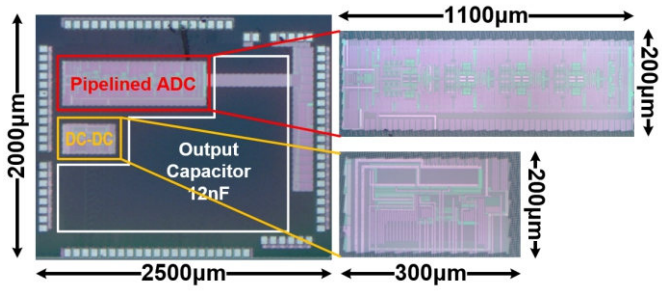


Fig. 2. Chip micrograph.

Publication(s)

[1] H. Wang, S. -W. Sin, C. -S. Lam, F. Maloberti and R. P. Martins, "LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter With Ripple Calibration," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, pp. 4174-4186, Dec. 2020.

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was supported in part by the Science and Technology Development Fund, Macau SAR, under Grant SKL-AMSV(UM)-2020-2022 and Grant SKL-AMSV-ADDITIONAL FUND and in part by the Research Committee of University of Macau under Grant MYRG2017-00192-FST.

A Wideband Noise-Shaping Pipeline-SAR ADC

Yan Song, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Bandwidth > 12.5MHz
Noise-Shaping Pipeline-SAR
Low power consumption, 4.5mW
Flip around error feedback Noise-shaping
Opamp reused
Silicon verified in 65 nm CMOS

DESCRIPTION

This paper presents a successive approximation register (SAR)-assisted noise-shaping (NS) pipeline architecture which breaks the speed bottleneck of existing SAR or SAR-assisted type NS analog-to-digital converters (ADCs). Rather than only for residue amplification and pipeline operation, the multiplying digital-to-analog converter (MDAC) is also reused as unity buffer and analog adder to realize the NS with error feedback (EF) structure in this design. While incorporating the proposed alternative loading capacitor (ALC) technique, an ideal 1st-order noise transfer function (NTF) is realized without additional feedback phase and only with a small analog circuit overhead. Unlike other NS SAR ADCs that involved amplification, the inter-stage gain attenuates the noise from the 2nd-stage comparator, thus leading to both high speed and resolution. Fabricated in 65 nm CMOS process, the prototype achieves a signal-to-noise-and-distortion ratio (SNDR) of 77.1 dB over 12.5 MHz BW with only 8 over–sampling ratio (OSR). Under a 1.2 V supply voltage, the ADC consumes 4.5 mW and exhibits a Scherier figure-of-merit (FoMs) of 171.5 dB.

The chip micro-photograph of the ADC prototype fabricates in 65nm CMOS with an active area of 0.014 mm2. The ADC has a BW that goes up to 12.5 MHz with 200 MS/s and OSR = 8. The FFT spectrum with a 1.5 MHz, −0.75dBFS sinusoidal input signal, with the prototype reaching the peak SNDR and a spurious-free-dynamic-range (SFDR) of 77.1 dB and 90.7 dB, respectively. The capacitor mismatch in the 1st-stage DAC is foreground calibrated by estimating the actual DAC bit-weight based on the least-mean-square (LMS) algorithm. The remaining harmonics appear in the spectrum due to the sampling and calibration accuracy limitations. Under a supply voltage of 1.2 V, the ADC consumes 4.5 mW and results in a FoMs of 171.5 dB. We measured 6 samples with the same testing setup, which confirm that they have a stable SNR and SNDR with only a small variation range less than 1 dB. The measured SNR and SNDR versus input amplitude, showing that the dynamic range (DR) is 78.5 dB. The measured SNR and SNDR versus OSR. Due to the noise floor, the SNR increases about 7 dB when the OSR doubles (with small OSRs), thus indicating a 1st-order NTF in our prototype.

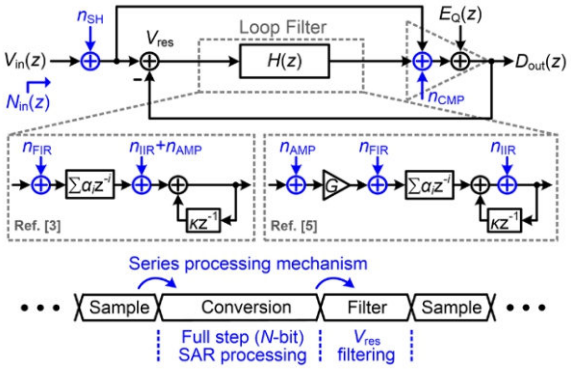


Fig. 1. Overall ADC Architecture and timing.

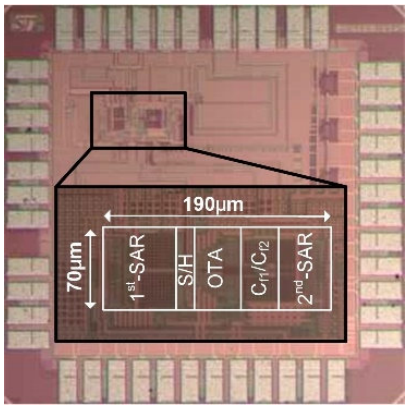


Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Song, Y. Zhu, C. Chan, L. Geng and R. P. Martins, "A 77dB SNDR 12.5MHz Bandwidth 0–1 MASH ∑Δ ADC Based on the Pipelined-SAR Structure," 2018 IEEE Symposium on VLSI Circuits, 2018, pp. 203-204.

[2] Y. Song, C. Chan, Y. Zhu and R. P. Martins, "A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC," in IEEE Journal of Solid-State Circuits, vol. 55, no. 2, pp. 312-321, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.