RESEARCH ABSTRACTS

High Resolution ADCs

A Low Supply Voltage Two-step TDC-assisted SAR ADC

Minglei Zhang, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Supply = 0.6V

SNDR >70dB

Low power consumption, 82uW

SAR+TDC architecture

Silicon verified in 65 nm CMOS

DESCRIPTION

This paper presents a low power-supplied 13-bit 20-MS/s time-to-digital converter (TDC)-assisted successive approximation register (SAR) analog-to-digital converter (ADC). In this hybrid architecture, the voltage-to-time converter and TDC realizes inherent process, voltage, and temperature (PVT) robustness by inner tracking, thus inducing no extra power and circuit overheads. The voltage-domain and time-domain speed-enhanced techniques accelerate the 1st and 2nd stage ADC conversion under a low power supply, respectively. Furthermore, in cooperated with detect-and-skip switching scheme in the SAR ADC and offset bit shifting scheme in the two-step TDC, the ADC achieves a 13-bit linearity. The prototype ADC was fabricated in a 65-nm CMOS technology with a power supply of 0.6 V, achieving 71.0-dB signal-to-noise and distortion ratio (SNDR) and 89.5-dB spurious-free dynamic range with a Nyquist input at 20 MS/s, while with a Schreier figure-of-merit of 181.9 dB.

The prototype two-step TDC-assisted SAR ADC was fabricated in a 1P9M 65-nm CMOS process. Fig. 15 shows its die photograph with an active area of 0.053 mm2. The power supply and SAR ADC reference both have a voltage of 0.6 V. Large bypass capacitance is added on chip to stabilize the reference voltage, and the output data of the ADC is decimated by 5 to mitigate the ripple that couples through the PAD ring. The unit capacitors in the SAR ADC are custom designed encapsulated metal-oxide-metal capacitors. The ADC uses one-time on-chip foreground calibration for the offset and FS output time of the VTC, while the background bit shifting is applied to the TRG offset at off chip as introduced in Section IV-B. All the other error sources are covered by the redundancies between stages and the intrinsic matching.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) with a conversion rate of 20 MS/s. The measured DNL and INL errors are within −0.74/+0.72 LSB and −1.03/+1.31 LSB, respectively, benefiting from the high-linear CDAC in the SAR ADC. The measured 66 536-point fast Fourier transform (FFT) spectrums with both the LF and Nyquist input signals at 20 MS/s. The ADC achieves 71.5-dB SNDR and 91.9-dB spurious-free dynamic range (SFDR) with an input frequency of 0.49 MHz, and 71.0-dB SNDR and 89.5-dB SFDR with an input frequency of 9.98 MHz. The measured SNDR and SFDR versus various ADC input frequencies with a sampling rate of 20 MS/s. The SNDR and SFDR stay above 69.5 dB and 84.8 dB, respectively, even with an 18-MHz input signal.

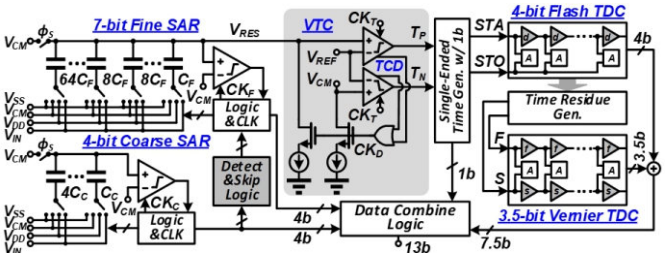

Fig. 1. Overall ADC Architecture and timing

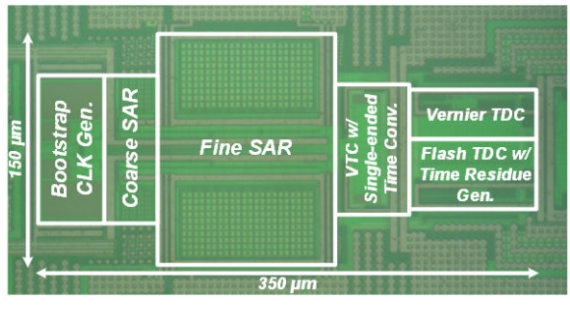

Fig. 2. Chip micrograph.

Publication(s)

[1] M. Zhang, C.-H. Chan, Y. Zhu, and R. P. Martins, “A 0.6V 13b 20MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed-enhanced techniques, in IEEE ISSCC Dig. Tech. Papers, Feb. 2019, pp. 66–67.

[2] M. Zhang, C. Chan, Y. Zhu and R. P. Martins, "A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques," in IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3396-3409, Dec. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator With Multirate Opamp Sharing

Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti and R.P. Martins

FEATURES

Multirate Opamp Sharing Firstly Proposed in MASH

Op-amp sharing to improve the power efficiency

SAR utilized (offset insensitive)

Multi-rate mode at 120/240MHz

Silicon verified in 65 nm CMOS

DESCRIPTION

It is a DT 2-1 MASH Delta-Sigma modulator with multirate opamp sharing technique for ADC, targeting the optimization of power efficiency in active blocks, like opamps and quantizers. Through the allocation of different settling times to the opamps and by adopting the multirate technique, the power of the shared opamps is utilized more efficiently, and the 4-bit SAR quantizer and the DWA in the first stage enjoy additional operation time. Moreover, the stringent timing issue of the first quantizer and DWA caused by the horizontal sharing scheme was correctly addressed, thus allowing the incorporation of a SAR quantizer in the design. The use of a SAR is not only more power and area efficient, but free from the input-referred offset limitations of the quantizer.

Fabricated in 65-nm CMOS, this modulator runs at multirate 120/240MHz achieves a mean SNDR of 77.1dB for a 5MHz bandwidth, consuming 4.2mW from a 1.2V supply and occupying 0.066mm² core area. It exhibits a Walden FoM of 69.7fJ/conv-step and a Schreier FoM of 167.9dB based on SNDR.

The measurement results show that this modulator achieved state-of-the-art performance. It enhances the opamps' power efficiency and the overall resolution further through allocating more reasonable settling time based on their various performance requests and capacitive loading. Therefore, we successfully exploit a high-resolution DT MASH at a signal bandwidth of 5MHz for LTE standards.

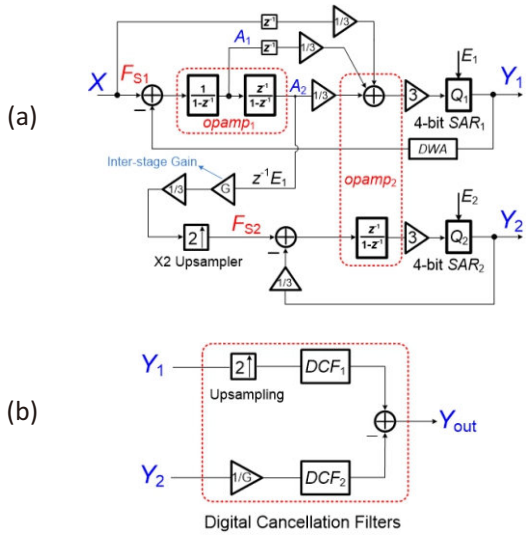

Fig. 1. (a) The proposed DT 2-1 MASH architecture and (b) its digital cancellation filters.

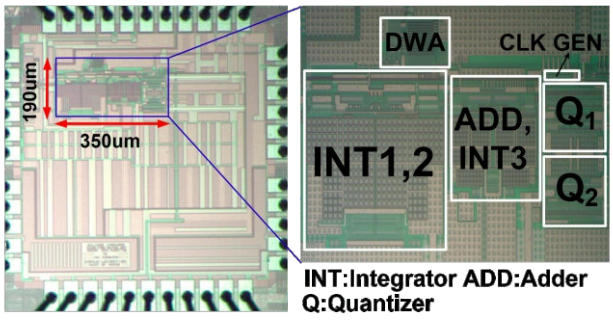

Fig. 2. Chip micrograph.

Publication(s)

[1] Liang Qi, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti, "A 12.5-ENOB 5MHz BW 4.2mW DT Multirate 2-1 MASH ΔΣ Modulator with Horizontal/Vertical Opamp Sharing in 65nm CMOS," ISSCC student research preview presentation, Feb. 2016.

[2] Liang Qi, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti, "A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 10, pp. 2641-2654, Oct. 2017.

Sponsorship

This work was supported by the Research Committee of University of Macau and Macao Science and Technology Development Fund(FDCT) under Grant FDCT/055/2012/A2.

A 10-MHz Bandwidth Two-Path Third-Order ΣΔ Modulator with Cross-Coupling Branches

Da Feng, Edoardo Bonizzoni, Franco Maloberti, Sai-Weng Sin and Rui Paulo Martins

FEATURES

Two-path architecture to reduce the channel speed

With an extra zero in modified NTF

Reduce the number of op-amps

Cross-coupling paths to realize the lowpass feature

Silicon verified in 65 nm CMOS

DESCRIPTION

It is a two-path discrete-time (DT) third-order sigma-delta (ΣΔ) modulator with an extra zero in the noise transfer function (NTF) located at z = −1, reducing the NTF coefficients of intermediate terms for optimal design. Applying polyphase decomposition of the NTF, the proposed ΣΔ modulator is implemented by a two-path architecture with cross-coupling branches.

This architecture optimizes the conventional 3rd-order modulator with a topological transformation of the basic scheme, by adding an extra zero in the NTF to reduce the intermediate terms. In addition, the extra zero ensures that applying the NTF polyphase decomposition technique, the proposed ΣΔ modulator can be implemented by a two-path architecture with cross-coupling branches, leading to performance at the state-of-the-art.

With cross-coupling branches, this modulator doubles the OSR for a given sampling frequency. The result is an increase of 3.5 bit in the resolution and a reduction of the power consumption. The techniques proposed in this brief allow using only two op-amps in each path at the cost of 1-bit of resolution.

The 65-nm CMOS experimental chip running at a sampling rate of 340 MHz achieves a DR of 68.8 dB and a SNDR of 65.4 dB for a 10-MHz signal bandwidth, occupying an active area of 0.2257 mm² and consuming 19.47 mW from a 1.2-V supply. The measured performance leads to a Walden FoM of 648.6 fJ/conversion-step and to a Schreier FoM of 152.4 dB (SNDR-based), respectively. With a lower FoMw and a smaller active area, the sampling frequency is about 40% higher than that of the conventional discrete-time implementations with the same CMOS technology.

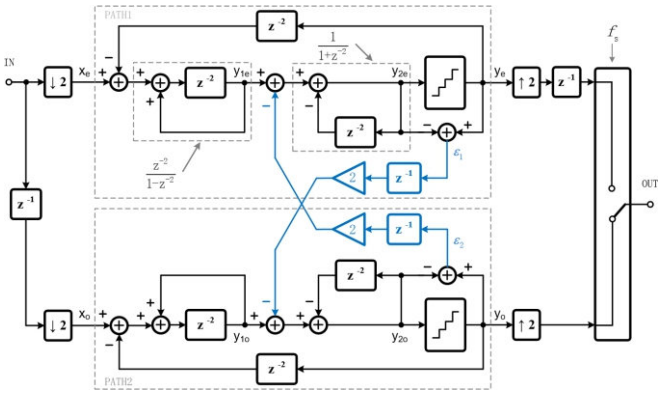

Fig. 1. Block diagram of the proposed third-order ΣΔ Modulator using a two-path architecture with cross-coupling branches.

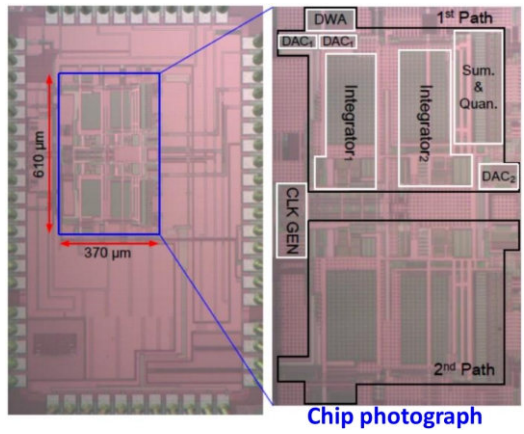

Fig. 2. Chip micrograph.

Publication(s)

[1] D. Feng, E. Bonizzoni, F. Maloberti, S. Sin and R. Martins, "A 10-MHz Bandwidth Two-Path Third-Order ΔΣ Modulator With Cross-Coupling Branches," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 10, pp. 1410-1414, Oct. 2018.

Sponsorship

This work was supported by Macau Science and Technology Development Fund (FDCT) under Grant FDCT/055/2012/A2.

A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance

Liang Qi, Ankesh Jain, Dongyang Jiang, Sai-Weng Sin, Seng-Pan U, Rui P. Martins and Maurits Ortmanns

FEATURES

Sturdy 3-0 MASH with wider bandwidth

Multibit DAC Nonlinearity Mitigation

NC works as dithering

Quantization Error Extraction in SAR

For 4G LTE-A Application

Silicon verified in 28 nm CMOS

DESCRIPTION

It is a dual-loop noise-coupling-assisted continuous time (CT) sturdy multi-stage noise shaping (SMASH) ΔΣ modulator (DSM), employing 1.5bit/4bit quantizers, respectively. The proposed SMASH can equivalently work as an overall fourth-order DSM with 4bit internal quantization.

To achieve 50MHz signal bandwidth for LTE-A applications, it is almost impossible to continue using a DT MASH architecture. Instead, a CT solution allows implementing such a large signal bandwidth. A CT sturdy MASH poses higher potential over a CT MASH owing to its relaxed matching requirement. Nevertheless, the quantization error cancellation and its extraction are still challenging in the CT domain.

On the other hand, DAC non-linearity becomes problematic with multi-GHz sampling frequency since DEM becomes less effective at low OSR while DAC calibrations often require large power and area consumptions.

A zeroth-order topology is intentionally selected for the second loop to accurately implement a unity-gain signal transfer function (STF) such that the 1.5bit noise leakage is minimized. Thereby, the proposed SMASH can equivalently work as an overall fourth-order DSM with 4bit quantization. The noise coupling applied in the SMASH whitens 1.5bit quantization noise and further reduces its in-band tone power, while a finite impulse response (FIR) filter integrated into the outermost feedback path suppresses the out-of-band noise power of the DAC input. Together, this circumvents any linearization technique for multibit DACs.

Fabricated in 28nm CMOS technology, this prototype measures an SNDR of 76.6dB and an SFDR of 87.9dB over a 50MHz bandwidth, consuming 29.2mW from 1.2V/1.5V supplies and occupying an active area of 0.085mm². It exhibits a Schreier figure-of-merit (SNDR) of 168.9dB.

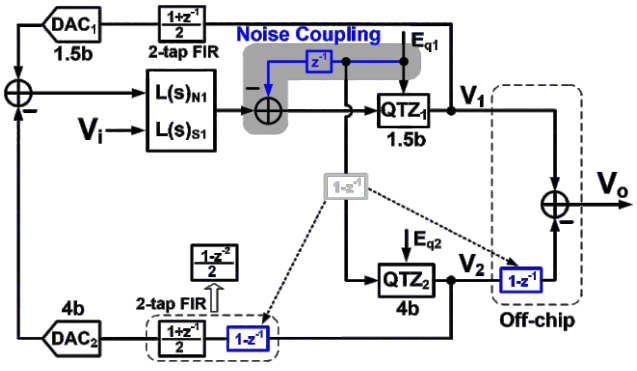

Fig. 1. Block diagram of the proposed CT dual-loop SMASH

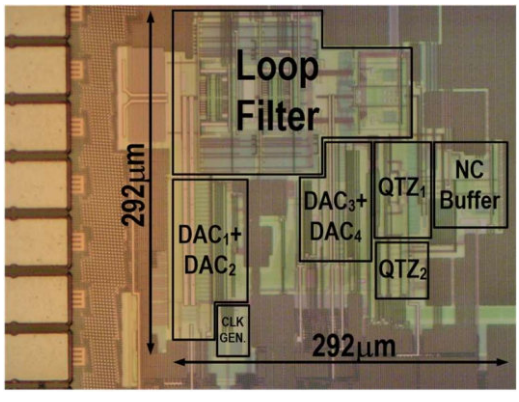

Fig. 2. Chip micrograph.

Publication(s)

[1] L. Qi, A. Jain, D. Jiang, S. Sin, R. P. Martins and M. Ortmanns, "20.5 A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS," 2019 IEEE International Solid-State Circuits Conference - (ISSCC), 2019, pp. 336-338.

[2] L. Qi, A. Jain, D. Jiang, S. Sin, R. P. Martins and M. Ortmanns, "A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance," in IEEE Journal of Solid-State Circuits, vol. 55, no. 2, pp. 344-355, Feb. 2020

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was funded by the Science and Technology Development Fund, Macau SAR (File no.076/2017/A2 & SKL-AMSV-2017-2019(DP)).

A 550µW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental ΣΔ ADC with 256 clock cycles in 65nm CMOS

Biao Wang, Sai-Weng Sin, Seng-Pan U, Franco Maloberti and R.P. Martins

FEATURES

First Linear-Exponential IADC

Linear-phase: lower KT/C penalty factor

Exponential-phase: Boosting the SQNR

Noise-coupling technique

Silicon verified in 65 nm CMOS

DESCRIPTION

It is an incremental analog-to-digital converter (IADC) with a two-phase linear-exponential accumulation loop. In the linear phase, the loop works as a first-order structure. The noise-coupling path is then enabled in the exponential phase thus boosting the SQNR exponentially with a few numbers of clock cycles.

The two-phase scheme combines the advantages of the thermal noise suppression in the 1st order IADC and SQNR boosting in the exponential mode. The uniform-exponential weight function allows the data weighted averaging (DWA) technique to work well, leading to the rotation of the multi-bit DAC mismatch error. Meanwhile, this scheme does not destroy the notches, which can be utilized to suppress the line noise.

In the initial 246 cycles of the linear phase, the IADC works as a 1st-order architecture and fully utilizes the oversampling operation on thermal noise suppression. After that, the circuit reconfigured as an exponential phase, boosts the SQNR exponentially in 10 clock cycles. It achieved the exponential accumulation with the noise-coupling ping-pong SC circuit. The uniform-exponential weighting allows the DWA technique to work well in improving the linearity by rotating the multi-bit DAC elements.

The prototype IADC that has been implemented in a 1P7M 65nm CMOS process, occupying an active area of 0.134 mm². With 1.2V supply, the ADC reaches an SNDR/DR of 100.8dB/101.8dB with 20kHz BW while consuming 550µW, resulting in an Walden/Schreier FoMW/FoMS of 153fJ /176.4dB, respectively. The DWA technique produces high linearity with DNL/INL of 0.27/0.84 LSBs.

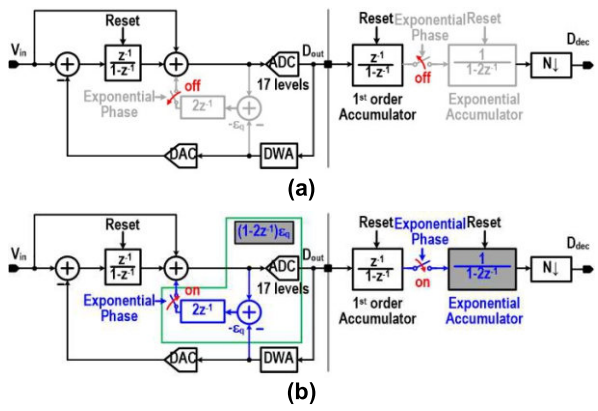

Fig. 1. Block diagram of the proposed Incremental ADC at (a) Linear-Phase and (b) Exponential-Phase.

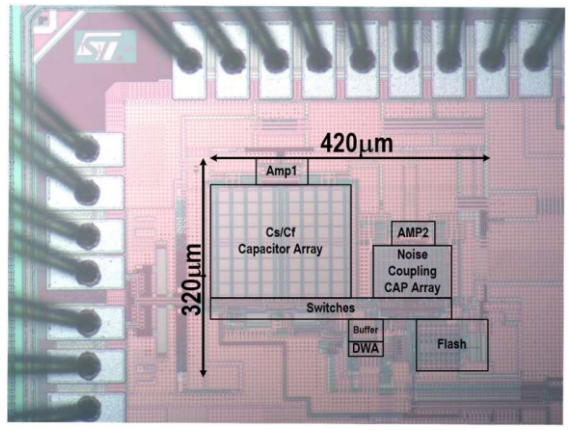

Fig. 2. Chip micrograph.

Publication(s)

[1] B. Wang, S. Sin, U. Seng-Pan, F. Maloberti and R. P. Martins, "A 550µW 20kHz BW 100.8DB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65NM CMOS," 2018 IEEE Symposium on VLSI Circuits, 2018, pp. 207-208.

[2] B. Wang, S. Sin, S. U., F. Maloberti and R. P. Martins, "A 550-µW 20-kHz BW 100.8-dB SNDR Linear- Exponential Multi-Bit Incremental ΔΣ ADC With 256 Clock Cycles in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 54, no. 4, pp. 1161-1172, April 2019. (Invited Special Issue of VLSI).

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was supported in part by Science and Technology Development Fund, Macau under Grant 055/2012/A2 and in part by the Research Committee of University of Macau under Grant MYRG2017-00192-FST.

A Time-Interleaved 2nd-Order Δ Σ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation

Dongyang Jiang, Liang Qi, Sai-Weng Sin, Franco Maloberti and R.P. Martins

FEATURES

Digital-feedforward extrapolating TI ΔΣM
Quadrable OSR = 208
Full-extrapolation in digital domain
Dithering to enhance the linearity
Silicon verified in 28 nm CMOS

DESCRIPTION

It presents a 4x time-interleaved (TI) 2nd-order discrete-time (DT) delta-sigma modulator (DSM). We propose a digital feed-forward extrapolation by first digitizing the internal analog nodes' information from one channel, and then extrapolating the other channels in the digital domain. As a result, this DSM only needs two operational amplifiers (op-amps) to realize four interleaving paths, thus reducing analog hardware overheads.

The digital feedforward extrapolation works by firstly digitizing the essential analog nodes' information (i.e., X, P_1, and P_2) from one channel and then fully extrapolating the other channels in the digital domain. This operation not only removes all burden analog adders, but also bypasses stringent matching requirements between the analog/digital extrapolating gains. Meanwhile, we linearize the digital feed-forward paths through injected dithering.

Fabricated in 28nm CMOS technology, the channel's clock is 520 MS/s, which leads to an equivalent sampling rate of 2.08GS/s. the increased sampling frequency results in two possible directions: 1) increase the OSR but with a fixed BW or 2) increase the BW with a fixed OSR. This implementation is the latter case, such ADC increased the effective output OSR from 52 to 208 with the BW fixed at 5MHz. The achieved peak SNDR is 86.1-dB. The ADC consumes a total of 23.1-mW with 1/1.15/1.5V power supplies, which results in a Schreier Figure of Merit (FOM) (based on SNDR) of 169.5dB.

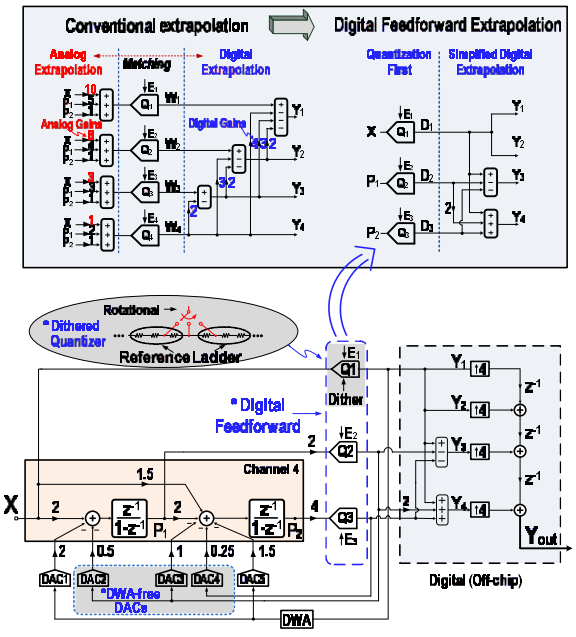

Fig. 1. System-level architecture of the extrapolating TI DSM (top) with conventional/ digital feedforward extrapolation comparison (bottom.)

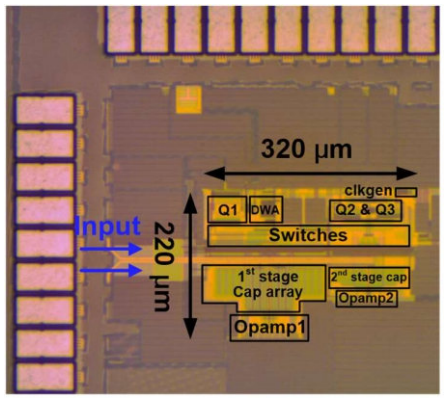

Fig. 2. Chip micrograph.

Publication(s)

[1] D. Jiang, L. Qi, S. -W. Sin, F. Maloberti and R. P. Martins, "A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved 2nd-Order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS," 2020 IEEE Symposium on VLSI Circuits, 2020, pp. 1-2

[2] D. Jiang, L. Qi, S. -W. Sin, F. Maloberti and R. P. Martins, "A Time-Interleaved 2nd-Order Δ Σ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation," in IEEE Journal of Solid-State Circuits, 2021, in early access.

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was funded by The Science and Technology Development Fund, Macau SAR [File no. 076/2017/A2, SKL-AMSV(UM)-2020-2022], and The Ministry of Science and Technology, China. [File no. EF001/AMSV/2018/MOST].