RESEARCH ABSTRACTS

Wireline Integrated Circuits

A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS

Chao Fan, Wei-Han Yu, Pui-In Mak, Rui P. Martins

FEATURES

SCH output wireline driver

FFE support

PAM-4 modulated TX

High throughput, 10 Gb/s

Low energy consumption, 0.16 pJ/bit

Silicon verified in TSMC 28nm CMOS

DESCRIPTION

This work proposes an SST-CML-Hybrid (SCH) output driver, and its corresponding hybrid-path feed-forward equalization (FFE) scheme, to enhance the energy efficiency of a PAM-4 transmitter (TX). Specifically, the SCH driver features one SST branch + one CML branch to co-synthesize the PAM-4 data, reducing substantially the signaling power, switching power and equalization power. The PAM-4 TX further integrates a half-rate serializer with 4-bit 3-tap FFE, duty-cycle correction circuits and a T-coil output matching network. Prototyped in 28-nm CMOS, the PAM-4 TX achieves a broadband return loss <; -10dB up to 50 GHz, and occupies a compact die area of 0.0345 mm². Operating at 40 Gb/s and at a 0.9-V supply, the TX dissipates 19.5 mW, of which 6.4 mW is due to the SCH driver. The corresponding energy efficiencies are 0.16 and 0.5 pJ/bit for the SCH driver and TX, respectively; both compare favorably with the prior art

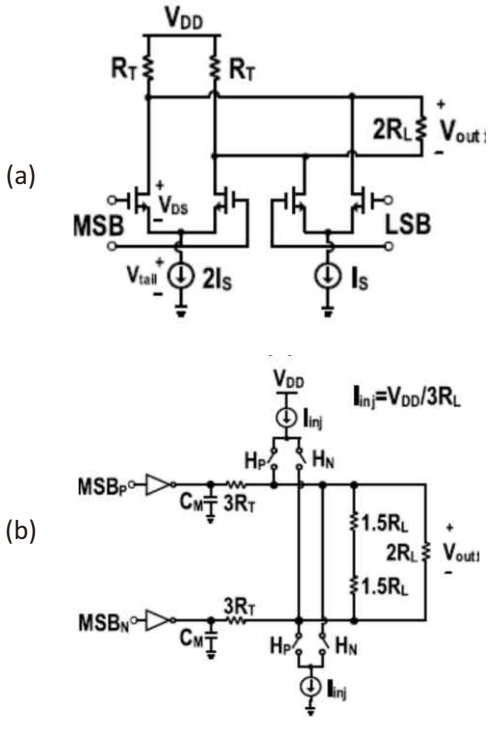


Fig. 1. (a) Conventional CML, and (b) proposed SCH PAM-4 driver.

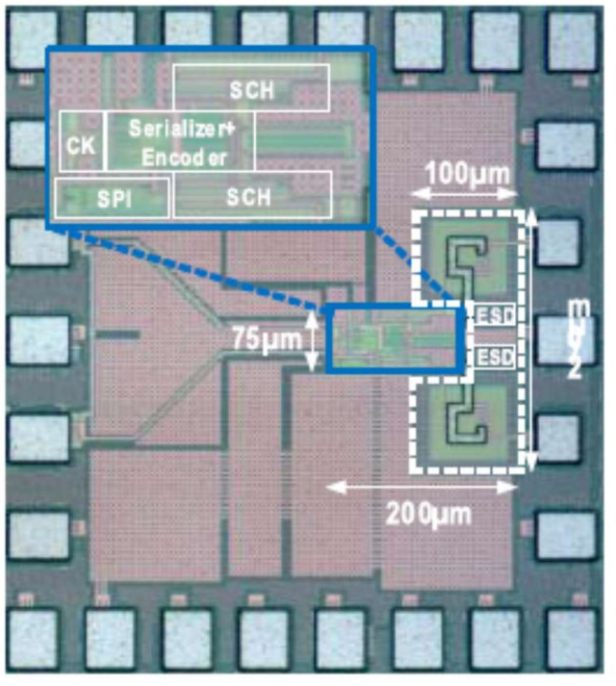


Fig. 2. Chip micrograph.

Publication(s)

[1] Chao Fan, Wei-Han Yu, Pui-In Mak, Rui P. Martins, "A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS," IEEE Transactions on Circuits and Systems – I, vol. 66, pp. 4850-4861, Dec. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 0.08mm² 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6 dBc/Hz FOM and 130kHz 1/f³ PN Corner

Hao Guo, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

Multi-resonant-RLCM-tank VCO

Single-turn multi-tap inductor with high-Q 1st-, 2nd- and 3rd-harmonic resonances

Remove the constraint of the DM-to-CM capacitance ratio with CM-only tunable capacitors

Significantly suppress the transistor noise to phase noise conversion

Silicon verified in 65nm CMOS

DESCRIPTION

We report a near-millimeter-wave VCO using a multi-resonant RLCM tank that enables compact and high-FoM implementation. Specifically, a single turn multi-tap inductor with k<0 and CM-only tunable capacitors, without the constraint of the DM-to-CM capacitance ratio, enable high-Q high-impedance resonances at different oscillation frequencies (e.g., F_{OSC}, $2F_{OSC}$, and $3F_{OSC}$.

Our VCO was prototyped in 65nm CMOS. The active and capacitive elements are laid out inside the inductor footprint for area savings. With our tunable capacitance range and resolution, the PN and FoM after manual resonance alignment is 5dB (8dB) better at a 1MHz (100kHz) offset. When operating in a PLL, C_{CM} can be tuned for frequency locking first, then C_2 to optimize the PN performance.

Benchmarking with the recent mm-wave VCOs, this work succeeds in improving both FoM and FoM_T over a wide range of frequency offsets. We also achieve a low 1/f³ PN corner and a small core area. Measuring a TR of 16% from 25.5 to 29.9GHz, our VCO achieves a FoM@1MHz up to 191.6dBc/Hz that is at least 2dB better than the prior art mm-wave VCOs in both CMOS and BiCMOS.

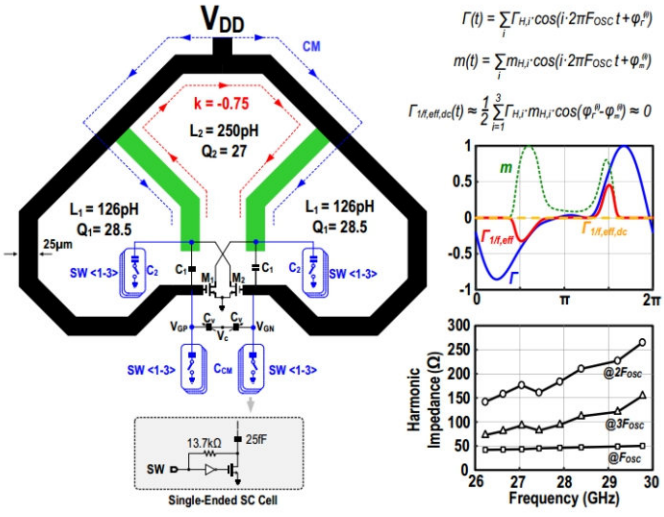


Fig. 1. Left: Proposed compact single-turn multi-tap inductor with high Q_1 and Q_2. Right: Simulated Γ, m and $\Gamma_{1/f,eff}$ in one cycle and harmonic impedances over TR.

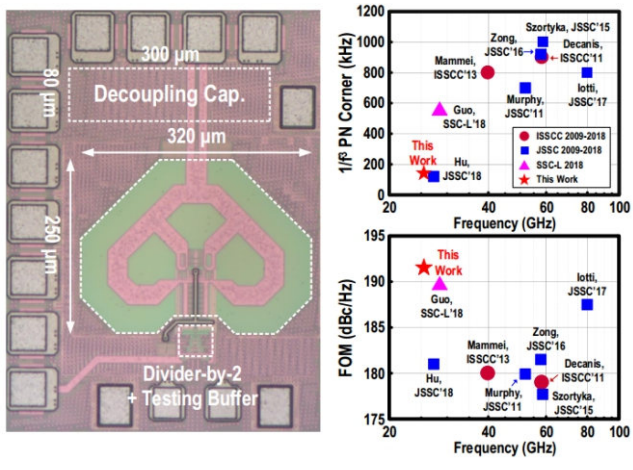


Fig. 2. Left: Die photo of the fabricated mm-wave VCO in 65nm CMOS. Right: Plots of FOM and 1/f³ PN corner with respect to more state-of-the-art mm-wave VCOs.

Publication(s)

[1] H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.08mm2 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6-dBc/Hz FOM and 130kHz 1/f³ PN Corner," IEEE International Solid-State Circuits Conference (ISSCC), pp. 410-411, Feb. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS

Xiaoteng Zhao, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

Half-rate bang-bang clock and data recovery circuit

Trimodal (NRZ/PAM-4/PAM-8)

Single-loop phase tracking technique

Silicon verified in 65nm CMOS

DESCRIPTION

We develop a half-rate bang-bang clock and data recovery (BBCDR) circuit supporting the trimodal (NRZ/PAM-4/PAM-8) operation. The observation of their crossover points distribution at the transitions introduces the single-loop phase tracking technique. In addition, low-power techniques at both the architecture and circuit levels are employed to greatly improve the overall energy efficiency and multiply data throughput by increasing the number of levels on the magnitude.

Fabricated in 28-nm CMOS, our prototype scores a 0.29/0.17/0.14 pJ/bit efficiency at 14.4/28.8/43.2 Gb/s under NRZ/PAM-4/PAM-8 modes, respectively. The jitter is <0.53 ps (integrated from 100 Hz to 1 GHz) with approximately-equivalent constant loop bandwidth, and we achieve at least 1-UI_{pp} jitter tolerance up to 10 MHz for all three modes.

Benchmarking this work with the recent state-of-the arts, we first design a trimodal (NRZ/PAM-4/PAM-8) BBCDR circuit and exhibit favorable energy efficiency (0.14 to 0.29 pJ/bit) and integrated jitter (0.48 to 0.53 ps).

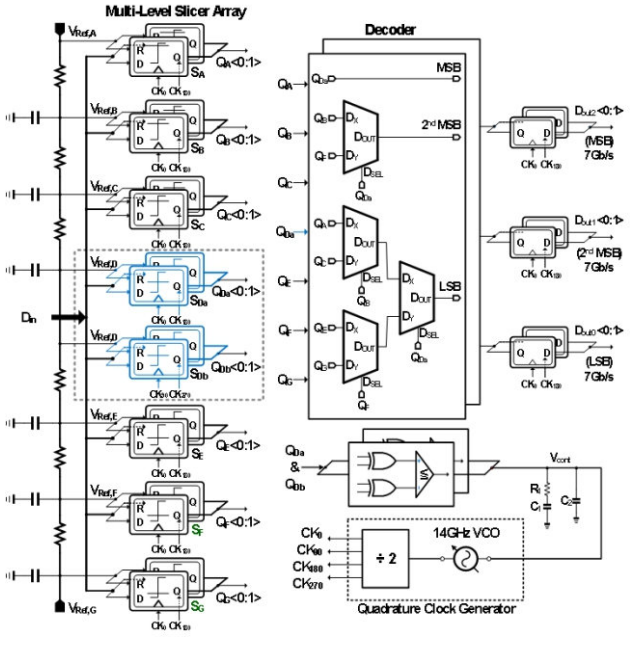


Fig. 1. Complete schematic of our trimodal BBCDR.

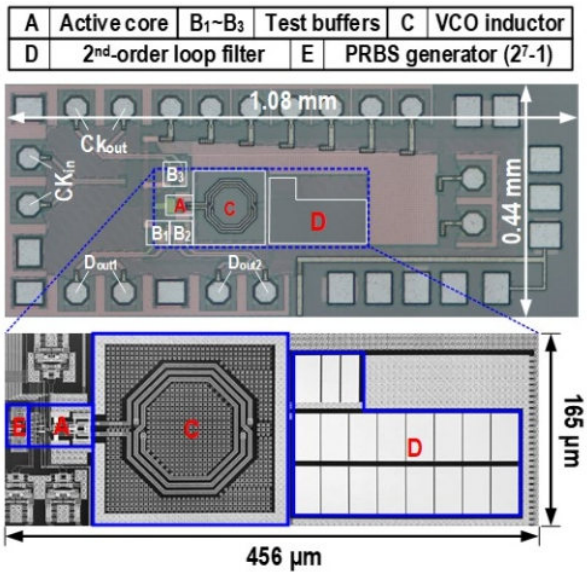


Fig. 2. Chip photo with area breakdown and detail of the core layout.

Publication(s)

[1] X. Zhao, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS," IEEE Transactions on Circuits and Systems - I, vol. 68, pp. 89-102, Jan. 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 0.0018-mm² 153% Locking-Range CML-Based Divider-by-2 With Tunable Self-Resonant Frequency Using an Auxiliary Negative-g_m Cell

Xiaoteng Zhao, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

CML-based divider-by-2

Tunable self-resonant frequency using an auxiliary negative-g_m cell

Silicon verified in 65nm CMOS

DESCRIPTION

High-performance radio frequency to millimeter-wave frequency dividers are the cornerstone of advanced local-oscillator generators for the 5th-generation (5G New Radio,and clock synchronization in the wireline and optical transceivers.

We report an area-efficient current-mode logic (CML)-based divider, with a tunable self-resonant frequency for locking range (LR) extension.

Specifically, a negative-g_m (NG) cell is inserted between the resonated shunt-peaking inductor and the load resistor to shift the divider's sensitivity curve (SC), enabling concurrently a higher operating frequency and a wider LR. We use the injection-locking concept, together with a graphical phasor diagram with the frequency-phase information to systematically explain the LR-extension mechanism.

Prototyped in a 65-nm CMOS, the divider occupies a tiny active area of 0.0018 mm². The measured LR is 153% (4–30 GHz) while consuming 4.06–4.28 mW at 30 GHz under a single 1.2-V supply.

Comparing the performance of the proposed divider with the state-of-the-art. This work succeeds in enhancing the flexibility of f_{SR} with an LR of 153% to achieve good figure of-merits: FOM_{Pdc} of 25.5 dB and FOM_P of 71.5.

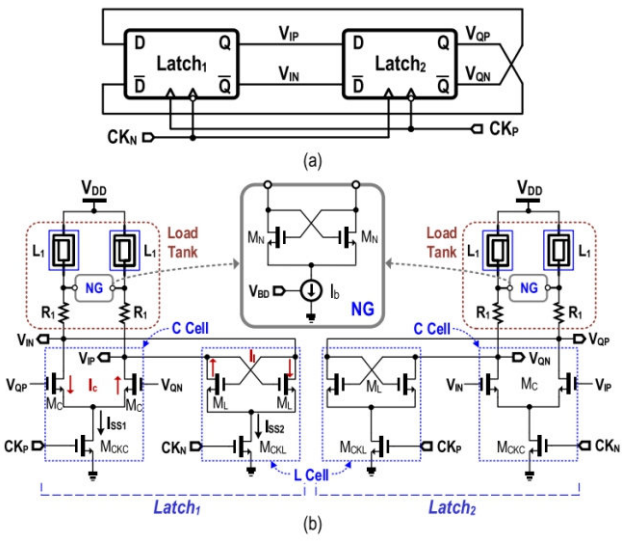


Fig. 1. (a) Two latches view and (b) detailed schematic of our proposed CML-based frequency divider-by-2.

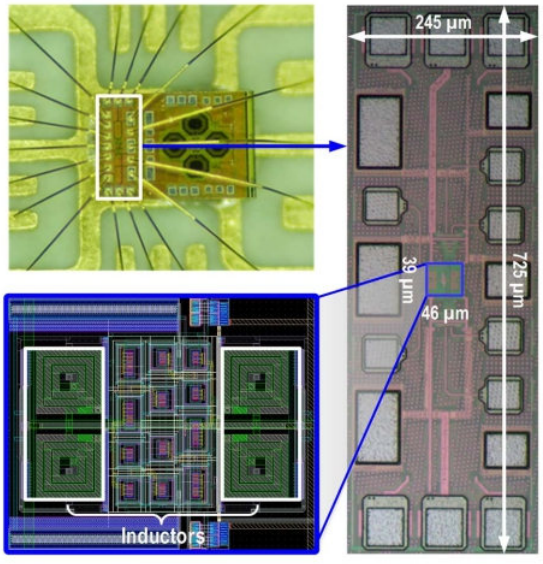


Fig. 2. Chip micrograph with bonding scheme and core layout detail.

Publication(s)

[1] X. Zhao, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.0018-mm² 153%-Locking-Range CML-Based Divider-by-2 with Tunable Self-Resonant Frequency Using an Auxiliary Negative-g_m Cell," IEEE Transactions on Circuits and Systems - I, vol. 66, pp. 3330-3339, Sep. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-Only Switched-Capacitor Arrays With a 187.6-dBc/Hz FOM

Yunbo Huang, Yong Chen, Hao Guo, Pui-In Mak, and Rui P. Martins

FEATURES

Current-reused VCO

Single-turn multi-tap inductor

Differential-only switched-capacitor arrays

Silicon verified in 65nm CMOS

DESCRIPTION

A millimeter-wave current-reuse voltage-controlled oscillator (VCO) features a single-turn multi-tap inductor and two separate differential-only switched-capacitor arrays to improve the power efficiency and phase noise (PN). A single-branch complementary VCO in conjunction with a multi-resonant resistor-inductor-capacitor-mutual inductance (RLCM) tank allows sharing the bias current and reshaping the impulse-sensitivity-function. The latter is based on an area-efficient RLCM tank to concurrently generate two high-quality factor differential-mode resonances at the 1st and 2nd-harmonic oscillation frequencies. and the core area is 0.116 mm².

Fabricated in 65-nm CMOS technology, our VCO at 27.7 GHz shows a PN of −109.91-dBc/Hz at 1-MHz offset (after on-chip divider-by-2), while consuming just 3.3 mW at a 1.1-V supply. It corresponds to a Figure-of-Merit (FOM) of 187.6 dBc/Hz. The frequency tuning range is 15.3% (25.2 to 29.4 GHz) and the core area is 0.116 mm².

Benchmarking with the prior arts, the current-reuse scheme allows our VCO to obtain a competitive FOM (187.4 dBc/Hz ±0.2 dB) at 1-MHz offset with the lower power (<3.5 mW) across the entire 15.3% TR.

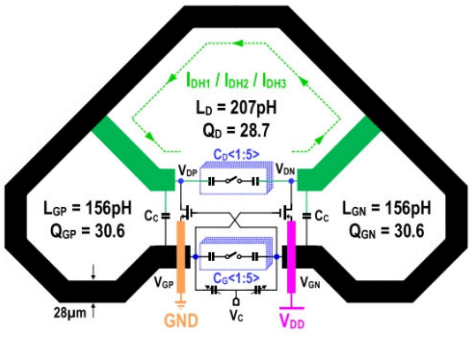


Fig. 1. Schematic of the proposed current-reuse VCO.

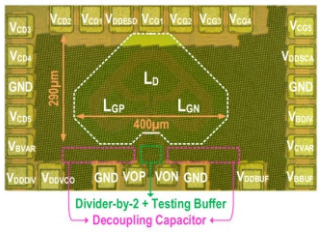


Fig. 2. Chip photo of the designed current-reuse VCO.

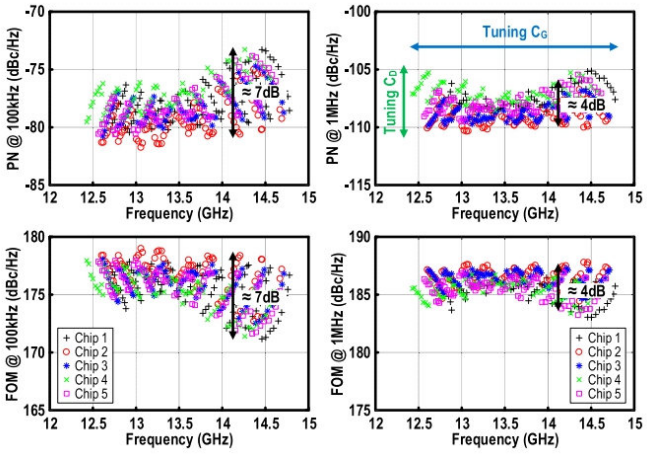


Fig. 3. Multi-chip tests for different SCAs settings.

Publication(s)

[1] Y. Huang, Y. Chen, H. Guo, P.-I. Mak, and R. P. Martins, "A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-only Switched-Capacitor Arrays with a 187.6-dBc/Hz FOM," IEEE Transactions on Circuits and Systems - I, vol. 67, pp. 3704-3717, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning

Hao Guo, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

Wideband-harmonic-shaping VCO

A tiny-coil head resonator for CM bandwidth extension

Wideband 1/f³ PN corner reduction without harmonic tuning

Silicon verified in 65nm CMOS

DESCRIPTION

We present a wideband-harmonic-shaping VCO that exhibits concurrently a high FoM and wideband 1/f3 PN-corner reduction without manual harmonic tuning. We devise a multi-LC tank with a high-and-wideband CM resonance at $2F_{OSC}$ and a low-and-wideband DM resonance at $3F_{OSC}$. To explain later, this scheme optimally shapes the ISF noise transfer over the wide TR from both the magnitude and phase perspectives. The key elements are a 1:2-turn transformer, a tiny coil head resonator (HR), and a switched-capacitor array (SCA) for one-dimensional frequency tuning.

The VCO fabricated in 65nm CMOS occupies a 0.24 mm2 core area. The $PN_{@10MHz}$ is -149dBc/Hz at F_{min}, and -146.1dBc/Hz at F_{max}, resulting in a $FoM_{@10MHz}$ of 195.1dBc/Hz at F_{min} and 196.9dBc/Hz at F_{max}. The corresponding 1/f³ PN corner increases from 90 to 180kHz due to AM-PM conversion, which identifies the corner frequency within a 3dB FoM degradation from $FoM_{@10MHz}$.

Benchmarking with other RF VCOs that exploit the narrowband resonance at $2F_{OSC}$, this work features a wideband high-impedance $|Z_{CM}|$ allowing $FoM_{@10MHz}$ improvement without manual harmonic tuning, while showing less 1/f³ PN corner variation. Specifically, our VCO shows a better $FoM_{@10MHz}$, covers a wider TR of 23.9% and operates at a much lower supply voltage of 0.4V. Compared to the prior work that uses no harmonic tuning, our VCO exhibits a smaller variation of $FoM_{@10MHz}$ of 1.8dB and 1/f³ PN corner of 90kHz over the respective TRs.

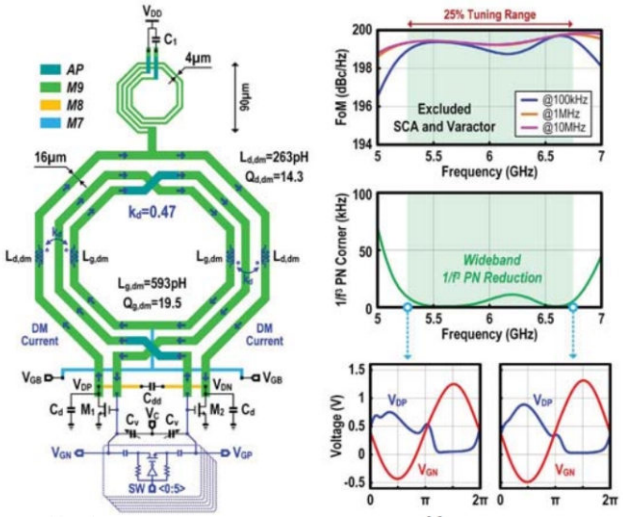


Fig. 1. Left: Detail of the proposed complete VCO. Right: Wideband FoM and 1/f³ PN-corner reduction without manual harmonic tuning.

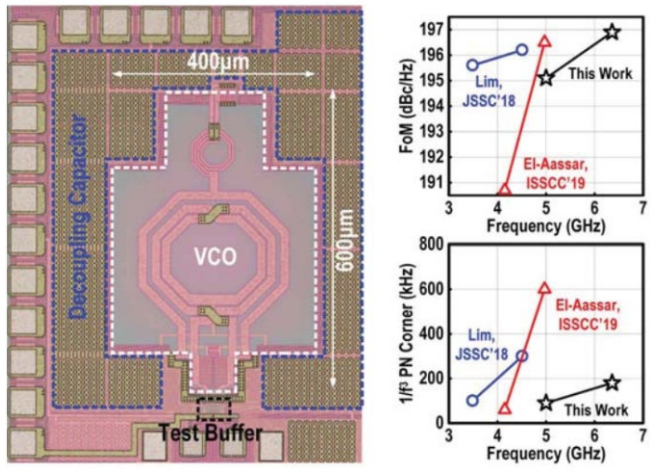


Fig. 2. Left: Die micrograph of the fabricated VCO in 65nm CMOS. Right: Plots of the FoM and 1/f³ PN corner with respect to the prior-art RF VCOs.

Publication(s)

[1] H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9 dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning," IEEE International Solid-State Circuits Conference (ISSCC), pp. 294-295, Feb. 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 36-Gb/s 1.3-mW/Gb/s Duobinary-Signal Transmitter Exploiting Power-Efficient Cross-Quadrature Clocking Multiplexers With Maximized Timing Margin

Yong Chen, Pui-In Mak, Chirn Chye Boon, and Rui P. Martins

FEATURES

Duobinary-signal transmitter

Power-efficient cross-quadrature clocking MUX

Maximized timing margin technique

Silicon verified in 65nm CMOS

DESCRIPTION

For wireline transmitters delivering a high-speed multi-level signal, such as four-level pulse-amplitude-modulation or duobinary, a high-performance multipl-exzer (MUX) is critical to serialize the low-speed parallel data into one full-speed output. To enhance the power efficiency and data eye's opening, this paper proposes a universal 2-to-1 MUX, featuring a cross-quadrature clocking technique to enlarge the timing margin, and a simplified three-latch topology without delay buffers to boost the internal bandwidth (BW). The MUX ratios are extendable to 4-to-2 and 4-to-1, and their benefits are exemplified via a duobinary-signal transmitter. It further includes an output driver unifying the MUX-and-SUM operation, a BW-extended single-to-differential converter, and an active-inductor-embedded clock buffer for swing enhancement. A predictive method for estimating the duobinary-signal data-dependent jitter according to the load capacitance of the output driver is developed.

Fabricated in 65-nm CMOS, the transmitter exhibits a figure-of-merit (FOM) of 1.3 mW/Gb/s at 36 Gb/s, while occupying a compact die area of 0.037 mm².

Benchmarking with the prior art, this work succeeds in improving the FOM and data eye opening by averting several power-hungry blocks, while operating the transmitter in the current domain to maximize the internal BW. It is possible to reduce the power consumption further by migrating this work to a more advanced process (e.g. 28-nm CMOS), resulting in lower power consumption in the clock path. Also, replacing the 2-latch+ 2-DFF array with high-speed digital circuits and employing the power-efficient divider-by-2 are prospective.

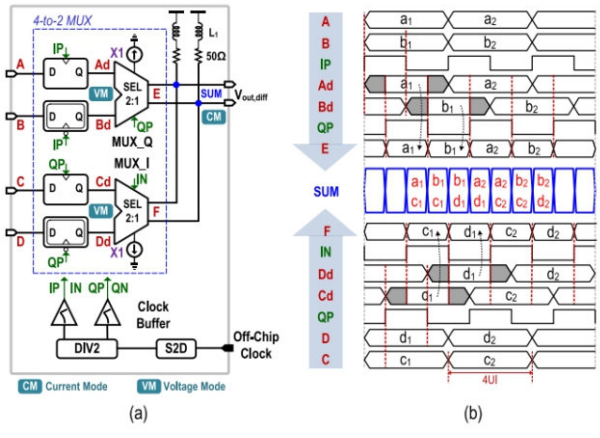


Fig. 1. (a) Top architecture of the proposed duobinary-signal transmitter. (b) Its timing diagram showing the maximum timing margin at every MUX stage.

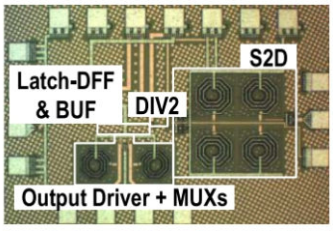


Fig. 2. Die photo of the duobinary-signal transmitter.

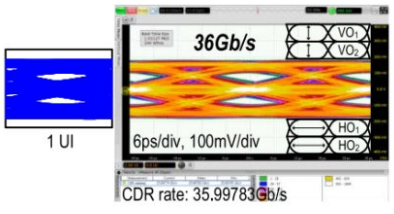


Fig. 3. Simulated (left) and measured (right) eye diagrams of the duobinary-signal transmitter at 36 Gb/s.

Publication(s)

[1] Y. Chen, P.-I. Mak, C. C. Boon, and R. P. Martins, "A 36-Gb/s 1.3-mW/Gb/s Duobinary-Signal Transmitter Exploiting Power-Efficient Cross-Quadrature Clocking Multiplexers with Maximized Timing Margin," IEEE Transactions on Circuits and Systems - I, vol. 65, pp. 3014-3026, Sept. 2018.

Sponsorship

Research Committee of University of Macau (MYRG2017-00223-AMSV).

An Area-Efficient and Tunable Bandwidth Extension Technique for a Wideband CMOS Amplifier Handling 50+ Gb/s Signaling

Yong Chen, Pui-In Mak, Haohong Yu, Chirn Chye Boon, and Rui P. Martins

FEATURES

Area-efficient and tunable BW-extension technique

High BWER with only one inductor

Wideband amplifier handling 50+Gb/s signaling

Silicon verified in 65nm CMOS

DESCRIPTION

It is an area-efficient and tunable bandwidth (BW) extension technique for a wideband CMOS amplifier to handle very high rate (50+ Gb/s) signaling. Its architectural advantages are identified by correlating the performances with the frequency domain [magnitude and group delay (GD) responses] and time domain (impulse and step responses) and comparing them with the existing solutions. Specifically, our technique enables a flexible ac characteristic by introducing a tunable grounded active inductor in the bridged-shunt peaking topology, offering: 1) a high BW enhancement ratio (BWER = 2.65×); 2) BW-power scalability with small in-band gain variation; and 3)fine tunability of the passband gain without affecting the BW, GD, and power.

The experimental prototype is a 65-nm CMOS four-stage differential amplifier occupying just 0.0077 mm2. It delivers a 15-dB gain over a 43-GHz BW with 45-mW power consumption. Small in-band gain variation (0.58 dB) and ripple (1.53 dB) are concurrently achieved with low in-band GD variation (17 to 35.3 ps) and ripple (18.3 ps). The achieved figure of merit of 5.48 [(dc Gain×BW) / Power] compares favorably with the prior art.

Benchmarking with the prior art, this work succeeds in enhancing the flexibility of the ac characteristics, while achieving a better FOM and area efficiency. This work realizes tunability by varying k_g in the current domain and k_v in the voltage domain with a little expense of in-band gain variation. In addition, differing from other works that employ more than two passive inductors along the signal path, causing more coupling and parasitics, this work extends BW by adding a GAI as an independent auxiliary path.

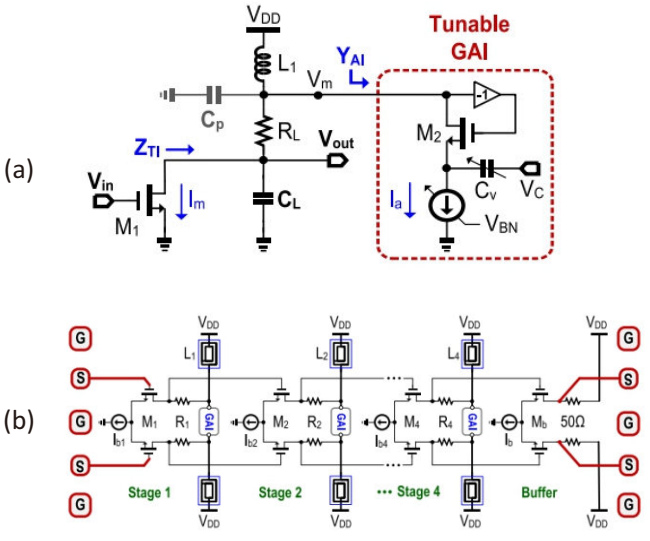
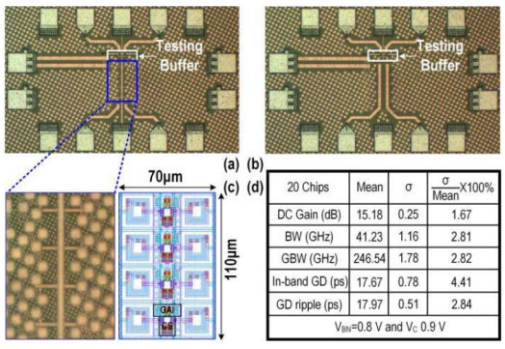


Fig. 1. (a) Simplified schematic of the proposed bridged-shunt peaking scheme with a tunable GAI. (b) Realized four-stage differential amplifier.



20 Chips	Mean	σ	$\frac{\sigma}{Mean}$X100%
DC Gain (dB)	15.18	0.25	1.67
BW (GHz)	41.23	1.16	2.81
GBW (GHz)	246.54	1.78	2.82
In-band GD (ps)	17.67	0.78	4.41
GD ripple (ps)	17.97	0.51	2.84
V_{BN}=0.8 V and V_C 0.9 V			

Fig. 2. (a) Amplifier's chip photograph. (b) Its reference path with an identical test buffer to de-embed the factual performances of the amplifier. (c) Layout details. (d) 20 chips were measured to confirm the robustness. [GBW = dc Gain × BW]

Publication(s)

[1] Y. Chen, P.-I. Mak, H. Yu, C. C. Boon, and R. P. Martins, "An Area-Efficient and Tunable Bandwidth-Extension Technique for a Wideband CMOS Amplifier Handling 50+ Gb/s Signaling," IEEE Transactions on Microwave Theory and Techniques, vol. 65, pp. 4960-4975, Dec. 2017.

Sponsorship

Research Committee of University of Macau (MYRG2017-00223-AMSV).