Wireless Transceivers

A 0.2V energy-harvesting BLE transmitter with a micropower manager achieving 25% system efficiency at 0dBm output and 5.2 nW sleep power in 28nm CMOS

J. Yin, S. Yang, H. Yi, W.-H. Yu, P.-I. Mak and R. P. Martins

FEATURES

Low supply voltage for energy harvesting, 0.2 V
High power efficiency BLE TX, 25% @ 0 dBm
Low leakage power, 5.2 nW
Low spur PLL
HD suppressed PA
Silicon verified in TSMC 28nm CMOS

DESCRIPTION

This paper reports an ultralow-voltage (ULV) energy-harvesting bluetooth low-energy (BLE) transmitter (TX). It features: 1) a fully integrated micropower manager (µPM) to customize the internal supply and bias voltages for both active and sleep modes; 2) a gate-to-source- coupling ULV voltage-controlled oscillator (VCO) using a high-ratio (5.6:1) stacking transformer to improve the phase noise and output swing; 3) an ULV class-E/F2 power amplifier (PA) with an inside-transformer LC notch to suppress the HD3, and finally 4) an analog type-I phase-locked loop (PLL) with a reduced duty cycle of its master-slave sampling filter (MSSF) to suppress the jitter and reference spur. The TX prototyped in 28-nm CMOS occupies an active area of 0.53 mm² and exhibits 25% system efficiency at 0-dBm output at a single 0.2-V supply. Without resorting from any external components, both the output HD2 (−49.6 dBm) and HD3 (−47.4 dBm) comply with the BLE standard. The FSK error is 2.84% and the frequency drift in a 425-µs data packet is <5 kHz under open-loop modulation. The use of negative-voltage power gating suppresses the sleep power of the entire TX to 5.2 nW.

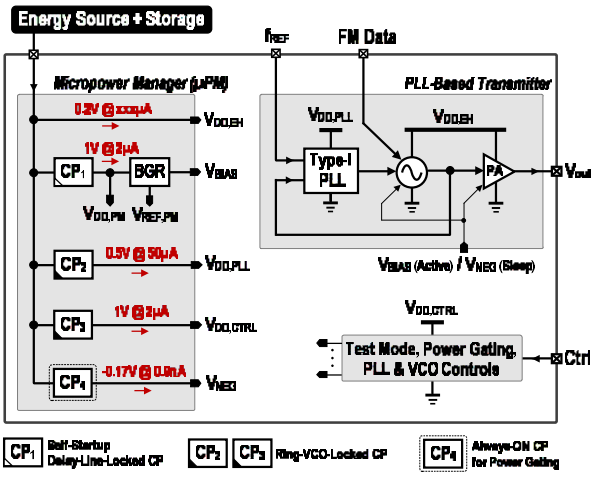

Fig. 1. Proposed energy-harvesting BLE TX with a fully integrated µPM to generate the internal supply and bias voltages that are insensitive to the voltage variation of the energy-harvester output (VDD,EH) down to 0.2 V.

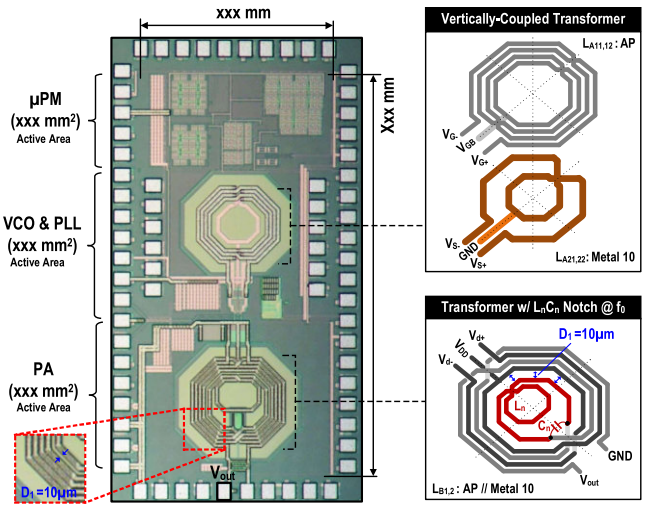

Fig. 2. Chip micrograph.

Publication(s)

[1] Jun Yin, Siheng Yang, Haidong Yi, Wei-Han Yu, Pui-In Mak, Rui Martins, “A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS,” IEEE International Solid-State Circuits Conference (ISSCC), Digest., pp. 450-451, Feb. 2018.

[2] Shiheng Yang, Jun Yin, Haidong Yi, Wei-Han Yu, Pui-In Mak, and Rui P. Martins, “A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS,” IEEE Journal of Solid-State Circuits, vol.54, pp. 1351-1362, May. 2019.

Sponsorship

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A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS

Wei-Han Yu, Haidong Yi, Pui-In Mak, Jun Yin, R. P. Martins

FEATURES

Low supply voltage for energy harvesting, 0.18 V
Ultra-low power BLE RX, 382 µW
Low leakage power, 1.3 nW
Fast start-up µPM
Power-gating LNA
Silicon verified in TSMC 28nm CMOS

DESCRIPTION

We propose an ultra-low-voltage Bluetooth low-energy (BLE) receiver (RX) front end with an on-chip micropower manager (µPM) to customize the internal voltage domains. It aims at direct powering by the sub-0.5-V energy harvesting sources like the on-body thermoelectric, eliminating the loss and cost of the interim dc–dc converters. Specifically, the RX incorporates: 1) a two-stage power-gating low-noise amplifier with fully on-chip input-impedance matching and passive gain boosting reducing both the active and sleep power; 2) a class-D voltage-controlled oscillator (VCO) in parallel with a class-C starter to secure a fast startup; and 3) a µPM using ring VCO-locked charge pumps and bandgap references to withstand the supply-voltage variation (0.18–0.3 V). Fabricated in 28-nm CMOS, the RX operates down to a 0.18-V supply, while exhibiting 11.3-dB NF and −12.5-dBm out-of-band IIP3. The VCO shows < −113 dBc/Hz phase noise at 2.5-MHz offset. The active and sleep power are 382 µW and 1.33 nW, respectively.

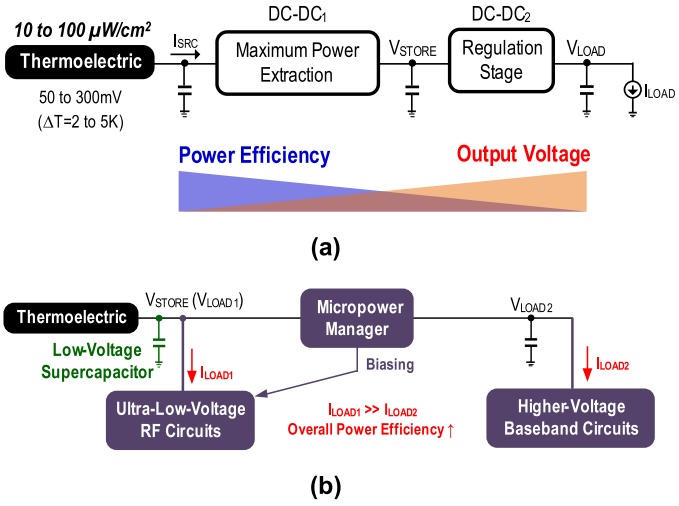


Fig. 1. (a) Conventional energy-harvesting topology. and (b) Codesign between our proposed energy-harvesting topology and ULV RF circuits, where a µPMcan provide the critical biases and support the standard voltage BB circuits.

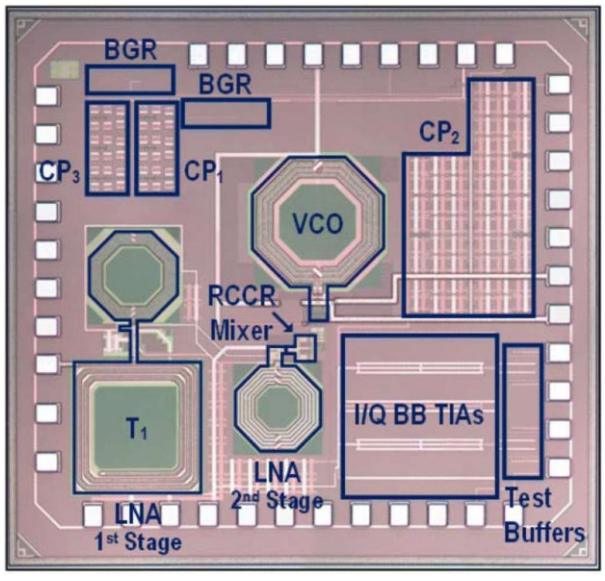


Fig. 2. Chip micrograph.

Publication(s)

[1] Wei-Han Yu, Haidong Yi, Pui-In Mak, Jun Yin, R. P. Martins, “A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS,” IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 414-415, Feb. 2017.

[2] Haidong Yi, Wei-Han Yu, Pui-In Mak, Jun Yin and R. P. Martins, “A 0.18-V 382-µW Bluetooth Low-Energy (BLE) Receiver with 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 53, pp. 1618-1627, Aug. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) P_{out}

Xingqiang Peng, Jun Yin, Pui-In Mak, Wei-Han Yu and R. P. Martins

FEATURES

Function-Reuse Class DCO-PA
High power efficiency ZigBee TX, 22.6% @ 6 dBm
Scalable supply voltage, 0.3-0.7 V
Low distortion, 2.29% EVM.
Compact area, 0.39 mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper describes a sub-1-V 2.4-GHz ZigBee transmitter (TX) with scalable output power (P_{out}) and system efficiency. It features a function-reuse class-F topology unifying the digital-controlled oscillator (DCO) and power amplifier (PA), designated as DCO-PA. Unlike the existing current reuse topologies that rely on transistor stacking, here the power consumption of the DCO and PA-driver is absorbed into the DCO-PA without losing the voltage headroom, while allowing a low supply voltage. The DCO-PA also benefits from a six-port transformer with customized coupling coefficients and turn ratios to jointly perform the functions of resonant tank and output matching network, saving the chip area. A fractional-N all-digital phase-locked loop (ADPLL) realizes a two-point data modulation. Its phase-interpolated time-to-digital converter prevents time-consuming calibration. The entire TX fabricated in 65-nm CMOS occupies a 0.39-mm² active area. The standalone DCO-PA shows a peak efficiency of 26.2% at a 6-dBm P_{out}, and a back-off efficiency of 17.7% at a −4.3 dBm P_{out} under a scalable supply voltage (0.3–0.7 V). The system efficiency, including the ADPLL, is 22.6% (14.5%) at 6-dBm (0-dBm) P_{out}. The HS-OQPSK modulated output complies with the ZigBee spectral mask with an adequate margin and the error vector magnitude is 2.29%.

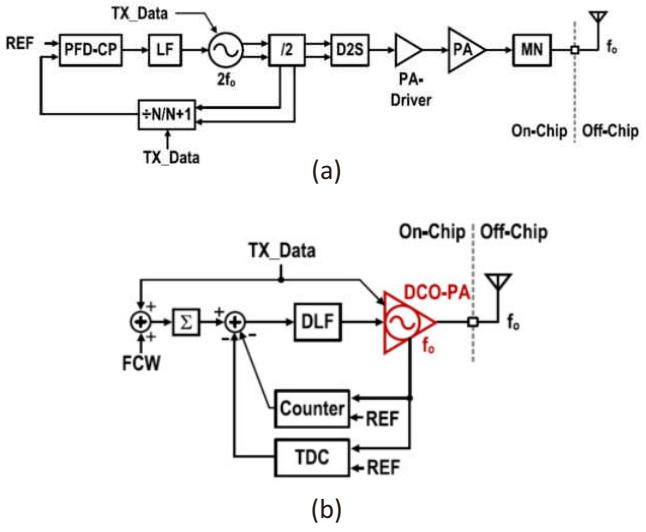


Fig. 1. ULP TXs using (a) conventional separated VCO and PA, and (b) proposed function re-use DCO-PA.

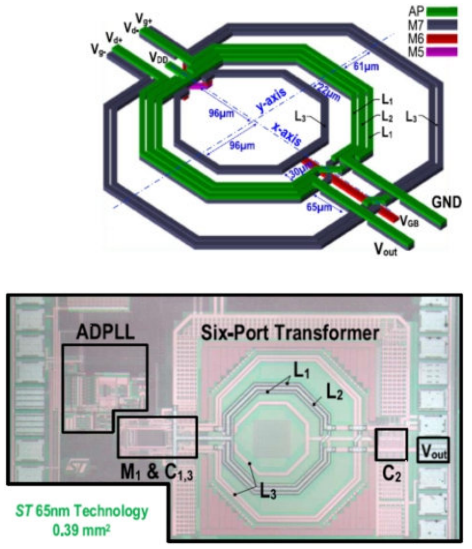


Fig. 2. Chip micrograph.

Publication(s)

[1] Xingqiang Peng, Jun Yin, Pui-In Mak, Wei-Han Yu and R. P. Martins, "A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) P_{out}," IEEE Journal of Solid-State Circuits, vol. 52, pp. 1495- 1508, Jun. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 0.0056-mm² -249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs

Shiheng Yang, Jun Yin, Pui-In Mak, and Rui P. Martins

FEATURES

A low-power block-sharing offset-free frequency-tracking loop (FTL) to calibrate the PVT variations of the voltage-controlled oscillator (VCO) frequency

Varactor-tuned dual multiplexed-ring VCOs to reduce jitter variation while extending the frequency tuning range.

Silicon verified in GF 28 nm CMOS

A state-of-the-art Jitter-FoM of −249 dBc/Hz at 3 GHz

DESCRIPTION

This work proposes an ultra-compact all-digital multiplying delay-locked loop (MDLL) featuring a low-power block-sharing offset-free FTL to calibrate the PVT variations of the VCO frequency. Such FTL utilizes a digital-controlled delay line (DCDL)-based low-power time-interval comparator and an adjacent-edge selector, to precisely detect the static phase offset (SPO) caused by the VCO frequency drifting in the presence of reference injection. The block-sharing-based SPO detection aids in nullifying the circuit-mismatch- and offset-induced deterministic error. Also, for the adjacent edge selector, block sharing between its control generation circuits and the coarse FTL further reduces the power consumption. The varactor-tuned dual multiplexed-ring VCOs (MRVCOs) serve to reduce jitter variation while extending the frequency tuning range.

Prototyped in a 28-nm CMOS with a core area of 0.0056 mm², the proposed MDLL covers a tuning range from 1.55 to 3.35 GHz, and exhibits a root-mean-square (rms) jitter of 292 fs at the 3-GHz output, under a 200-MHZ reference clock. The power consumption is 1.45 mW at a 0.8-V supply, resulting in an FoM of −249 dB favorably comparable with state-of-the-art.

Benchmarking with the recent ring-VCO-based MDLLs and ILCMs, this work shows improved area efficiency of >4.2× and FoM referring to the reference frequency (FoMr) of >2dB. Moreover, the FTL's power consumption of 0.3mW is the lowest reported.

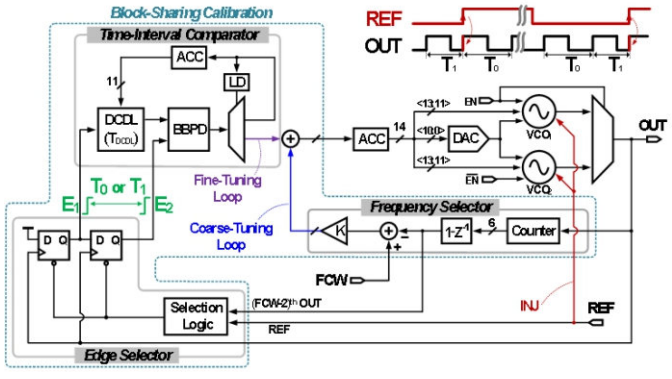
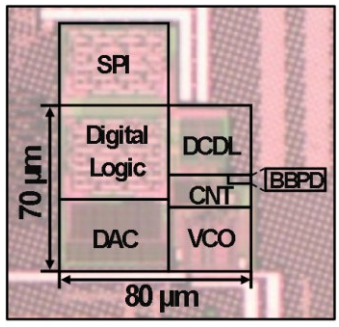


Fig. 1. Proposed all-digital MDLL architecture.



(a)

Power Consumption (mW)	
Digital Logic	0.2
AES and TIC*&	0.04
Counter	0.02
DAC	0.03
VCO	1.16
Total	1.45

* AES: Adjacent Channel Selector, TIC: Time-Interval Comparator.
& Power of comparison logic in AES is included in the digital logic.

(b)

Fig. 2. (a) Chip micrograph and (b) area breakdown.

Publication(s)

[1] S. Yang, J. Yin, P. -I. Mak, and R. P. Martins, "A 0.0056-mm² -249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs," IEEE Journal of Solid-State Circuits, pp. 89-98, vol. 54, Jan. 2019.

[2] S. Yang, J. Yin, P. -I. Mak, and R. P. Martins, "A 0.0056mm² All-Digital MDLL Using Edge Re-extraction, Dual Ring-VCOs and a 0.3mW Block-Sharing Frequency-Tracking Loop Achieving 292fs$_{rms}$ Jitter and -249dB FoM," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 118-119, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of the University of Macau.

A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA

Chao Fan, Jun Yin, Chee-Cheow Lim, Pui-In Mak, and Rui P. Martins

FEATURES

A 60GHz current-reuse LO generator (LOG) employing current-mode implicit frequency tripling

Achieve large output swing, low phase noise, and low subharmonic spurs simultaneously

Silicon verified in TSMC 65 nm CMOS

A state-of-the-art peak FoM of 186.7 dBc/Hz

DESCRIPTION

This work proposes a 60GHz current-reuse LOG featuring current-mode implicit frequency tripling. It includes : 1) a current-output VCO to generate a large 3rd-harmonic current with low phase noise; 2) an area-efficient passive harmonic-current filter (HCF) using the S-shape inductors to reject the 1st- and 2nd-harmonic leakage currents at f_{LO} and $2f_{LO}$; and 3) a current-reuse transimpedance amplifier(TIA) stacked atop the VCO and HCF to recover a large output swing with low power.

Prototyped in 65nm CMOS, the proposed LOG exhibits a high FoM of 184.9 to 186.7dBc/Hz at a 1MHz offset over a frequency tuning range from 54.9 to 63.5GHz (14.5%). The measured subharmonic spurs are <−61dBc.

Benchmarking with the prior art, our LOG exhibits a best-in-class FoM@1MHz and low 1st- and 2nd- harmonic spurs. Specifically, comparing with the voltage-mode implicit frequency tripling technique that entails a buffer stage to boost the 3rd-harmonic voltage while suppressing the large fundamental voltage at the class-F VCO output, our design consumes less power and shows improved FoM@1MHz by >5.2dB, and subharmonic spurs by 10dB.

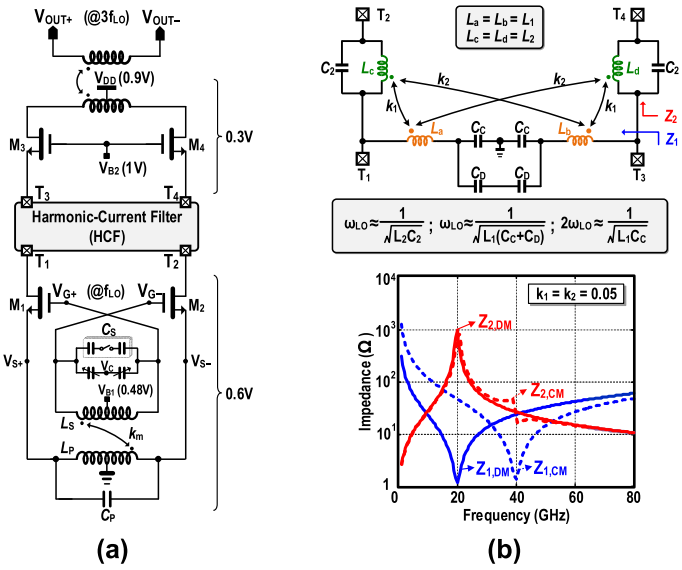


Fig. 1. (a) Proposed 60-GHz LOG using current-mode implicit frequency tripling technique and (b) passive harmonic-current filter.

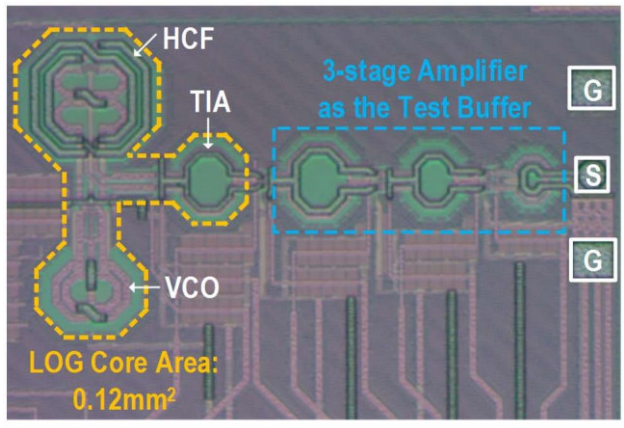


Fig. 2. Chip micrograph.

Publication(s)

[1] C. Fan, J. Yin, C. -C. Lim, P. -I. Mak, and R. P. Martins, "A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 282-283, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Push-Pull LNA

Kai Xu, Jun Yin, Pui-In Mak, Robert Bogdan Staszewski, and Rui P. Martins

FEATURES

A function-reuse single-MOS digitally controlled oscillator power amplifier (DCO-PA) improves antenna-to-DCO isolation

A noninverting transmitter matching transformer with a zero-shifting capacitor to suppress the 2nd-harmonic emission of the DCO-PA

A push-pull low-noise amplifier (LNA) reuses the transmitter matching transformer for passive gain boosting

Silicon verified in TSMC 65 nm CMOS

DESCRIPTION

This work proposes a simple power-efficient sub-1-V fully integrated RF front end for 2.4-GHz transceivers. It introduces the following innovations. First, a function-reuse single-MOS DCO-PA with full supply utilization improves antenna-to-DCO isolation for better resilience to jammers. Second, a noninverting transmitter (TX) matching transformer with a zero-shifting capacitor suppresses the second-harmonic emission of the DCO-PA and allows a single-pin antenna interface for both TX and receiver (RX) modes eliminating the transmit/receive (T/R) switches in the signal path. Third, a push-pull low-noise amplifier (LNA) reuses the TX matching transformer for passive gain boosting that reduces power consumption.

Prototyped in 65-nm CMOS, the RF front end occupies merely 0.17 mm². Through the functional merge of the oscillator and PA, it can transmit 0 dBm at RF, featuring 10.2% power efficiency when delivering the RF power as low as −10 dBm at a 0.3-V supply. Under a 0.5-V supply, the LNA shows 11-dB gain and 6.8-dB noise figure while consuming 174 µW.

To the best of our knowledge, the presented single-MOS DCO-PA architecture is the first fully integrated single-ended solution with competitive carrier phase noise and power efficiency, especially at low power modes while simultaneously handling the harmonic emissions and easy switching to the RX LNA.

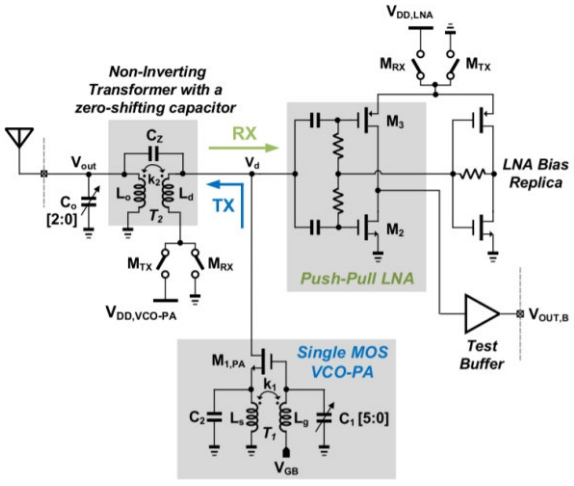


Fig. 1. Schematic of the proposed single-pin antenna interface RF Front End.

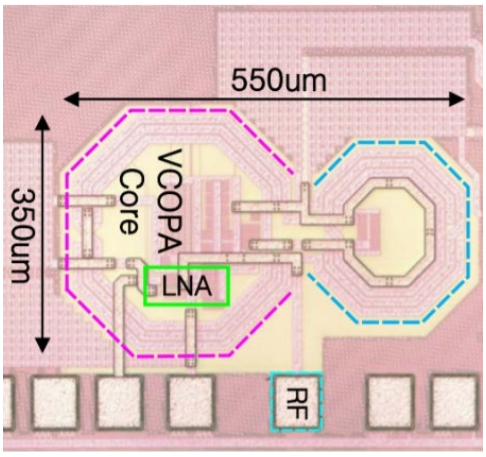


Fig. 2. Chip micrograph.

Publication(s)

[1] K. Xu, J. Yin, P. -I. Mak, R. B. Staszewski, and R. P. Martins, "A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Push-Pull LNA," IEEE Journal of Solid-State Circuits, pp. 2055-2068, vol. 55, Aug. 2020.

[2] K. Xu, J. Yin, P. -I. Mak, R. B. Staszewski, and R. P. Martins, "A 2.4-GHz Single-Pin Antenna Interface RF Front-End with a Function-Reuse Single-MOS VCO-PA and a Push-Pull LNA," IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 293-294, Nov. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

An Inverse-Class-F CMOS Oscillator with Intrinsic-High-Q 1st -Harmonic and 2nd -Harmonic Resonances

Chee Cheow Lim, Harikrishnan Ramiah, Jun Yin, Pui-In Mak, and Rui P. Martins

FEATURES

A single-ended PMOS-NMOS-complementary architecture to generate the differential outputs

A transformer tank generates two intrinsic-high-Q resonances at the fundamental frequency F_{LO} and the 2nd-harmonic frequency $2F_{LO}$

Silicon verified in TSMC 65 nm CMOS

A state-of-the-art FoM of 196.1 dBc/Hz at 4 GHz

DESCRIPTION

This work proposes an inverse-class-F (class-F^{-1}) CMOS oscillator. It features: 1) a single-ended PMOS-NMOS-complementary architecture to generate the differential outputs, and 2) a transformer-based 2-port resonator to boost the drain-to-gate voltage gain (A_V) while creating two intrinsic-high-Q impedance peaks at the fundamental (f_{LO}) and double ($2f_{LO}$) oscillation frequencies. The enlarged 2nd-harmonic voltage extends the flat span in which the Impulse Sensitivity Function (ISF) is minimum, and the amplified gate voltage swing reduces the current commutation time, thereby lowering the $-g_m$ transistor's noise-to-phase noise (PN) conversion.

Prototyped in 65-nm CMOS, the class-F^{-1} oscillator at 4 GHz exhibits a PN of –144.8 dBc/Hz at 10 MHz offset while offering a tuning range of 3.5 to 4.5 GHz. The corresponding figure-of-merit (FoM) is 196.1 dBc/Hz, and the die area is 0.14 mm².

Benchmarking with the prior art, our class-F^{-1} CMOS VCO exhibits the highest FOMs at both 100kHz and 10MHz offsets over a comparable tuning range while achieving low frequency pushing.

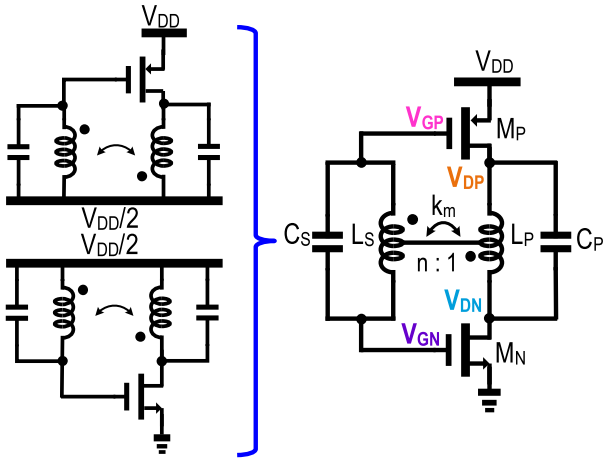


Fig. 1. Class-F-1 oscillator with a PMOS-NMOS-complementary topology to generate the differential outputs.

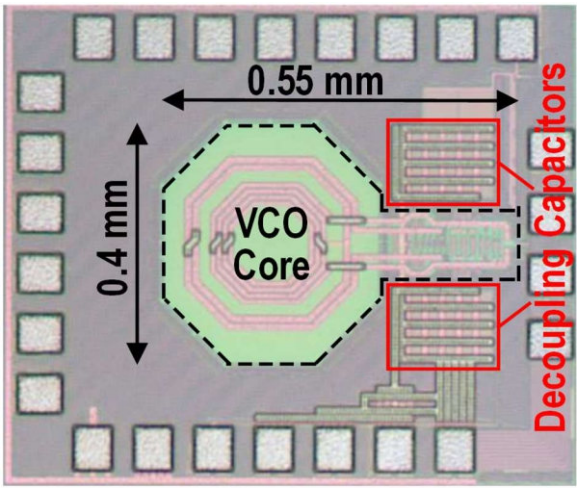


Fig. 2. Chip micrograph.

Publication(s)

[1] C. -C. Lim, H. Ramiah, J. Yin, P. -I. Mak, and R. P. Martins, "An Inverse-Class-F CMOS Oscillator with Intrinsic-High-Q First Harmonic and Second Harmonic Resonances," IEEE Journal of Solid-State Circuits, pp. 3528-3593, vol. 53, Dec. 2018.

[2] C. -C. Lim, J. Yin, P. -I. Mak, H. Ramiah, and R. P. Martins, "An Inverse-Class-F CMOS VCO with Intrinsic-High-Q 1st– and 2nd-Harmonic Resonances for $1/f^2$-to-$1/f^3$ Phase Noise Suppression Achieving 196.2dBc/Hz FoM," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 374-375, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of the University of Macau.

Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools

Ricardo Martins, Nuno Lourenço, Nuno Horta, Shenke Zhong, Jun Yin, Pui-In Mak and Rui P. Martins

FEATURES

A complementary class-B/C hybrid-mode voltage-controlled oscillator (VCO) topology to minimize the power consumption at a standard high supply voltage

A two-step electronic-design-automation-assisted (EDA-assisted) flow to optimize device parameters and generate the layout automatically

Silicon verified in TSMC 65 nm CMOS

Measurement results confirm the effectiveness of the EDA-assisted flow

DESCRIPTION

Optimal VCO design for ultralow-power (ULP) radios has to fulfill simultaneously multiple requirements such as frequency tuning range, phase noise, power consumption, and frequency pushing. The manual design struggles to approach the full potential that a given topology can achieve. This work proves the role of EDA tools by fully supporting the complex design of a ULP complementary Class-B/C hybrid-mode VCO. In the 1st step of the EDA-assisted flow, we perform a worst-case corner of worst-case tuning sizing optimization over a 108-dimensional performance space, offering sizing solutions with power consumption down to 145 µW at the worst-case. In the 2nd step, we introduce an automatic layout generation tool to offer valuable insights into the post-layout design space and devise a ready-for-tape-out fine optimization strategy.

The hybrid-mode VCO designed by the two-step EDA-assisted flow is prototyped in 65-nm CMOS. It occupies a die area of 0.165 mm² and dissipates 297 µW from a 0.8 V supply at 5.1 GHz. The phase noise at 1MHz offset is −110.1dBc/Hz, resulting in a competitive Figure-of-Merit (FoM) of 189.4 dBc/Hz, well-suited for ULP applications.

(a)

(b)

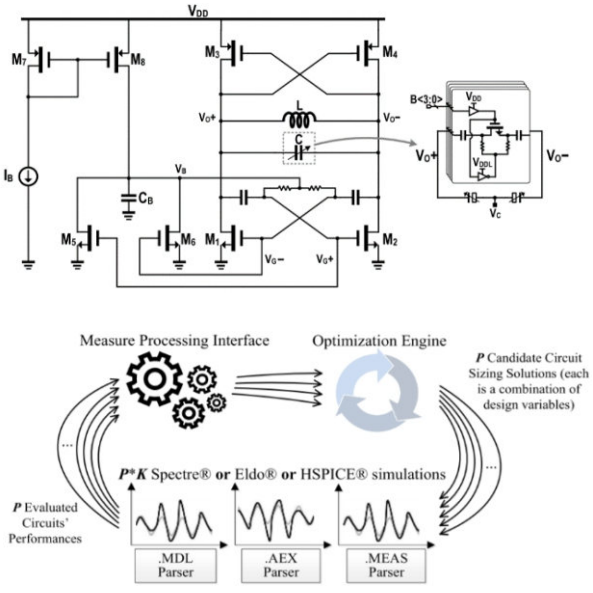
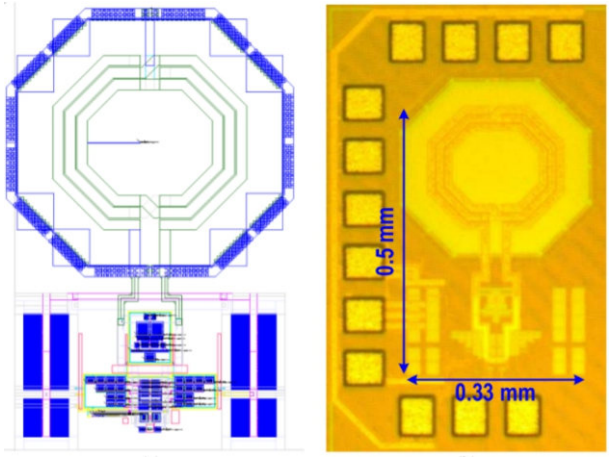


Fig. 1. (a) Complementary class-B/C hybrid-mode VCO topology and (b) flow of multi-test bench analog and RF IC sizing optimization.



(a) (b)

Fig. 2. (a) Automatically generated layout outputted by the EDA tool and (b) chip micrograph.

Publication(s)

[1] R. Martins, N. Lourenço, N. Horta, S. Zhong, J. Yin, P. -I. Mak and R. P. Martins, "Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools," IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), pp. 3965-3977, vol. 67, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

A 0.7-to-2.5 GHz, 61% EIRP System Efficiency, 4-Element MIMO TX Exploiting Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver

Wei-Han Yu, Ka-Fai Un, Pui-In Mak and Rui P. Martins

FEATURES

- Wideband MIMO transmitter (0.7 to 2.5 GHz)
- High EIRP System Efficiency, 61%
- High EIRP average power, 19.2 dBm
- No matching network to avoid power loss
- Analog spatial de-interleaver for 4-channel baseband
- Silicon verified in 65 nm CMOS

DESCRIPTION

It is a 4-element MIMO transmitter (TX) system that features an analog spatial de-interleaver to simplify the baseband-input complexity and increase the spatial matching of the sub-TXs. The MIMO diversity gain and power-combining gain are jointly exploited to relax the output power of the power amplifiers while eliminating their output matching networks, leading to a compact implementation of the entire TX system. The MIMO effectiveness is improved by introducing an RF to baseband DC feedback technique that enhances the matching among the sub-TXs against process variation.

In the verification, the TX system is co-designed with a compact antenna array-on-PCB that generates a null zone in the propagation pattern, and the electric-field polarization angle, to achieve diversity propa-gation. All techniques together improve the signal-to-noise ratio and/or the data rate by generating multiple data streams according to the signal power arriving at the receiver over different fading channels.

Prototyped in 65-nm CMOS, the MIMO TX chip occupies 1.44 mm². It covers an RF range of 0.7–2.5 GHz, and shows an equivalent isotropically radiated power of 23.9 dBm. When transmitting a 20-MHz 64-QAM orthogonal frequency division multiplexing signal at 2.3 GHz, the average system efficiency is 61% and error-vector magnitude is −26 dB.

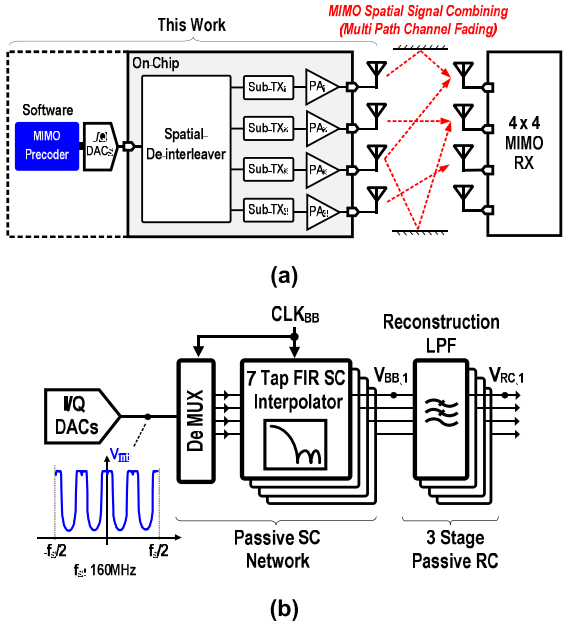


Fig. 1. (a) MIMO TX architecture and (b) analog spatial de-interleaver.

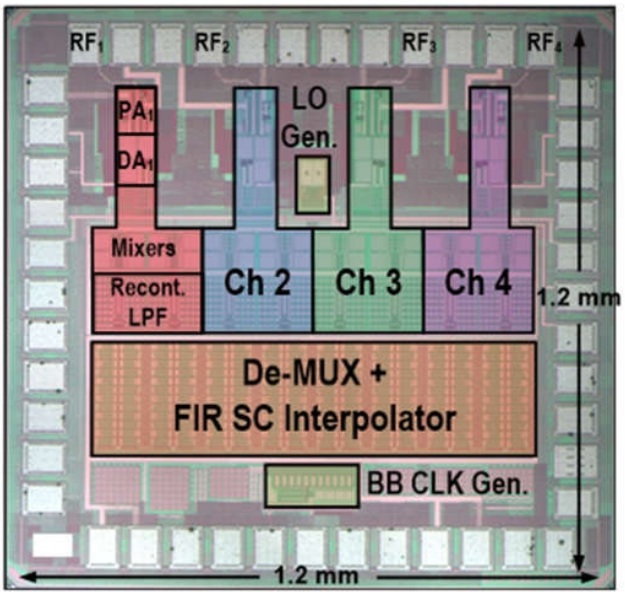


Fig. 2. Chip micrograph.

Publication(s)

[1] W. Yu, K. Un, P. Mak and R. P. Martins, "A 0.7–2.5 GHz, 61% EIRP System Efficiency, Four-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 14-25, Jan. 2018.

Sponsorship

Macao Science and Technology Development Fund SKL Fund and the University of Macau.

A 0.12-mm² 1.2-to-2.4 mW 1.3-to-2.65 GHz Fractional-N Bang-Bang Digital PLL with 8-µs Settling Time for Multi-ISM-Band ULP Radios

Ka-Fai Un, Gengzhen Qi, Jun Yin, Shiheng Yang, IEEE, Shupeng Yu, Chio-In Ieong, Pui-In Mak and Rui P. Martins

FEATURES

Wide frequency range DPLL (1.3 to 2.65 GHz)

Low power consumption, 1.2 to 2.4 mW

Fast settling time, 8 µs

Mismatch-free DTC gain calibration

Split coarse-fine PLL loops with different bandwidth

Silicon verified in 65 nm CMOS

DESCRIPTION

It is a wideband fractional-N bang-bang DPLL for multi-ISM-band ULP radios. To improve the settling time, we proposed two techniques: 1) a mismatch-free DTC gain calibration scheme and 2) split coarse-fine PLL loops. They, together,allow fast startupsettling and channel switching. The employed ring VCO (RVCO) aids to extend the frequency tuning range and generate multi-phase outputs.

Prototyped in 65-nm CMOS, the DPLL consumes 1.2 to 2.4 mW over a wide frequency locking range of 68.3% (1.3 to 2.65 GHz) and occupies a die area of 0.12 mm². The settling time measures 8 µs at an 82-MHz initial frequency error.

Benchmarking with other state-of-the-art fractional PLLs, this work significantly reduces the convergence time of the DTC gain calibration loop, with a settling time that is even faster than an ADPLL only using a TDC.

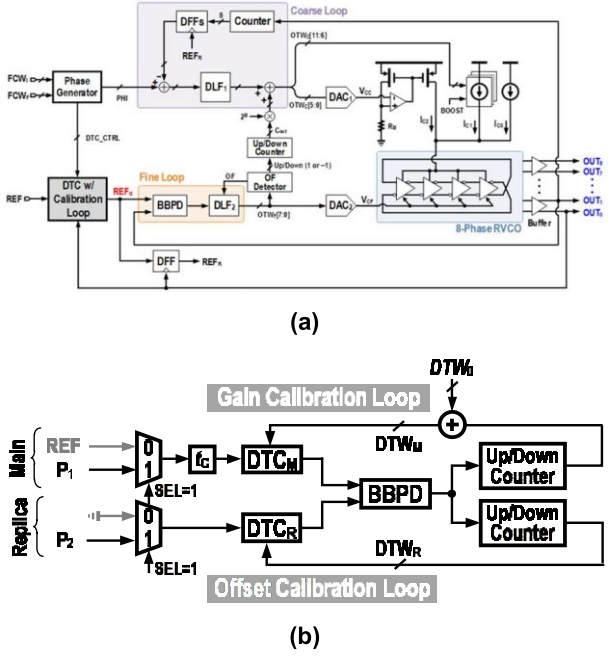


Fig. 1. (a) Digital PLL (RFE) architecture and (b) calibration loop for DTC.

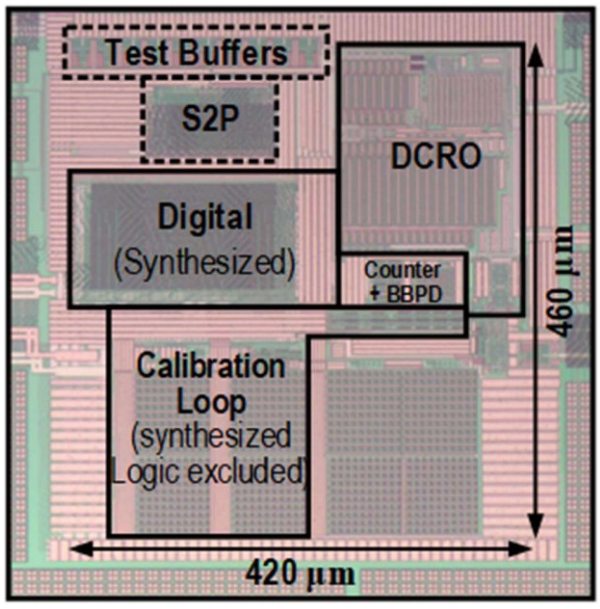


Fig. 2. Chip micrograph.

Publication(s)

[1] K.-F. Un, G. Qi, J. Yin, S. Yang, S. Yu, C.-I. Ieong, P.-I. Mak, and R. P. Martins, "A 0.12-mm² 1.2-to-2.4-mW 1.3-to-2.65-GHz Fractional-N Bang-Bang Digital PLL With 8-µs Settling Time for Multi-ISM-Band ULP Radios," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 9, pp. 3307-3316, Sept. 2019.

Sponsorship

Macao Science and Technology Development Fund SKL Fund and the University of Macau.

Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection

Ka-Fai Un, Feifei Zhang, Pui-In Mak, Rui P. Martins, Anding Zhu and Robert Bogdan Staszewski

FEATURES

Analytical study of interpolative digital transmitter

Procedures for determining sampling rate, resolution, linear interpolation ratio

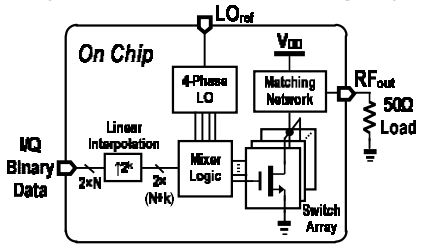
Fulfilling replica rejection and noise floor for different specifications with relaxed high speed digital interface

Improved replica rejection by interpolation, 23 dB

Improved noise floor by interpolation, 2.2 bits

DESCRIPTION

The digital transmitter (DTX) offers both high power efficiency and frequency flexibility by merging signal amplification and modulation in the switching power amplifier. Yet, the back-end high-speed digital baseband interface is challenging and bulky for obtaining low out-of-band noise. This work provides an analytical study of the DTX linear interpolation technique, which can be easily utilized for optimizing the replica rejection and noise-filtering capabilities of the DTX.



(a)

$$H_{2^k}(jf) = \frac{1}{\pi T_s f}\sin(\pi T_s f)\prod_{n=1}^{k}\cos\left(\frac{\pi T_s f}{2^n}\right)$$

Linear Interpolation Rate	1×	2×	4×	8×	16×
Required OSR	50	25	12.5	6.25	5.4
Dominant Replica	1st	2nd	4th	8th	1st

(b)

Fig. 1. (a) Interpolative digital transmitter architecture, and (b) frequency response of the 2^k-step linear interpolator and the dominated replicas.

An IEEE 802.11g orthogonal frequency division multiplexing (OFDM) signal has been generated to verify the derived results, with the sampling frequency chosen to be 120 MHZ. The first replica is suppressed to –24.4/–47.2 dBc without/with interpolation, respectively. The noise floor of 2×11-bit ENOB is –159 dBc/Hz at 95 MHz offset without interpolation while the noise floor of 9-bit ENOB is –160 dBc/Hz at 96 MHz offset with 8× interpolation.

The linear interpolation technique not only can suppress the replicas of the sampling in an RF DTX, but also can lower the quantization noise floor level. The results are supported by quantitative examples by concerning the practical hardware limits at RF. It is revealed that linear interpolation can aid effectively sampling-frequency reduction without sacrificing the replica rejection. It can also relax the resolution of the baseband signal for smaller I/O pin count.

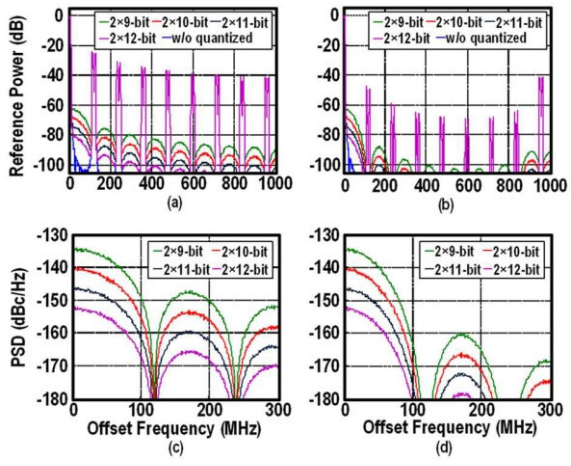


Fig. 2. Replica and noise spectrum without (left)/ with (right) linear interpolation.

Publication(s)

[1] K.-F. Un, F. Zhang, P.-I. Mak, R. P. Martins, A. Zhu and R. B. Staszewski, "Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, pp. 37-41, Jan. 2020.

Sponsorship

Macao Science and Technology Development Fund SKL Fund and the University of Macau and Microelectronic Circuits Centre Ireland (MCCI), Cork, Ireland.

A 0.038mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop

Gengzhen Qi, Pui-In Mak and Rui P. Martins

FEATURES

SAW-less Multiband Transceiver (TXR)

Small area, 0.038mm²

Using N-Path Switched-Capacitor (SC) Gain Loop as a reconfigurable transmitter (TX) and receiver (RX)

Utilizing Switched-BB-extraction technique in RX mode

Utilizing High-efficiency PA driver (PAD) in TX mode

Fabricated in 65nm CMOS technology

DESCRIPTION

It is a SAW-less compact multiband transceiver (TXR) for LTE standard by employing a switched-capacitor (SC)-Gain Loop that is a negative-gain stage with an SC network as its feedback. Any signals, radio frequency (RF) or baseband (BB), properly injected into the loop will undergo gain, down-mix and up-mix; all are primary functions of transmitter (TX) or receiver (RX). Thus, the SC-gain loop can operate as a basic TX by injecting the BB signal while extracting the RF signal, or a basic RX by injecting the RF signal while extracting the BB signal. This duality suggests the possibility of using the SC-gain loop as a reconfigurable TXR (Fig. 1) appropriate for LTE-TDD. Elegantly, the extra downmix path in the TX and upmix path in the RX allow the SC-gain loop to effectively combine with the gain-boosted N-path technique to realize LO-defined high-Q bandpass (de)modulation.

The TXR fabricated in 65nm CMOS has a die area of 0.038mm² (Fig. 2). For TX mode, the output power shows -1dBm at 1.88GHz (Band2) with -40dBc $ACLR_1$ and 2.0% EVM. The output noise floor is -154.5dBc/Hz at 80MHz offset The TX-mode consumes 31.3mW (Band5) to 38.4mW (Band2). For RX mode, the S_{11} is <–12dB. The NF ranges from 2.2 to 3.2dB. The RF BW reaches to 10MHz. The achieved OB-P_{1dB} (-5dBm) and OB-IIP_3 (+8dBm) are both competitive at 80MHz offset.

Benchmarking with the prior art, the transmitter succeeds in improving the multiband flexibility and area efficiency that is 24x better than the state-of-the-art, while preserving a comparable power efficiency (2.1% for Band2 and 2.4% for Band5); while the receiver succeeds in achieving comparable power consumption, NF and OB-IIP_3.

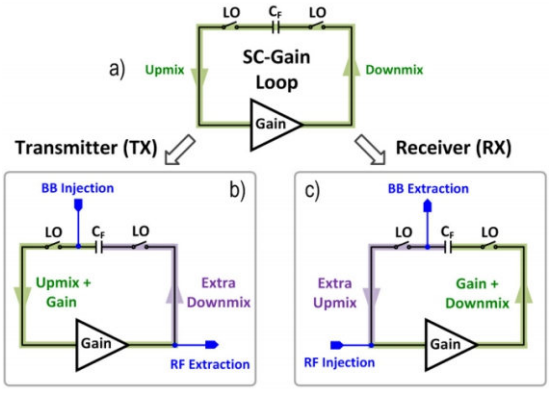


Fig. 1. (a) Switched-capacitor (SC)-Gain Loop. It can operate as a (b) TX under BB-injection RF-extraction, or (c) RX under RF-injection BB-extraction.

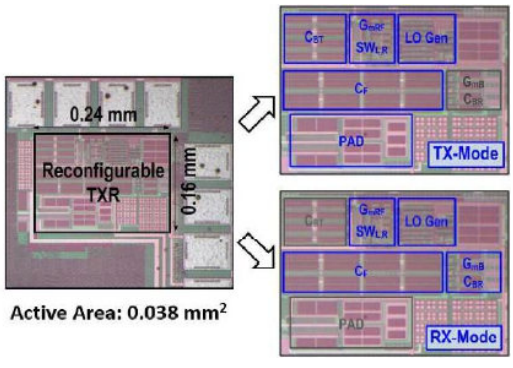


Fig. 2. Chip micrograph.

Publication(s)

[1] G. Qi, P.-I. Mak and R. P. Martins, "A 0.038mm2 SAW-less multi-band transceiver using an N-path SC gain loop," in IEEE Journal of Solid-State Circuits, vol. 52, no. 8, pp. 2055-2070, Aug. 2017.

[2] G. Qi, P.-I. Mak and R. P. Martins, "A 0.038mm² SAW-less multi-band transceiver using an N-path SC gain loop," in IEEE ISSCC Dig. Tech. Papers, Feb. 2016, pp. 452-453.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Multiband FDD SAW-less Transmitter for 5G-NR Featuring a BW-Extended N-Path Filter-Modulator, a Switched-BB Input and a Wideband TIA-Based PA Driver

Gengzhen Qi, Haijun Shao, Pui-In Mak, Jun Yin and Rui P. Martins

FEATURES

Covering 5G-NR FDD bands (1.4 to 2.7GHz)
Low output noise, ≤−157.5dBc/Hz
High transmitter (TX) efficiency, 2.8%–3.6%
Bandwidth-extended N-path filter-modulator
Switched-baseband (BB) input network
TIA-based power amplifier driver (PAD)
Fabricated in 28-nm CMOS technology

DESCRIPTION

An SAW-less transmitter (TX) supporting a 20-MHz BW is proposed in Fig. 1. It aims to cover the 5G-NR FDD bands in the 1.4-to-2.7-GHz range. To balance the performance metrics: channel BW, output noise at small Δf, multiband flexibility, and integration level, three key innovations are featured: 1) a BW-extended N-path filter modulator (BW-Ext FIL-MOD)—it embeds a high-order gain-boosted N-path filter into the I/Q modulator and leads to BW extension and steeper OB filtering; 2) a switched-BB input network—it avoids the mutual loading effect between the BW-Ext FIL-MOD and input network, to uphold a high-Q filtering profile at RF and to reduce the nonlinearity and crosstalk at BB; and 3) a trans-impedance amplifier (TIA)-based PAD—it absorbs the bias and signal currents of the BW-Ext FIL-MOD for better linearity and power efficiency. It also features an inner-parallel Gm linearizer to suppress its third-order cross-intermodulation product (CIM_3).

Fabricated in 28-nm CMOS technology (Fig. 2), the proposed TX manifests a 20-MHz passband BW and a consistently low OB noise (≤−157.5dBc/Hz) for different 5G-NR bands between 1.4 and 2.7GHz. The TX achieves sufficient output power (+3dBm), high TX efficiency (2.8%–3.6%), and high linearity ($ACLR_1$ <-44dBc and EVM <2%). The active area is 0.31mm².

Benchmarking with the prior art, this work manifests several performance advantages, namely, the linearity, OB noise and TX efficiency thanks to the effective BW-Ext FIL-MOD, switched-BB input network and wideband TIA-based PAD.

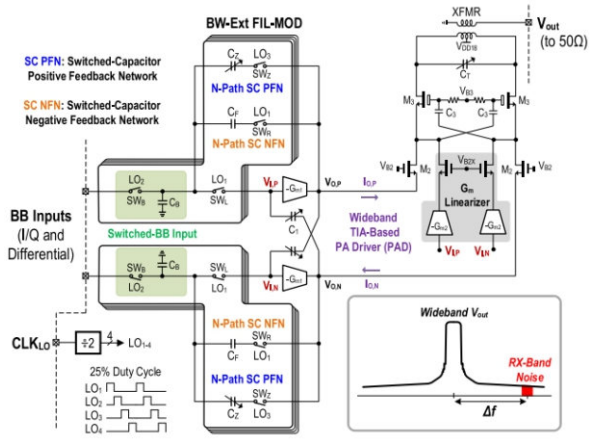


Fig. 1. The fully integrated multiband transmitter (TX) with low receiver (RX)-band noise.

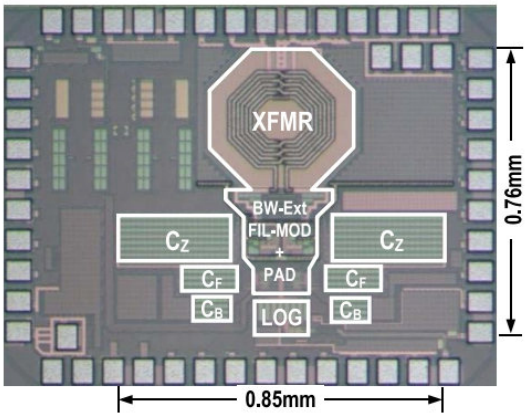


Fig. 2. Chip micrograph.

Publication(s)

[1] G. Qi, H. Shao, P.-I. Mak, J. Yin and R. P. Martins, "A multiband FDD SAW-less transmitter for 5G-NR featuring a BW-extended N-path filter-modulator, a switched-BB input and a wideband TIA-based PA driver," in IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3387-3399, Dec. 2020.

[2] G. Qi, H. Shao, P.-I. Mak, J. Yin, . P. Martins, "A 1.4-to-2.7GHz FDD SAW-less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, an Isolated-BB Input and a Wideband TIA-Based PA Driver Achieving <-157.5dBc/Hz OB Noise" IEEE ISSCC Dig. Tech. Papers, pp. 172-174, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A SAW-less Tunable RF Front-End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-LC N-Path LNA

Gengzhen Qi, Barend van Liempd, Pui-In Mak, Rui P. Martins and Jan Craninckx

FEATURES

SAW-less tunable RF-FE for 3GPP bands (0.7 to 1GHz)

High TX-RX isolation, >50dB tunable rejection

The first to achieve <-100dBm IM_3 at +20dBm TX power

The first to handle >+30dBm in-band TX power

Large-signal handling switched-LC N-path LNA

Fabricated in 0.18-µm SOI CMOS technology

DESCRIPTION

A SAW-less tunable RF-front end (RF-FE) prototype (Fig. 1) is proposed that integrates the gain-boosted (GB) switched-LC N-path LNA of together with the electrical-balance duplexer (EBD). The EBD cancels the transmitter–receiver (TX–RX) leakage at the RX frequency by dynamically optimizing the balance of a hybrid transformer, which enables in-band full-duplex (IBFD) operation. A transconductor-based LNA in parallel with a switched-LC N-path network creates input and output notches to reject TX leakage for frequency-division duplexing (FDD) operation. The LNA's signal-handling capability is enhanced via optimum switch biasing. This technique enables high linearity, better large-signal handling capability, and dual-frequency TX-to-RX isolation.

Fabricated in 0.18-µm SOI CMOS (Fig. 2), the RF-FE shows >50-dB tunable rejection from the TX input to the LNA output at both TX and RX frequencies, for all 3GPP bands from 0.7 to 1GHz. It is the first tunable RF-FE including an LNA that achieves +70-dBm TX-path IIP_3 and <−100-dBm IM_3 at +20-dBm TX power when a full-duplex spaced (FDS) jammer is applied at the antenna (FDD case) and the first that handles >+30-dBm in-band TX power while providing >50-dB self-interference cancellation (IBFD case). It consumes 62.5mW operating at 1GHz with 11.7-dB RX cascaded NF and 3.6-dB TX insertion loss, and occupies 9.62mm² active area.

This work features a highly integrated RF-FE for FDD and IBFD operations, meanwhile achieving comparable performances on TX-RX isolation, OB-IIP_3, OB-iB_{1dB} and NF etc., when benchmarked with the state-of-the-art works.

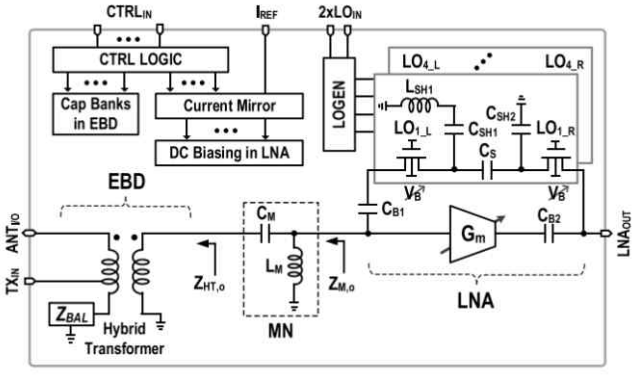


Fig. 1. High integrated RF- front end (RF-FE) using an electrical-balance duplexer (EBD) and a switched-LC N-path low-noise amplifier (LNA).

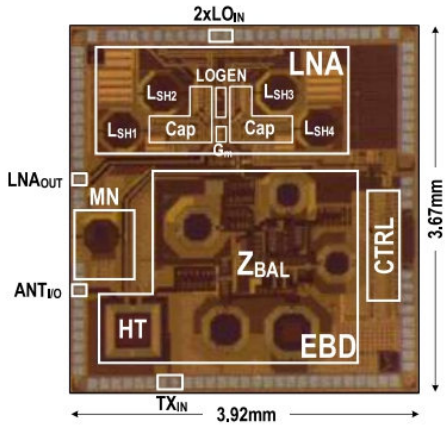


Fig. 2. Chip micrograph.

Publication(s)

[1] G. Qi, B. van Liempd, P.-I. Mak, R. P. Martins and J. Craninckx, "A SAW-less tunable RF front-end for FDD and IBFD combining an electrical-balance duplexer and a switched-LC N-path LNA," in IEEE Journal of Solid-State Circuits, vol. 53, no. 5, pp. 1431-1442, May. 2018.

[2] G. Qi, B. van Liempd, P.-I. Mak, R. P. Martins and J. Craincks, "0.7-1 GHz LO-defined SAW-less LNA for FDD using SOI CMOS technology," in IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Jun. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 0.096-mm² 1–20-GHz Triple-Path Noise Canceling Common-Gate Common-Source LNA With Dual Complementary pMOS–nMOS Configuration

Haohong Yu, Yong Chen, Chirn Chye Boon, Pui-In Mak, and Rui P. Martins

FEATURES

Common-gate common-source LNA

Triple-path noise canceling

Dual complementary pMOS-nMOS configuration

Silicon verified in 65nm CMOS

DESCRIPTION

We propose a novel wideband common-gate (CG) common-source (CS) low-noise amplifier (LNA) with a dual complementary pMOS–nMOS configuration to provide a current-reuse output. Triple-path noise-cancellation is revealed to eliminate the thermal noise of the two CG transistors. Simultaneously, partial cancellation of intrinsic third-order distortion of output-stage transistors improves the input third-order intercept point (IIP3). In addition, we embed a resistive feedback in one of the auxiliary CS amplifiers to balance the multiple tradeoffs between noise figure (NF), input matching (S_{11}), and forward gain (S_{21}).

Fabricated in 65-nm CMOS, the proposed wideband LNA exhibits an IIP3 of 2.2–6.8 dBm and an NF of 3.3–5.3 dB across a 19-GHz BW while consuming 20.3 mW at 1.6 V. S11 is <−10 dB up to 23 GHz by designing a π-type inputmatching network. The LNA exhibits a peak S21 of 12.8 dB and occupies a very compact die area of 0.096 mm².

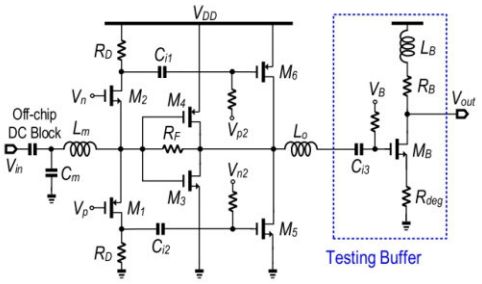


Fig. 1. Complete schematic of our wideband LNA.

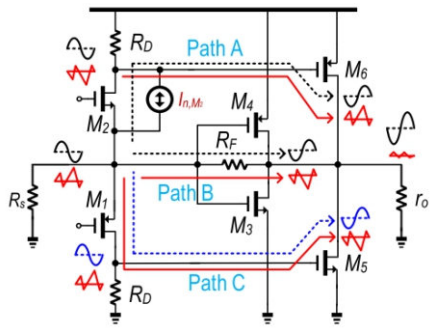


Fig. 2. Overall triple-path NC mechanism.

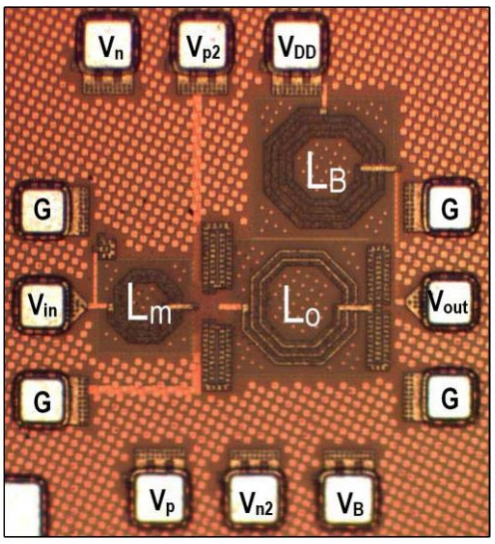


Fig. 3. Die photograph of the fabricated wideband LNA.

Publication(s)

[1] H. Yu, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, "A 0.096-mm² 1-to-20-GHz Triple-Path Noise-Cancelling Common-Gate Common-Source LNA with Complementary pMOS-nMOS Configuration," IEEE Transactions on Microwave Theory and Techniques, vol. 68, pp. 144-159, Jan. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled MM-Wave VCO Using a Single-Center-Tapped Switched Inductor

Yatao Peng, Jun Yin, Pui-In Mak and Rui P. Martins

FEATURES

An inductive mode-switching technique to vary the effective tank inductance without compromising the tank quality factor

Coupling four voltage-controlled-oscillator (VCO) cores for phase noise reduction

Silicon verified in TSMC 65 nm CMOS

A state-of-the-art peak FoM of 186.6 dBc/Hz at 50 GHz

DESCRIPTION

This work proposes a mode-switching quad-core-coupled millimeter-wave (mm-Wave) VCO, using an inductive mode-switching technique to extend the frequency tuning range and improve the phase noise. The switches not only serve for in-phase coupling among the VCO cores but also can modify the equivalent tank inductance suitable for coarse frequency tuning. The frequency gaps between the multi-resonant frequencies are controlled by the common-mode (CM) inductance LCM precisely set by the lithography fabrication. Together with the tiny varactors for fine frequency tuning, a wide and continuous frequency tuning range can be achieved. It is analytically shown that tiny switches (i.e., small parasitic capacitance) for mode selection are adequate to avoid bimodal oscillation, synchronize the VCO cores against resonance frequency mismatches, and prevent PN degradation. A symmetrical layout of a single-center-tapped switched inductor also aids the VCO to be immune to magnetic pulling

Prototyped in 65-nm CMOS, our VCO exhibits a 16.5% tuning range from 42.9 to 50.6 GHz. The phase noise at 50 Ghz is −115.6 dBc/Hz at 3-MHz offset, corresponding to a figure-of-merit (FoM) of 183.6 dBc/Hz. The die size is 0.039 mm²

Benchmarking with the prior fundamental VCOs operating above 40GHz, our design exhibits the best-in-class phase noise and FOM.

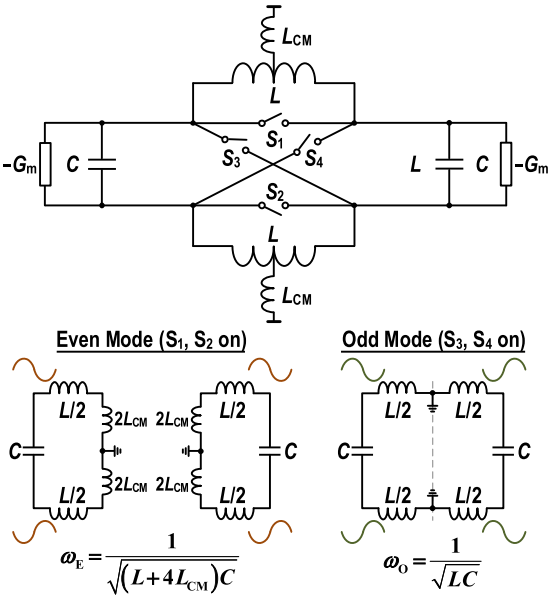


Fig. 1. Proposed inductive mode-switching technique.

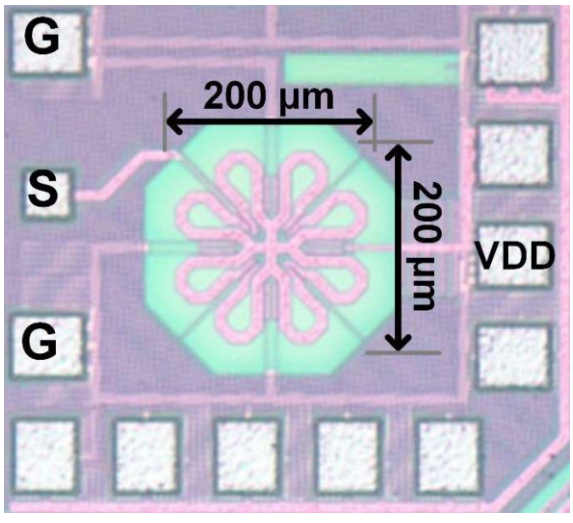


Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Peng, J. Yin, P. -I. Mak, and R. P. Martins, "Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled mm-wave VCO Using a Single-Center-Tapped Switched Inductor," IEEE Journal of Solid-State Circuits, pp. 3232-3242, vol. 53, Nov. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of the University of Macau.