澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

SKL 2010DP
模拟与混合信号
超大规模集成电路
国家重点实验室
（澳门大学）
State Key Laboratory of Analog and Mixed-Signal VLSI
(University of Macau)
中华人民共和国科学技术部
The Ministry of Science and Technology of the People's Republic of China

模擬與混合信號超大規模集成電路
國家重點實驗室
State Key Laboratory of
Analog and Mixed-Signal VLSI

State Key Lab of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) Newsletter

Motto: "Locally, from (World) Quality towards (National) Quantity"

座右銘:立足本土、人才培養, 以世界級質量創建國家級規模

Year 10
No . 10

March 2021

2020 Milestones

Co-Funded by
Macao Science and Technology Development Fund (FDCT)

Events

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) participated in the 14th Annual Meeting of the Committee for China and Macao Cooperation in Science and Technology held in Zhuhai, Guangdong, China, December 10, 2020.

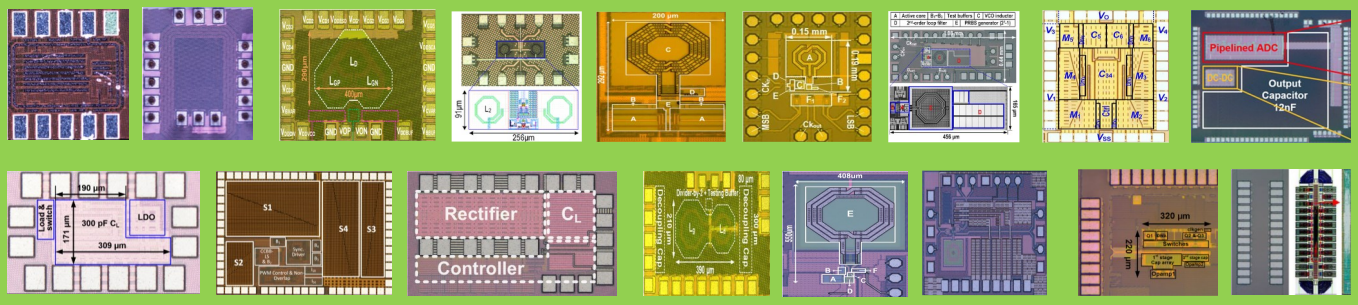
The SKL AMS-VLSI from UM and IDQ-Macau jointly developed and donated 2 ventilator prototypes to Angola and Mozambique.

UM's online workshop on IC advances in China (ICAC 2020) held on June 2020 successfully attracted 10000 from around the world.

Prof. Elvis Mak Pui-In elected Fellow of the UK Royal Society of Chemistry in the United Kingdom.

Prof. Lam Chi Seng appointed Associate Editor of the internationally renowned journal IEEE Transactions on Industrial Electronics.

State-of-the-Art Chips - Designed and Tested in 2020 (17 chips)



ISSCC 2021

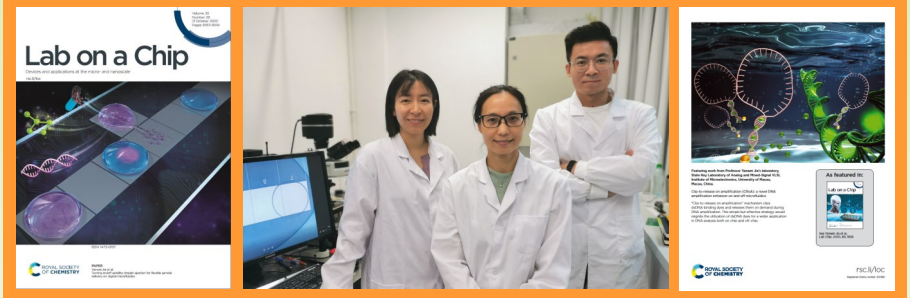
A team of faculty members and students from the SKL AMS-VLSI and ECE/FST, University of Macau (UM) published their results to the 67th IEEE International Solid-State Circuits Conference (**ISSCC**) in **February 2021** virtually (in San Francisco, CA, USA), the most competitive conference in the world in the field of chip design. However, due to the Outbreak of the New Corona Virus followed by the Declaration of Public Health Emergency of International Concern by World Health Organization, the SKL AMS-VLSI delegation was reluctantly absent from this significant event in the area this year.

This year, 2 digest papers in areas of Data Converters and RF were accepted at ISSCC 2021, "A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz $1/f^3$ PN Corner Without Harmonic Tuning", provided by H. Guo, Y. Chen, P-I. Mak, R. P. Martins, and "A 25MHz-BW 75dB-SNDR Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC with Background Offset Calibration", provided by H. Zhang, Y. Zhu, C-H. Chan, R. P. Martins. Besides, 1 SKLab PhD student received a Student Research Preview and Prof. Yan Lu delivered a tutorial on "Fundamentals of Fully Integrated Voltage Regulators".

2 New Master Programs

The Institute of Microelectronics (IME) will provide two new programs of Master in Microelectronics which will help to train research scholars and application engineers in the area of microelectronic integrated circuits.

New Breakthroughs in Nucleic Acid Analysis Technique and New Microfluidic Technology



A research team from Institute of Microelectronics (IME) proposed a novel DNA amplification enhancer to significantly improve the performance of DNA amplification methods in both benchtop assays and on-chip assays in microfluidic devices. This enhancer would allow users to observe, with the naked eye, the results of nucleic acid amplification tests for different kinds of viruses, such as the novel coronavirus, thereby facilitating fast, portable virus testing for large populations. The study has been published in the well-known international journal Lab on a Chip from the Royal Society of Chemistry, UK. The article was selected as featured paper to appear in the back cover of the journal.

This team has also developed a new on-chip sample delivery technology. The new technology will not only enhance droplet dispensing on chips, but will also greatly improve sample preparation efficiency, paving the way for realizing 'lab-on-a-chip'. This article was also selected as featured paper to appear in the inside back cover.

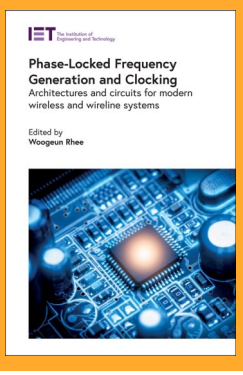
PhD Graduate from UM Receives Young Researcher Award 2020

Dr. Wen-Liang Zeng (Steven), a doctoral graduate from the University of Macau's State Key Laboratory of Analog and Mixed Signal VLSI, Institute of Microelectronics, and Department of Electrical and Computer Engineering, was awarded the "Young Investigator Award 2020" by the International Institute of Macau and the Macau Foundation, with his doctoral thesis "Design, Control and Analysis of Integrated DC -DC Converters for Low-Power Applications", in which the award ceremony was held successfully on January 18, 2021.

8 New PhD Graduates in 2020

8. **LI Mingzhong,** *Patterned Surface Wettability and Advanced Droplet Manipulation Techniques for Disease Diagnostics using Digital Microfluidics*.
7. **Guo Mingqiang,** *Mismatch Calibration Techniques for Low-Power High-Speed Time-Interleaved ADC*.
6. **Yang Zunsong,** *Low-Reference-Spur Integer-N RF Phase-Locked Loop*.
5. **Guo Hao,** *Millimeter-Wave Multi-LC-Tank Voltage-Controlled Oscillator*.
4. **Zhao Xiaoteng,** *Power-Efficient Bang-Bang Clock and Data Recovery Circuit*.
3. **Li Xiaofei,** *Mismatch Calibration Techniques for Low-Power High-Speed Time-Interleaved ADC*.
2. **Lin Jie,** *Mismatch Calibration Techniques for Low-Power High-Speed Time-Interleaved ADC*.
1. **Mao Fangyu,** *Mismatch Calibration Techniques for Low-Power High-Speed Time-Interleaved ADC*.

A Chapter in a Book by The Institution of Engineering and Technology - IET, UK



Selected works from each research line

In ISSCC 2019 and JSSC 2020

Piezoelectric Energy Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier with Capacitor-Reuse for Input Power Adaptation

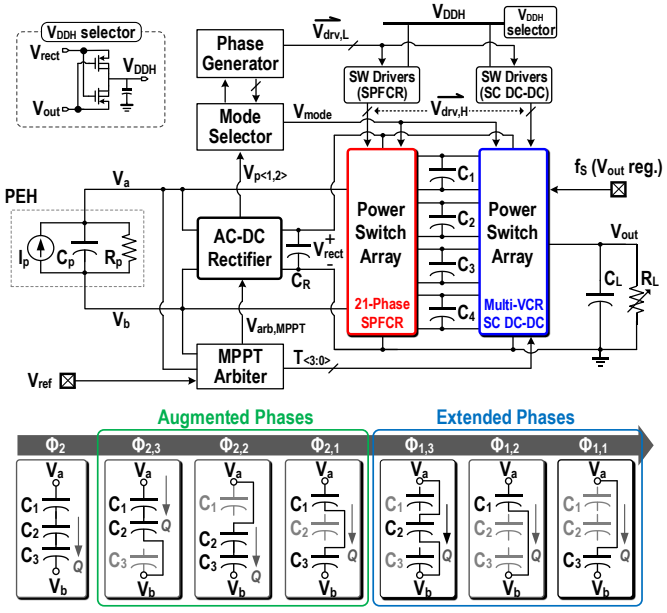
Zhiyuan Chen, Man-Kay Law, Pui-In Mak, Xiaoyang Zeng and Rui P. Martins

From Wireless and Biomedical Innovation Center (WMIC)

Motivation

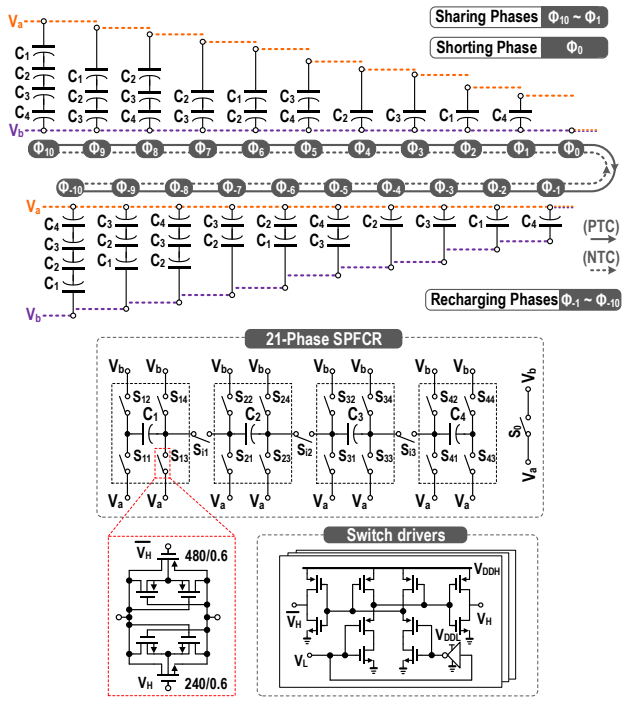
This work proposes a split-phase flipping-capacitor rectifier (SPFCR) to resolve the hard tradeoff between the number of capacitors and the energy extraction efficiency for capacitive piezoelectric energy harvesting (PEH) interfaces. By splitting the capacitor usage into multiple phases, this work can achieve the most number of flipping phases using the same number of capacitors when compared with the state of the art. To further improve the input power adaptation, the flipping capacitors are reconfigured as a multiple voltage conversion ratio switched-capacitor DC-DC converter during the non-flipping period without using extra passives. Fabricated in 0.18-μm CMOS, the proposed 21-phase SPFCR PEH interface demonstrates a measured maximum output power improving rate (MOPIR) of up to 9.3× with VD=0.12V when compared with the conventional FBR interface over an equivalent FBR input power range from 0.15 to 5.57μW.

Architecture



System overview of the proposed SPFCR and capacitor reuse multiple-VCR SC DC-DC converter for piezoelectric energy harvesting, as well as the capacitor reconfiguration examples using SPFCR with 3 flying capacitors.

Implementation



Reconfiguration and circuit implementation of 21-phase SPFCR with the switch drivers.

Verification

	This work	JSSC'17 [17]	JSSC'17 [18]	JSSC'19 [19]
Technology	0.18 μm	0.35 μm	0.18 μm	0.18 μm HV
Energy Extraction Technique	SPFCR	SSHC	FCR	SE-SSHC
Piezoelectric Harvester	MIDE PPA1021	MIDE V21BL	P5A4E @ 5mm3	Custom MEMS
Harvester Size	71×10.3×0.86 mm³	90×16.7×0.79mm³	5×1×1 mm³	7×2 mm² (4 pieces)
C_p	22nF	45nF	78.4pF	1.94pF
Key Component	4 Capacitors[a] 21 phase	8 capacitors[a] 17 phase	4 Capacitors[b] 7 phase	8 Capacitors[b] 17 phase
C_{total}	272nF	360nF	1.44nF	4nF
MOPIR	5.9 ~ 9.3× @V_D=0.12V 3.7 ~ 6.2× @V_D=0V	9.7×	4.83×	8.21×
P_{in} adaptation	Capacitor-reuse Multi-VCR SC DC-DC	no	no	no
MPPT	Yes ($V_{OC,FBR}$-based)	no	no	no
Voltage Flipping Efficiency	0.84	0.8	0.85	0.69
Chip Size	0.2 mm²	2.9 mm²	1.7 mm²	5.3 mm²
Output Power	0.5 ~ 64 μW	161.8 μW	50.2 μW	186 μW
Operating Freq.	200Hz	92 Hz	110 kHz	219Hz

[a] Off-chip component [b] On-chip component

Performance summary and comparison with the state-of-the-art PEH systems.

Acknowledgement: This work was supported in part by the Science Foundation Ireland under Grant 14/RP/I2921 and in part by the Science and Technology Development Fund, Macau SAR, under Grant 0044/2019/A1 and Grant SKL Fund.

In JSSC 2020

A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Push–Pull LNA

Kai Xu, Jun Yin, Pui-In Mak, Robert Bogdan Staszewski and Rui P. Martins

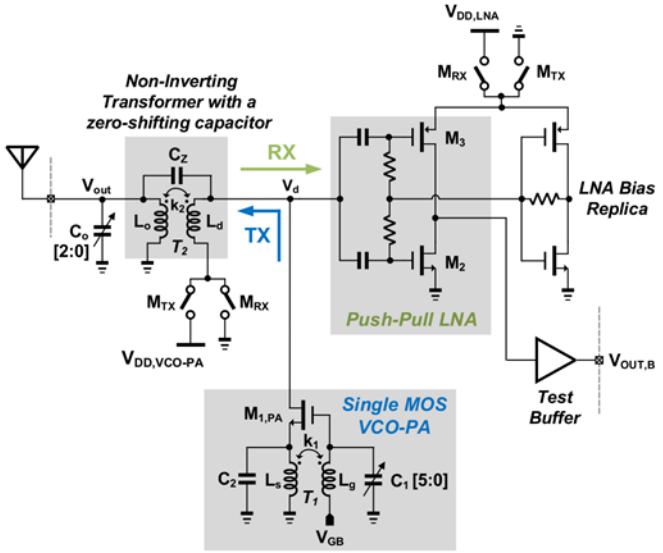
From Wireless and Biomedical Innovation Center (WMIC)

Motivation

Ultra-low-power radios play a crucial role in the expansion of IoT connectivity where wireless sensors gather and exchange a massive amount of data. In battery-operated low-data-rate, short-range sensor applications, such as temperature, humidity and pressure monitoring, as well as health tracking, the major bottleneck lies in the battery life.

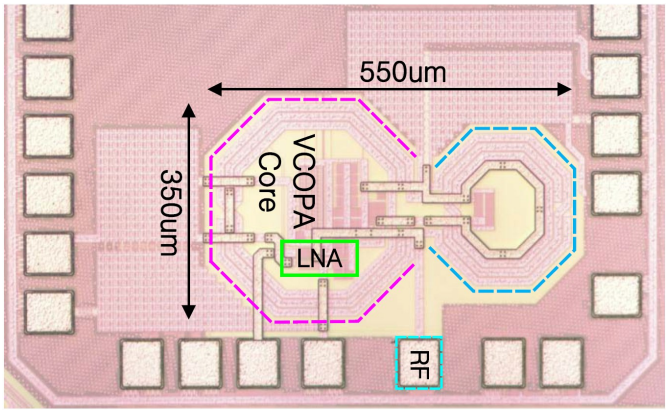
In this work, we propose a simple power-efficient sub-1-V fully integrated RF front end for 2.4-GHz transceivers. It features (1) a function-reuse single MOS digitally controlled oscillator power amplifier (DCO-PA) to improve antenna-to-DCO isolation for better resilience to jammers; (2) a noninverting TX matching transformer with a zero-shifting capacitor to suppress the second-harmonic emission of the DCO-PA and allows a single-pin antenna interface for both TX and RX modes eliminating the T/R switches in the signal path; (3) a push–pull low-noise amplifier (LNA) to reuse the TX matching transformer for passive gain boosting that reduces power consumption.

Architecture



Schematic of the single-pin antenna interface RF front end.

Implementation



Chip micrograph of the single-pin antenna interface RF front end in 65 nm CMOS.

Verification

COMPARISON WITH STATE-OF-THE-ART 2.4-GHz LNA

	Technology	Frequency (GHz)	Supply (V)	P_{DC} (μW)	NF (dB)	Gain (dB)	IIP3 (dBm)	FOM * (dB)
[34]	65nm	2.4	0.7	475	2.8	17.4	-10.7	28.8
[35]**	40nm	2.4	0.8	30	3.3	14.2	-11.6	38.2
[35]**	40nm	2.4	0.18	30	5.2	14	-8.6	37.7
[36]	65nm	2.4	0.3	930	4.7	20.2	-20	20.7
This work	65nm	2.4	0.5	174	6.8	11	-2.2	30.2

* $FOM=10\log\left(10^{Gain/20}\cdot10^{(IIP3-10)/20}/(10^{NF/10}P_{DC}\cdot10^{-3})\right)$ [34] ** [35] includes two LNA designs with simulation results only

COMPARISON WITH STATE-OF-THE-ART 2.4-GHz RFE

	CICC' 18 [12]		JSSC' 19 [7]		JSSC' 14 [16]		JSSC' 16 [13]		JSSC' 17 [14]		This work		
CMOS Technology	40nm		40nm		130nm		130nm		65nm		65nm		
Supply Voltage (V)	0.4		0.6 to 0.9		1		1.2		0.3 to 0.7		0.3 to 0.7		
RF band (GHz)	2.4		2.4		2.4		2.4		2.4		2.4		
TX Architecture (in open loop operation)	LC-VCO + Class-D PA		Ring OSC + Edge Combiner + SC-DPA		VCO-PA-LNA co-design		PA-VCO Stack		Function-Reuse Class-F DCO-PA		Single-MOS DCO-PA		
RF Power (dBm)	-10	0	-20	-3.3	-30	-4.4	-5	-1	-5	0	-20	-10	0
Power Consumption (mW) (VCO + Divider + Buffer + PA)	1.27	4.22	0.27	1.62	1.5	7	2.58	4.46	2.04	4.4	0.62	0.98	4.8
Efficiency (%)	8	23.7	3.7	28.9	0.07	5.2	12.2	17.9	15.5	22.6	1.6	10.2	20.8
Active Area (mm^2)	0.35		0.0166		0.5		0.2		0.39		0.17		
HD2/HD3 (dBm) @ P_{out}	-52 / - @ 0dBm		-42.5 / -48.5 @ 0dBm ***		N/A		-50 / -47 @ 0dBm		-43.2 / -47.6 @ 0dBm		-44.4 / -50.2 @ 0dBm		
VCO Phase Noise (dBc/Hz) @ 2.5 MHz / RF power	-123 **		-90		-125 @ -4.4Bm		-129 @ -1dBm		-125 @ 6dBm		-126 @ 0dBm -108 @ -20dBm		
VCO Frequency Range (GHz)	2.3-2.5		2.4-2.5		2.2-2.488		2.26-2.58		2.376-2.408		2.2-2.5		
TX_FOM * (dBm) @ 0dBm	-75.7		-		-		-73.5 @ -1dBm		-66.7		-67.6		
5MHz jammer Image Spur (dBm) @ -30dBm interferer	N/A		N/A		N/A		N/A		-13		-41		
Max P_{out} Variation (dB) under VSWR = 1.5 : 1 @ P_{out}	N/A		N/A		N/A		N/A		2.1dB @ 6dBm		1.1dB @ 0dBm		
VCO-PA efficiency (%) under VSWR = 1.5 : 1 @ P_{out}	N/A		N/A		N/A		N/A		14 to 27.5 @ 6dBm		16 to 24.5 @ 0dBm		
No. of external components	2		2		0		2		1		0 ****		
Integrated T/R Switch	No		No		Yes		No		No		Yes		

* TX_FOM = HD2 + 10log(PDC) [12] ** Normalized from 2X carrier frequency *** DPA operated in saturation region under 1.2V supply **** Bondwire utilized for input matching in RX mode

Acknowledgement: This work was in part funded by Science and Technology Development Fund, Macau SAR (File no. 0069/2016/A2), and by University of Macau (File no. MYRG2018-00196-AMSV).

In Analytical Chemistry 2020

Portable NMR with Parallelism

Ka-Meng Lei, Dongwan Ha, Yi-Qiao Song, Robert M Westervelt, Rui P. Martins, Pui-In Mak, and Donhee Ham

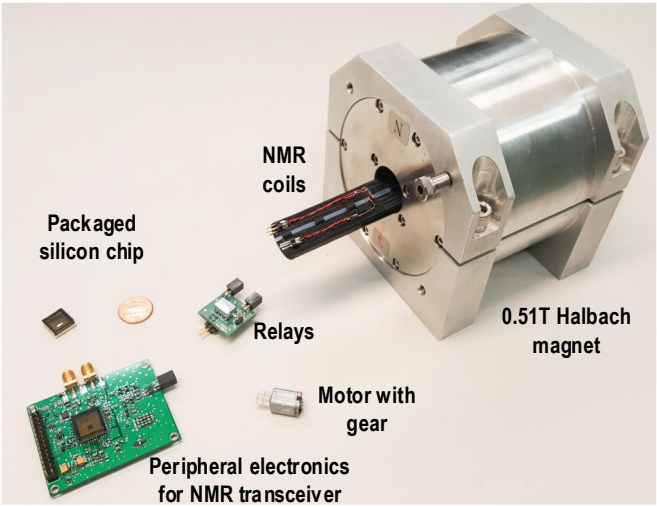
From Wireless and Biomedical Innovation Center (WMIC)

Motivation

Nuclear Magnetic Resonance (NMR) is an essential method to observe the molecular information and dynamics of the samples in the laboratory. It plays a crucial role in chemistry, physics, and biology. Yet, the bulky size and slow throughput are two critical drawbacks for NMR.

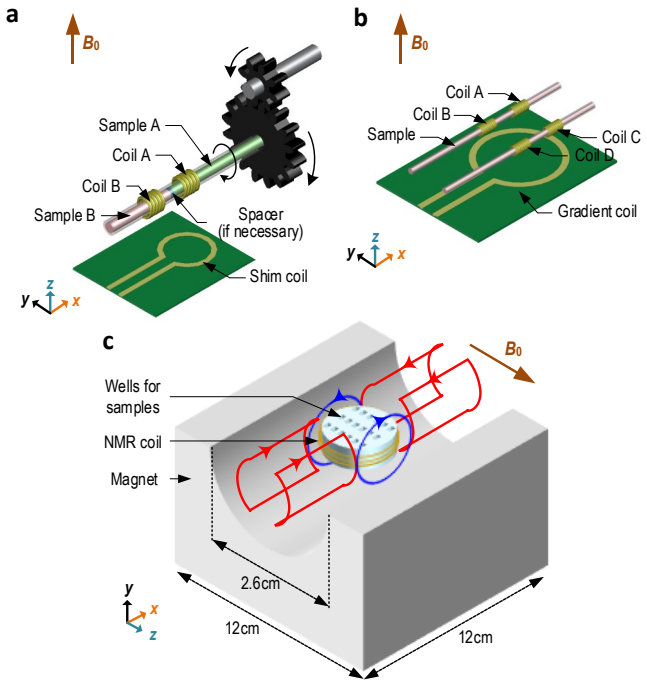
Portable NMR combining a permanent magnet and a complementary metal-oxide-semiconductor (CMOS) integrated circuit has recently emerged to offer the long desired online, on-demand, or in situ NMR analysis of small molecules for chemistry and biology. Here we take this cutting-edge technology to the next level by introducing parallelism to a state of-the-art portable NMR platform to accelerate its experimental throughput.

Architecture



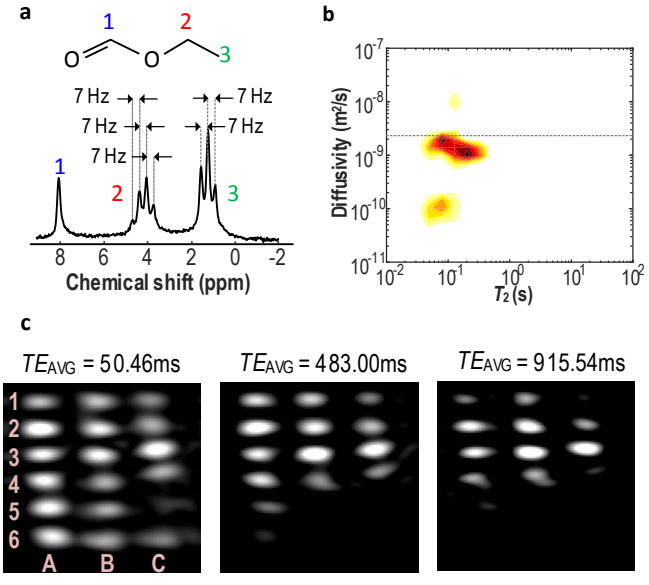
Our portable NMR platform, whose key components are the Halbach magnet and the silicon IC. The motor, together with the shim coils, improved the homogeneity of the magnetic field for high resolution spectroscopy.

Implementation



Configuration for (a) high resolution spectroscopy, (b) relaxometry, and (c) high-throughput T_2-screening enabled by magnetic resonance imaging.

Verification



Experimental results from the portable NMR platform with parallelism. (a) ^{1}H NMR spectrum from ethyl formate. (b) 2D D-T_2 maps from heavy milk. (c) T_2 of 18 samples with varying concentrations of β-lactoglobulin treated at different temperatures. All of the experiments are accelerated by 2 – 4.5 times.

Acknowledgement: This work was supported in part by the Macao Science and Technology Development (FDCT) – State Key Lab (SKL) Fund, US Department of Energy Basic Energy Sciences grant (DE-FG02-07ER46422), US Advanced Research Projects Agency-Energy (DE-AR0001063), and the US National Science Foundation (DMR-1231319 and EFMA-1542807).

In Microsystems & Nanoengineering Nature Publishing Group

A Digital Microfluidic System with 3D Microstructures for Single-cell Culture

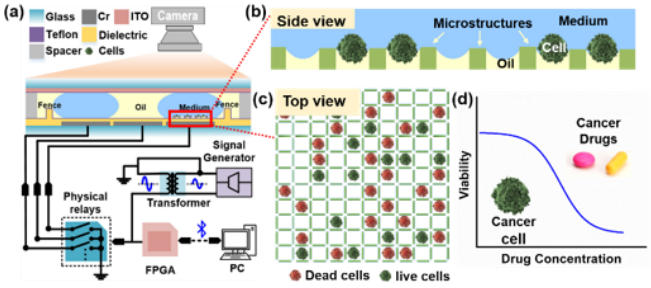
Jiao Zhai, Haoran Li, Ada Hang-Heng Wong, Cheng Dong, Shuhong Yi, Yanwei Jia, Pui-In Mak, Chu-Xia Deng and Rui P. Martins

From Wireless and Biomedical Innovation Center (WMIC)

Motivation

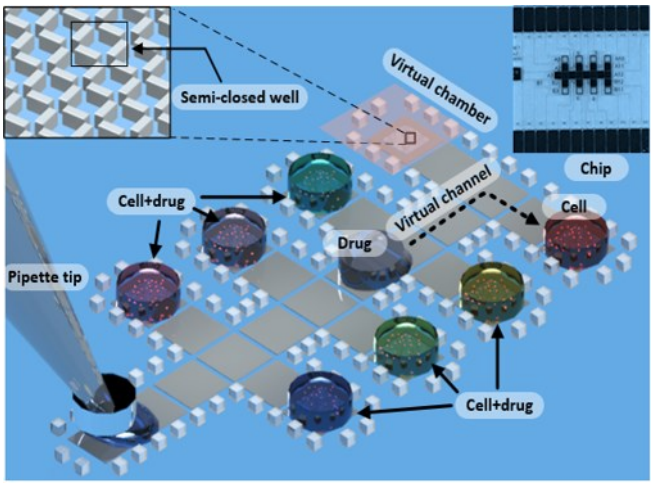
Despite the precise controllability of droplet samples in digital microfluidic (DMF) systems, their capability in isolating single cells for long-time culture is still limited: typically only a few cells can be captured on an electrode. Although fabricating small-sized hydrophilic micropatches on an electrode aids single cell capture, the actuation voltage for droplet transportation has to be significantly raised, resulting in a shorter lifetime for the DMF chip and a bigger risk for damaging the cells. Therefore, a more robust system with higher efficiency in trapping single cells on-chip and a low actuation voltage is desired without compensating the droplet movement efficiency. The most powerful 3D microstructures widely employed in channel microfluidics for single cell trapping have been neglected in exploration on digital microfluidics. The target of this work is to explore this direction of research.

Architecture



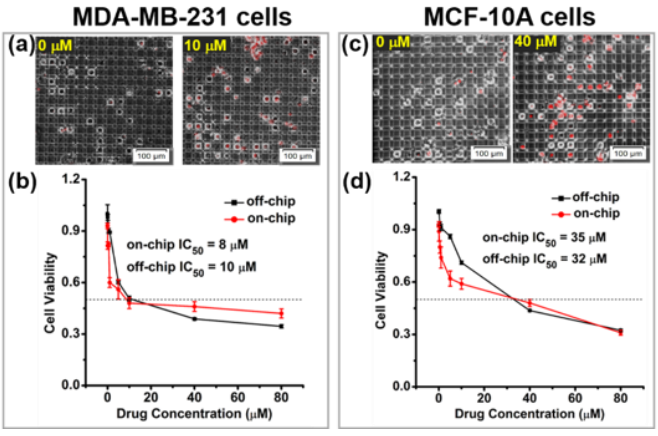
In this report, we present a DMF system for single cell culture with innovative micropatterned arrays constructed by 3D microstructures fabricated on the DMF chip to trap single cells and to prevent the trapped cells from aggregating during a long-time cell culture. To minimize the influence of electric actuation voltage on the cellular health, a low evaporation temperature and gas soluble silicone oil with a solubility of oxygen several times greater than in water and a fluorinated surfactant were introduced in the system to lower the actuation voltage to 36V, 4 times lower than normally used (150V).

Implementation



Our optimum results exhibited that about 20% micro-wells over a 30 × 30 array were occupied by isolated single cells. The cell viability can be obtained in 24 hours culturing, providing a fast result return.

Verification



To exemplify the technological advances, drug sensitivity tests were run in our DMF system to investigate the cell response of breast cancer cells (MDA-MB-231) and breast normal cells (MCF-10A) to a widely used chemotherapeutic drugs, Cisplatin (Cis). The results on-chip were consistent with that screened in conventional 96-well plates.

Acknowledgement: This work was supported by FDCT110/2016/A3 and AMSV SKL Fund from the Macau Science and Technology Development Fund (FDCT), MYRG2017-00022-AMSV and MYRG2018-00114-AMSV from the University of Macau.

In IEEE APCCAS 2019 & IEEE TCAS-I 2021

A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM- 4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS

Xiaoteng Zhao, Yong Chen, Pui-In Mak, and Rui P. Martins

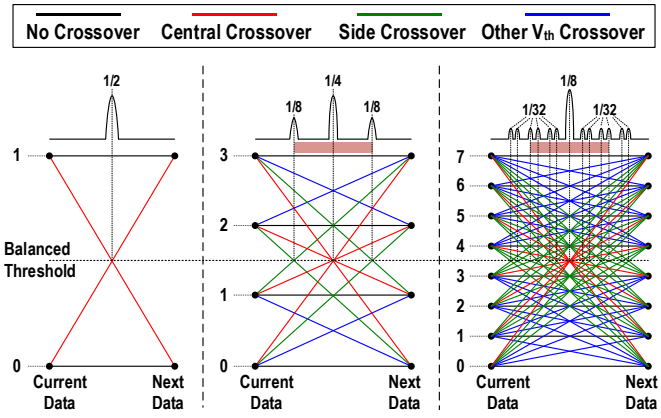
From Wireless and Biomedical Innovation Center (WMIC)

Motivation

The bandwidth (BW) limitation of the channel, which is associated with the dielectric loss and skin effect, has recently become one of the bottlenecks of high-speed electrical and optical links. When the data rate escalates, this issue gets worse especially for the non-return-to-zero (NRZ) format. To surmount this, a variety of multi-level pulse amplitude modulation (PAM) techniques are widely explored for their higher BW efficiency.

This paper proposes a trimodal half-rate bang-bang clock and data recovery (BBCDR) circuit incorporating a single-loop phase-tracking loop that only detects the balanced-threshold transitions of the NRZ/PAM-4/PAM-8 patterns, saving the required sampling slicers. Besides, we introduce a number of low-power architectural and circuit techniques to improve the energy efficiency (<0.29 pJ/bit) in 28-nm CMOS and uphold a good jitter performance.

Principle



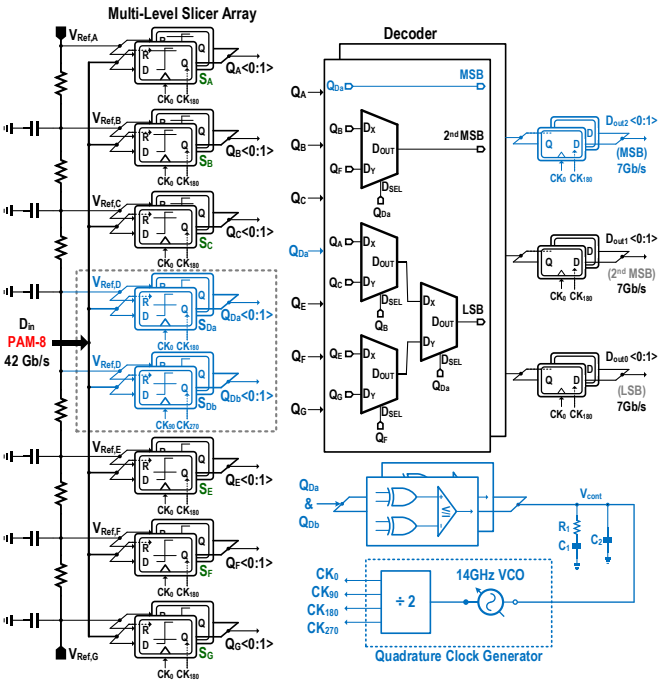
Crossover-points distribution in NRZ,PAM-4 and PAM-8 signaling.

	Slicer							2nd MSB Decoder	LSB Decoder	VCO Divider	XOR V/I
	A	B	C	D	E	F	G				
NRZ	✕	✕	✕	✓	✕	✕	✕	✕	✕	✓	✓
PAM-4	✕	✓	✕	✓	✕	✓	✕	✓	✕	✓	✓
PAM-8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓ Powered on ✕ Powered off

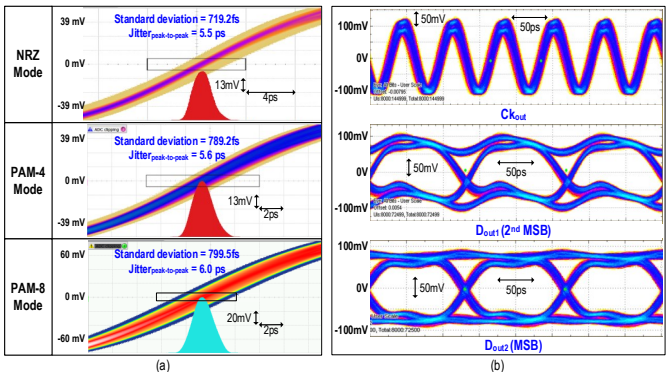
Operation of sub-block under different modes.

Implementation



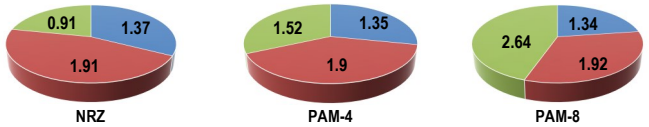
Complete schematic of the proposed trimodal BBCDR circuit under PAM-8 mode.

Verification



(a) Jitter histogram distribution under three modes and (b) recovered clock and data eyes under PAM-4 mode.

NRZ		PAM-4		PAM-8	
Module	Power (mW)	Module	Power (mW)	Module	Power (mW)
VCO Core	1.37	VCO Core	1.35	VCO Core	1.34
Clock Tree	1.91	Clock Tree	1.90	Clock Tree	1.92
Data Path	0.91	Data Path	1.52	Data Path	2.64
Total	4.19	Total	4.77	Total	5.90



Power breakdown under three modes

Acknowledgement: This work was supported in part by the Guangzhou Science and Technology Innovation and Development of Special Funds (GSTIC) under Grant EF002/IME-CY/2019/GSTIC and in part by the Macau Science and Technology Development Fund (FDCT)—SKL Fund.

In JSSC 2020

A 1.6GS/s 12.2mW 7/8-way Split Time-Interleaved SAR ADC achieving 54.2-dB SNDR with Digital Background Timing Mismatch Calibration

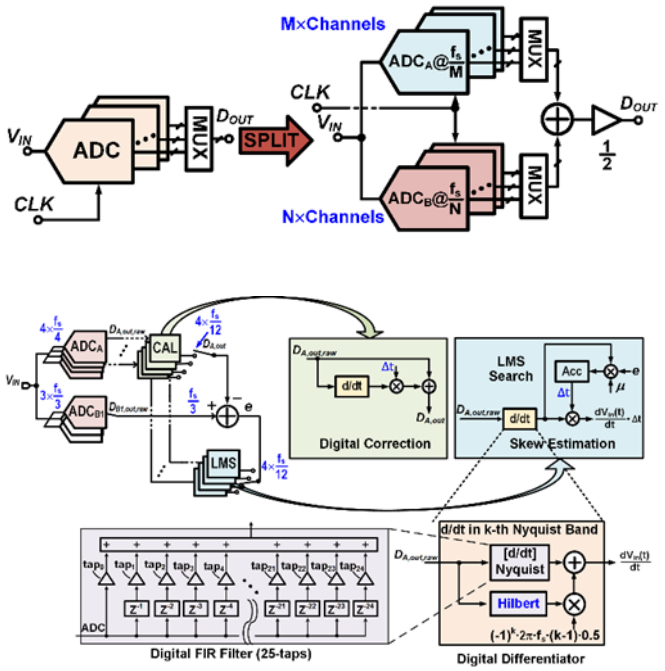
Mingqiang Guo, Jiaji Mao, Sai-Weng Sin, Hegong Wei, and Rui P. Martins

From Data and Power Conversion Innovation Center (DPIC)

Motivation

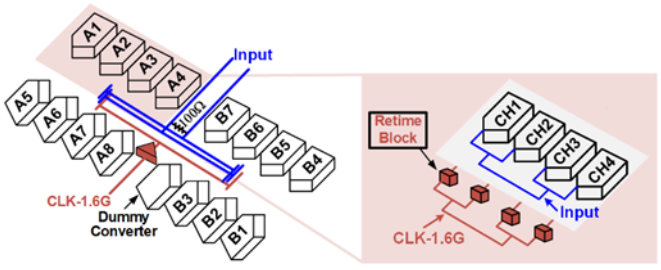
This work presents a split time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with digital background timing-skew mismatch calibration. It divides a TI-SAR ADC into two split parts with the same overall sampling rate but different numbers of TI channels. Benefitting from the proposed split TI topology, the timing skew calibration convergence speed is fast without any extra analog circuits. The input impedance of the overall TI-ADC remains unchanged, which is essential for the preceding driving stage in a high-speed application. We designed a prototype 7/8-way split TI-ADC implemented in 28nm CMOS. After a digital background timing skew calibration, it reaches a 54.2 dB SNDR and 67.1 dB SFDR with a near Nyquist rate input signal and a 2.5GHz effective resolution bandwidth (ERBW). Furthermore, the power consumption of ADC core (mismatch calibration off-chip) is 12.2mW running at 1.6GS/s, leading to a Walden FOM of 18.2fJ/conv.-step and a Schreier FOM of 162.4dB, respectively.

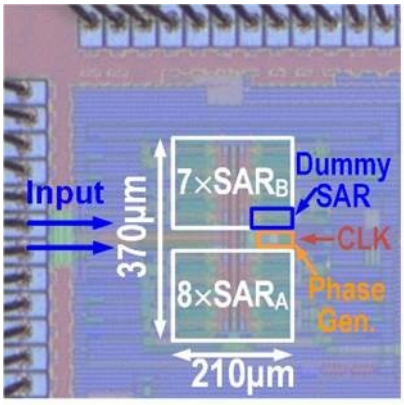
Architecture



The proposed split time-interleaved ADC with the background timing-skew calibration.

Implementation

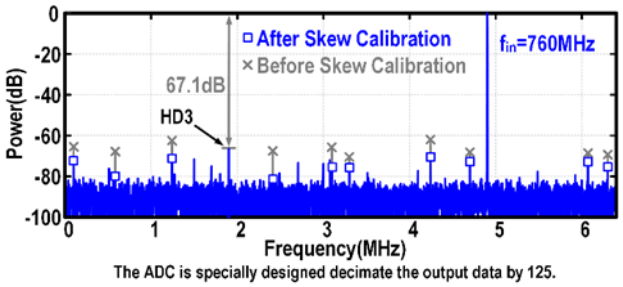




ADC Architecture, and Chip Photograph.

Verification

Measured output spectrum



The ADC is specially designed decimate the output data by 125.

ADC Comparison Table

	ISSCC-15 [25] H.-K. Hong	ISSCC-15 [26] B.-R.-S. Sung	JSSC-18 [3] C.-Y. Lin		VLSI-16 [13] Y.-C. Lien	VLSI-17 [12] Lei Luo	This Work	
Technology	45nm	45nm	40nm		16nm	16nm	28nm	
Architecture	TI-SAR	TI-FATI	TI-SAR		TI-SAR	TI-SAR	TI-SAR	
Resolution(bit)	10	10	10		10	10	10	
Speed(GS/s)	1.7	1.6	2.6		1.6	2.0	1.6	
Supply(V)	1.2	1.1	0.95		1.1	0.85/1.5	0.9/0.8	
Skew Correction	Analog	Analog	Digital		Analog	Analog	Digital	
SFDR@Nyq.(dB)	62.0	61.2	57.8		61	56	67.1	
SNDR@Nyq.(dB)	51.2	56.1	50.6		50.3	50.1	54.2	
SNDR@>Nyq.(dB)	NA	NA	NA		NA	NA	51.3@2.52GHz	
Power(mw)	15.4	17.3	18.4	39.2(1)	9.8	10.4	12.2	19.8(1)
Area(mm²)	0.057	0.36	0.825	0.92(1)	0.023	0.014	0.078	0.168(1)
FOM@Nyq.(fJ/c.-s)	30.4	21	25.6	54.5(1)	19.2	19.9	18.2	29.5(1)
FOMS@Nyq.(dB)	158.6	162.8	159.1	155.8(1)	160.2	159.9	162.4	160.3(1)

(1)With estimated calibration power and area

Acknowledgement: This work was financially supported by Research Grants of University of Macau (Ref: MYRG2018-00204-AMSV) and Macau Science & Technology Fund (Ref: SKL-AMSV-2017-2019(DP)).

In ISSCC 2020 and JSSC 2020

An 8-Bit 10-GS/s 16× Interpolation-Based Time-Domain ADC With <1.5-ps Uncalibrated Quantization Steps

Minglei Zhang, Chi-Hang Chan, Yan Zhu, and Rui P. Martins

From Data and Power Conversion Innovation Center (DPIC)

Motivation

Application

- ❑ Wireline Communications
- ❑ RF-Sampling Systems
- ❑ Oscilloscopes and Wideband Digitizers

Existing Time-Interleaved ADC Challenges

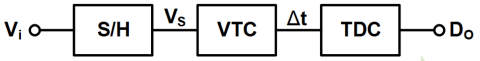
Time-Interleaved SAR

- Large Input Capacitance
- Limited Bandwidth
- Large Channel Number

Time-Interleaved Flash

- Limited Resolution
- Power Hungry
- Large Calibration Overhead

Time-Domain ADC Characteristics



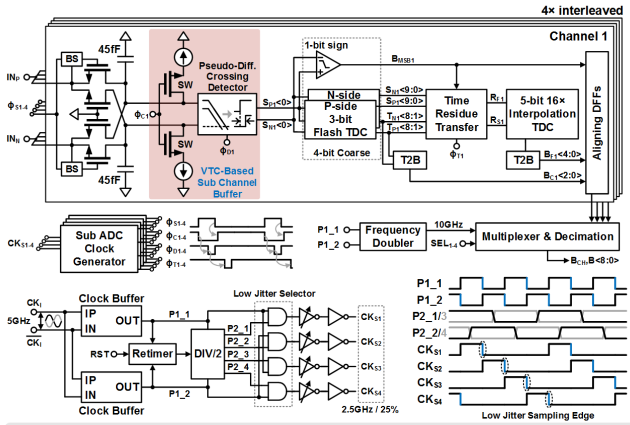
☺ Easy to be Interleaved
- ✓ Small Input Capacitance -> Large Bandwidth
- ✓ Inherent Isolation between S/H & QTZ
- ✓ Speed/Power/Area Technology Scaling

☹ Need Calibration for Sub 2 ps Time Step

This Work: Calibration-Free Time LSB Step (1.375 ps)

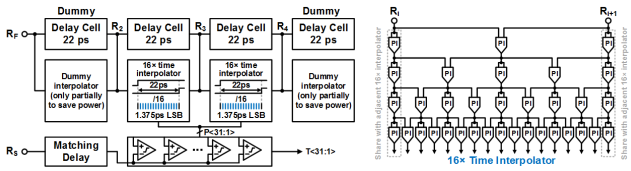
Architecture

8-bit Fully Time-Domain ADC Architecture (4×)



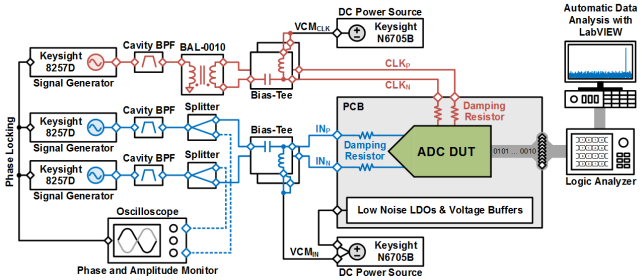
- VTC-Based Sub Channel Buffer
- Interpolation-Based Inter-Stage Gain (16×)
- Uncalibrated Inter-Stage Gain & QTZ Step
- 4× TI with 2.5 GS/s per Channel
- 8-bit 1.375 ps Time LSB Step
- Support >18 GHz Input

5-bit 2nd-Stage 16× Interpolation TDC

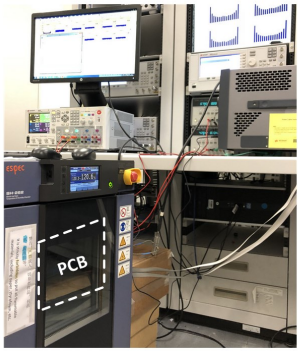


Implementation

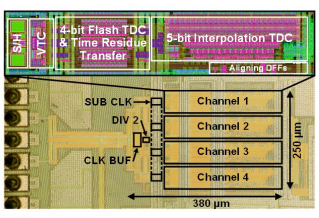
Measurement Setup



Measurement Environment & Chip Micrograph

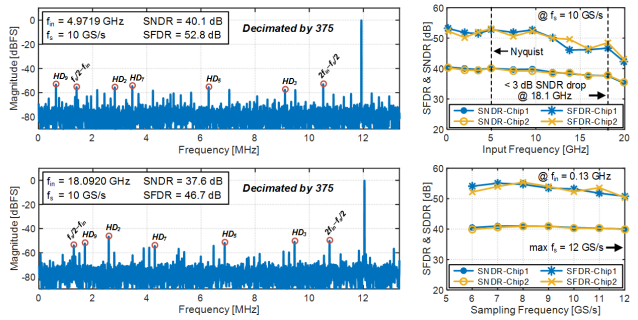


- 65 nm CMOS
- Active Area: 0.095 mm²
- Chip On Board
- Critical Bonding Length < 0.5 µm
- V&T Robustness Measurement



Verification

Measurement Results



Performance Comparison

	This Work	S. Zhu JSSC 16	M. Hassan. CICC 19	S. L. Tual ISSCC 14	L. Kull VLSI 13	Y. Frans VLSI 16
Architecture	TI Time Domain ADC			TI SAR ADC		
Technology	**65nm CMOS**	65nm CMOS	65nm CMOS	28nm SOI	32nm SOI	16nm FinFET
Resolution [bits]	**8**	6	6	6	8	8
Sampling Speed [GS/s]	**10**	10	10	10	8.8	28
Number of Channels	**4×**	4×	2×	8×	8×	32×
Supply Voltage [V]	**1.0**	1.3	1.0	1.0	1.0	0.9
Power [mW]	**50.8**	98.0	29.7	32.0	35.0	280.0
SNDR @ Nyq. [dB]	40.1	27.2	32.5	33.8	37.0	31.5
SFDR @ Nyq. [dB]	52.8	42.1	40.7	41.1	48.8	39.1
SNDR @ >Nyq. [dB]	37.6 @18.1GHz	24.6* @7.0GHz	26.0* @8.0GHz	29.7 @19.8GHz	N/A	N/A
SFDR @ >Nyq. [dB]	46.7 @18.1GHz	32.3* @7.0GHz	28.5* @8.0GHz	46.1 @19.8GHz	N/A	N/A
FOM_W [fJ/conv.-step]	61.5	523.7	86.2	80.4	68.9	325.7
FOM_S [dB]	150.0	134.3	144.8	145.7	148.0	138.5

* Estimated from the input frequency sweep results.

Acknowledgement: This work was supported by The Science and Technology Development Fund of Macau (FDCT) under Grants 093/2015/A3, 088/2016/A2 and the University of Macau under Grants MYRG2018-00146-AMSV, MYRG2019-00056-AMSV.

In ISSCC 2020 and JSSC 2021

A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5

Mo Huang, Yan Lu and Rui P. Martins

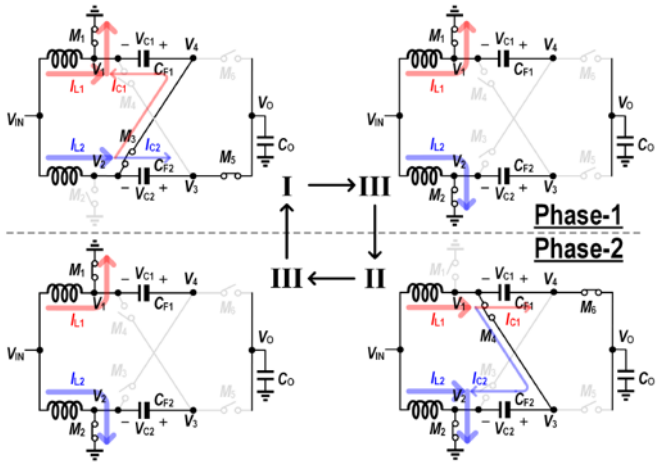
From Data and Power Conversion Innovation Center (DPIC)

Motivation

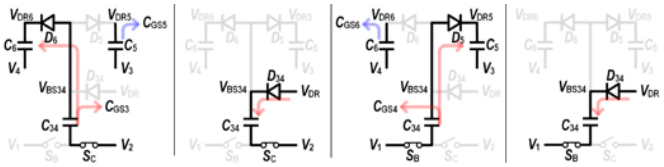
High conversion ratio (CR) boost converters are in high demand for LED backlighting in a multitude of products including smartphones and tablets. The conventional boost converter with high CR has large inductor current ripples, thus requiring high-quality inductor to mitigate the efficiency degradation. Meanwhile, a narrow switching pulse width in the high CR converters limits the switching frequency. The hybrid converter with flying capacitors can widen the pulse width for the same CR, but hard-charging has been an issue in previous works.

This article presents a monolithic two-phase, flying capacitor cross-connected boost converter that is suitable for high-CR and high-power-density applications. It simultaneously addresses the flying capacitor hard-charging, narrow pulse width, and output current ripple issues. It achieves a 93.7% peak efficiency at a conversion ratio of 4.5.

Architecture

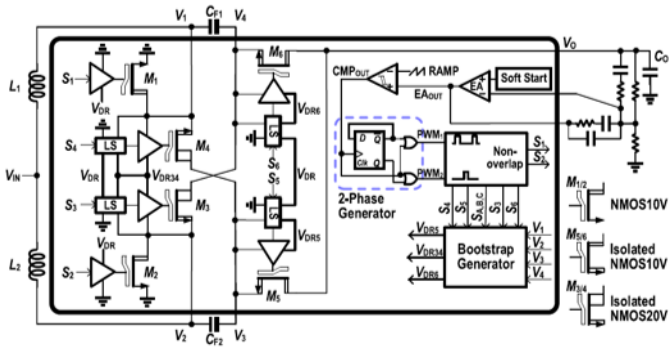


Working principle of the proposed converter

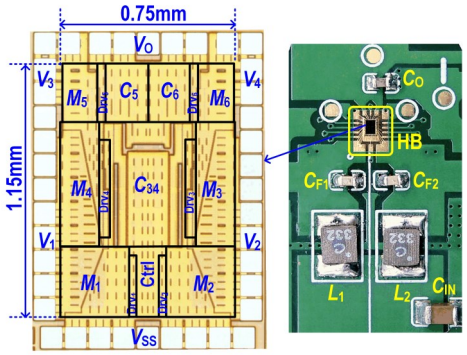


Working principle of the proposed shared bootstrap capacitor and cascade high-side gate drivers.

Implementation

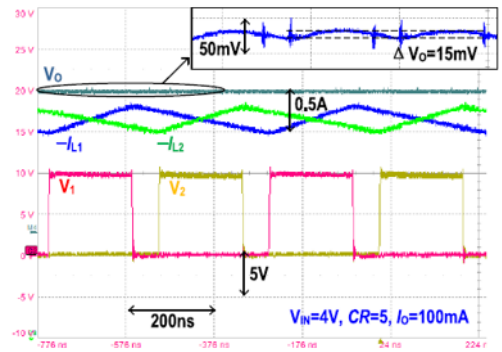


Full schematic

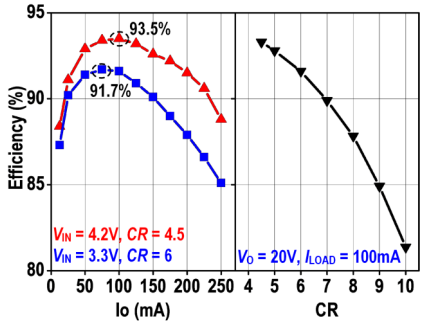


Chip and PCB photographs

Verification



Full schematic



Measured efficiencies

Acknowledgement: This work was supported in part by the Key-Area Research and Development Program of Guangdong Province under Grant 2019B010140002; in part by the Natural Science Foundation of China under Grant 61974046; in part by the Science and Technology Development Fund, Macau, SAR, under Grant 45/2019/A3 and Grant SKL-AMSV (UM)-2020-2022; and in part by the Start-up Research Grants of the University of Macau under Grant SRG2019- 00173-IME.

In TPEL 2020

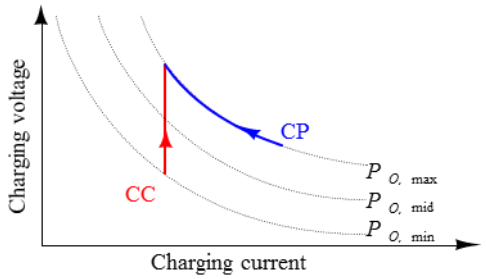
A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging

Zhicong Huang, Chi-Seng Lam, Pui-In Mak, Rui P. Martins, Siu-Chung Wong, and Chi K. Tse

From Data and Power Conversion Innovation Center (DPIC)

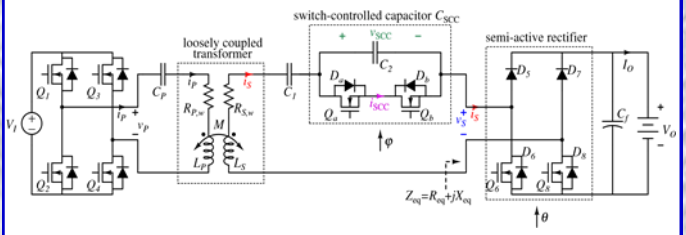
Motivation

Inductive power transfer (IPT) is a growing technology to wirelessly supply power in applications where physical connection is inconvenient or impossible. This work proposed a single-stage inductive-power-transfer (IPT) converter operating as a wireless constant-power (CP) and maximum-efficiency battery charger. By maintaining a constant output power rather than providing a constant output current throughout the dominant stage of battery charging, the IPT converter can make the utmost of its power capability, thus having faster charging rate.



V-I characteristics of CC charging and CP charging.

Architecture

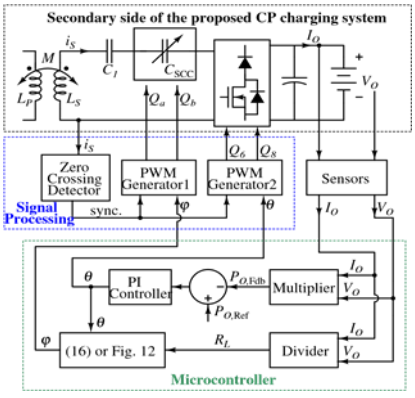


Schematics of the proposed wireless CP charging system.

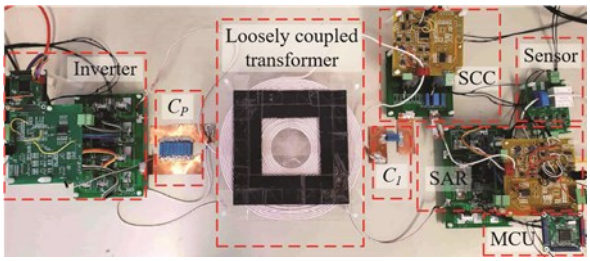
The proposed single-stage IPT converter adopts series-series compensation, and includes a switched-controlled capacitor (SCC) and a semi-active rectifier (SAR) in the secondary. The SCC and SAR aim to emulate optimum impedance of the resonator and the load in the secondary. We proposed a novel operation approach to achieve a simple solution to CP charging and maximum efficiency throughout the charging process.

The proposed fixed frequency control scheme and real-time regulation does not require wireless feedback communication. Soft switching and low voltage stress can be easily achieved.

Implementation

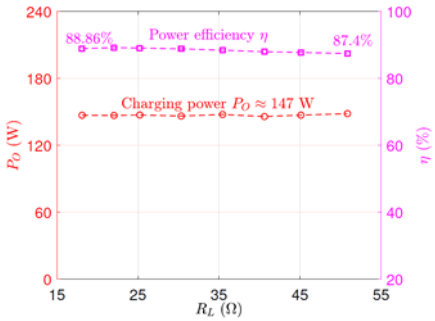


DCT conceptual operation waveforms under sleep mode.

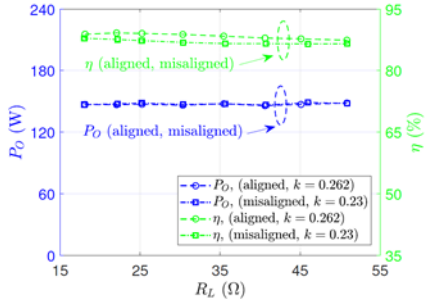


Experimental setup.

Verification



Measured power and efficiency versus battery resistance.



Validation of the proposed method under aligned and misaligned conditions.

Acknowledgement: This work was funded by The Science and Technology Development Fund, Macau SAR (FDCT) (File no. 025/2017/A1, SKL-AMSV(UM)-2020-2022) and by the University of Macau (File no. MYRG2017-00090-AMSV, UM Macao Postdoctoral Fellowship).

In A-SSCC 2019 and JSSC 2020

A VHF Wide Input Range CMOS Passive Rectifier with Active Bias Tuning

Xiaofei Li, Yan Lu and Rui P. Martins

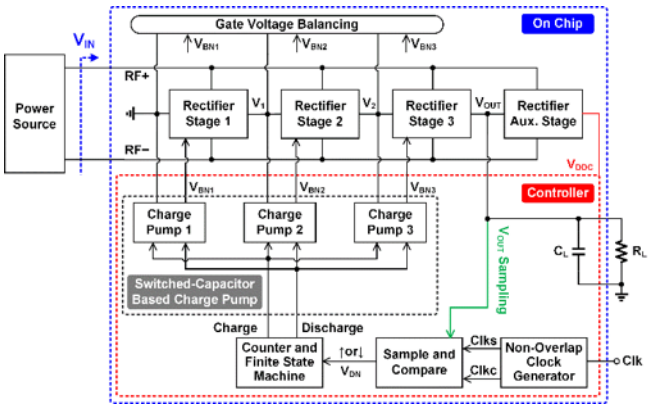
From Data and Power Conversion Innovation Center (DPIC)

Motivation

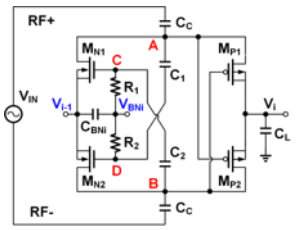
Tiny implantable medical devices in mm-size demand advanced wireless power solutions that operate at hundreds of MHz, and mainly use passive rectifiers for AC-DC power conversion. A conventional cross-connected (CC) rectifier can operate with high frequency and low input voltage, but only achieves good efficiencies in a very narrow input power range, due to the shoot-through and reverse currents.

This work presents a CMOS passive rectifier with active bias tuning (ABT), allowing a widely extended input range with high power conversion efficiency. And, we compensate the process, voltage, and temperature variations with the ABT scheme that leads to a robust design for very high frequency operation. Meanwhile, we propose a peak V_{OUT} searching scheme to indicate the charging/discharging directions for the ABT. We obtain a bias voltage balancing among stacked rectifier stages with a switched-capacitor network.

Architecture

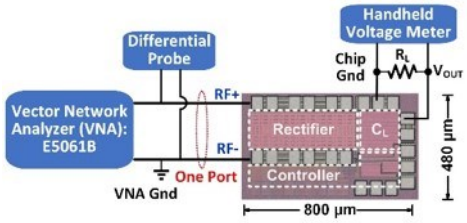


System overview of the proposed rectifier with active bias tuning.

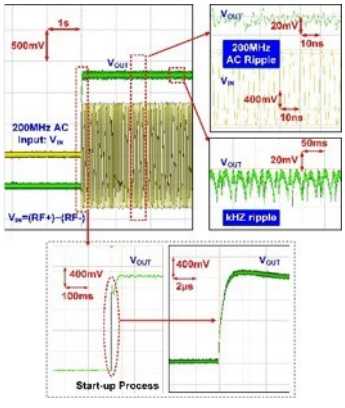


The proposed CC rectifier with VCN active bias tuning.

Implementation

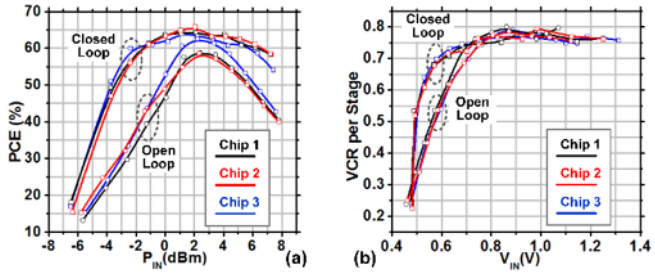


The proposed rectifier is fabricated in a 65-nm CMOS process.



Measured transient waveforms of V_{OUT} and V_{IN}, during start-up and steady state, with an input power of 2.05 dBm and R_L = 3 kΩ.

Verification



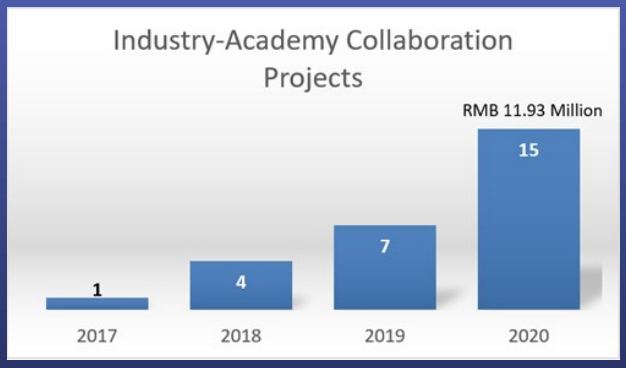
Measured (a) PCE versus input power and (b) VC.

	JSSC'17	TCAS-II'17	JSSC'17	JSSC' 17	JSSC'19	This Work
Freq. (MHz)	144	900	915	402	915	200
Process (nm)	180 SOI	65	180	180	180	65
Chip Area (mm^2)	0.078	0.084	N.A.	1.44	0.066	0.384
Rectifier Type	Active	Passive	Passive	Passive	Passive	Passive
No. of Stages	1	5	1-8	3	2-12	3
Load Cap (nF)	0.25	100	N.A.	1.1	N.A.	0.08
Load (Ω)	N. A.	147k	2k-10M	30k	10k-1M	3k
Input Power Range (dBm)	N. A.	−16 to −5	-25 to 2.5	-11 to -1	-22 to 4	−7 to 7
Max PCE	66.5%	36.5%	25%	31.9%	34.4%	64.4%

Acknowledgement: This work was supported in part by the Research Committee of University of Macau under grant MYRG2018-00102-AMSV, and Macao Science and Technology Development Fund (FDCT) SKL fund.

Technology Transfer and Commercialization Activities

In Dec. 2019, AMSV established the Hengqin branch Microelectronics Research Center (MRC) in the Zhuhai UM Research Institute (ZUMRI) and it has received 2 million RMB sponsorship from Zhuhai Government by 2020. In Jun. 2020, ZUMRI co-organized the 2nd Workshop on IC Advances in China (ICAC 2021), virtually online. More than 2500 attendees completed the registration (not including the attendees who watched the Bilibili live broadcast), among which 90% of the registered attendees are from Mainland China, 73 from Hong Kong, Macau and Taiwan, 80 from North America, 40 from Europe, and 57 from other Asian countries. Around 720 engineers from companies signed up for the conference and the Bilibili live broadcast popularity value peaked as high as 15,000. In addition, the MRC of ZUMRI participated in the Greater Bay Area IC design forum in Zhuhai, and co-organized the ISSCC 2021 China press conference (virtual).



Number of industry-Academy Projects has rapidly grown in the past three years

Zhu Hai Hi-tech Zone IC Development Forum

Macau Industrial Products Show 2020

IME explores industry-academy collaboration with chip design companies in Zhuhai

Upholding Scientific Leadership in ISSCC Benchmark in Terms of State-of-The-Art Chips

Academy in China	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	Total
University of Macau ★	2	1	1	3	2	3	6	7	8	6	2	41
HKUST	1	1	2	3	4	3	4	2	1	1		22
Tsinghua University	1			2		1			2	5	6	17
Fudan University	1	1	2	1				2	3	1		11
Chengdu UESTC								1		3	3	7
Peking University								1		1	4	6
Chinese Acad. Sci.	1		1	1							1	4
Southeast University									1	1	1	3
Shanghai Jiaotong U.									1	1		2
Zhejiang University											2	2
Tianjin University										1		1
Xi'an Jiaotong U.										1		1
Univ. of S&T of China											1	1

★★★★★★★★★★★★★★★★★★★★
Awards and Student Research Previews (PhD) in 2011 - 2020:
★★★★★★★★★★★★★★★★★★★★

1 x Far-East Best Paper Award (1st in China)
7 x SSCS Pre-Doctoral Achievement Awards
2 x ISSCC Silkroad Awards
1 x ISSCC Student Research Preview Award
15 x ISSCC Student Research Previews

★★★★★★★★★★★★★★★★★★★★

US and WO Patents Granted in 2020

1. "Flipping-Capacitor Rectifier Circuit," US Patent, US10756643B2, **August.**
2. "Apparatus and Method for On-Chip Microfluids Dispensing," US Patent, US16648009, **August.**
3. "Pipelined Analogue to Digital Converter," EUROPEAN (under review), EP 20157326.8, **July.**
4. "Single-Loop Linear-Exponential Multi-Bit Incremental Analog-to-Digital Converter," US Patent, No. 10,644,718 B1, **May.**
5. "APPAREIL ET PROCÉDÉ DE DISTRIBUTION DE MICROFLUIDES SUR PUCE" [French], WO patent, WO2020024119A1, **February.**
6. "Apparatus and Method for On-Chip Microfluids Dispensing," WO PATENT, No. WO2020024119A1, **February.**

New Academics Joined SKL AMS-VLSI in 2021

Assistant Professor

Yang Jiang received the B.Sc. degrees in electrical and electronics engineering and Ph.D. degree in electrical and computer engineering from the University of Macau (UM), Macao, China, in 2012 and 2019, respectively. He is currently an Assistant Professor at SKL AMS-VLSI.

Research Interests: Integrated Power Converters, Integrated Device Drivers, Energy Harvesting Interface.

Assistant Professor

Minglei Zhang received the B.Sc. Degrees and Ph.D. degree in microelectronics and solid-state electronics from the Tianjin University, Tianjin, China, in 2011 and Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, 2017, respectively. He is currently an Assistant Professor at SKL AMS-VLSI.

Research Interests: High-speed ADC for optical links, Time-domain integrated circuits, Mixed-signal computing.

Events and Visits

Visit by Lei Wai Nong, Secretary for Economy and Finance, Macao SAR

Visit by Ao Ieong U, Secretary for Social Affairs and Culture, Macao SAR

Visit by a Delegation from Macao Higher Education Bureau

Visit by Ma Iao Lai, Committee Member of the Chinese People's Political Consultative Conference

Visit by a Delegation from Guangzhou City Government

Visit by a Delegation from Zhongshan City Government

Visit by a Delegation from Shenzhen Association for Science and Technology

Visit by a Delegation from Guangzhou Municipal Science and Technology Bureau

Events and Visits

Professors from IME Awarded by Macao FDCT in Technological Invention

1st Prize: Enabling Internet-of-Everything (IoE) Connectivity with Advanced Electronic Chips (1st time awarded in Macao)

2nd Prize: Leading-Edge-Efficiency Data and Power Conversion Integrated Circuit Designs for Emerging Systems

Institute of Microelectronics (IME) Projects displayed at 7th Macau Industrial Products Show

Publications

Book Chapter

- *"Multiplying DLLs" Chapter 24 in "Phase-Locked Frequency Generation and Clocking: Architectures and circuits for modern wireless and wireline systems," **The Institution of Engineering and Technology - IET, UK***, **2020.**

Major IEEE Solid-State Circuits Conferences – 14 Papers in 2020 and 4 Papers in 2019

IEEE Asian Solid-State Circuits Conference (ASSCC 2020), Virtual, **Nov. 2020**
- "A 6.78-MHz Single-Stage Regulating Rectifier with Hysteretic Control and Current-Wave Modulation"
- "A 65.5-dB SNDR 8.1–11.1-nW ECG SAR ADC With Adaptive-Latching OSC-Based Comparator and DAC Calibration"
- "A Two-Phase Three-Level Buck DC–DC Converter With X-Connected Flying Capacitors for Current Balancing"

IEEE Symposium on VLSI Circuits (VLSIC 2020), Honolulu, USA, **Jun. 2020**
- "A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved 2nd-order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS"
- "A 10.4mW 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp"

IEEE Custom Integrated Circuits Conference (CICC 2020), Boston, USA, **Mar. 2020**
- "A 0.0285mm^2 0.68pJ/bit Single-Loop Full-Rate Bang-Bang CDR without Reference and Separate Frequency Detector Achieving an 8.2(Gb/s)/μs Acquisition Speed of PAM-4 data in 28nm CMOS"
- "A Power-Efficient Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Displays"

IEEE International Solid-State Circuits Conference (ISSCC 2020), San Francisco, CA, USA, **Feb. 2020**
- "A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration"
- "A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5"
- "A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation"
- "A 1.4-to-2.7GHz FDD SAW-Less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, an Isolated-BB Input and a Wideband TIA-Based PA Driver Achieving <−157.5dBc/Hz OB Noise"
- "A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input "
- "A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA"
- "A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved 2nd-order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS" **[Student Research Preview]**

IEEE Asian Solid-State Circuits Conference (ASSCC 2019), Macao SAR, China, **Nov. 2019**
- "A 200-MHz Wide Input Range CMOS Passive Rectifier with Active Bias Tunning"
- "A 0.003-mm^2 440fs$_{RMS}$-Jitter and -64dBc-Reference-Spur Ring-VCO-Based Type-I PLL Using a Current-Reuse Sampling Phase Detector in 28-nm CMOS"
- "A High DR High-Input-Impedance Programmable-Gain ECG Acquisition Interface with Non-inverting Continuous Time Sigma-Delta Modulator"
- "A 1.2V 86dB SNDR 500kHz BW Linear-Exponential Multi-Bit Incremental ADC Using Positive Feedback in 65nm CMOS"

IEEE Conferences – 10 Papers

IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2020), Vietnam, **Dec. 2020**
- "A Single-Stage Delay-Tuned Active Rectifier for Constant-Current Constant-Voltage Wireless Charging"

The 27th IEEE International Conference on Electronics Circuits and Systems (ICECS 2020), Virtual, **Nov. 2020**
- "An Implantable Photovoltaic Energy Harvesting System with Skin Optical Analysis"

IEEE International Symposium on Circuits and Systems (ISCAS 2020), Virtual, **Oct. 2020**
- "A 6.4pJ/bit Strong Physical Unclonable Function Based on Multiple-Stage Amplifier Chain"
- "Low Complexity Illumination-Invariant Motion Vector Detection Based on Logarithmic Edge Detection and Edge Difference"
- "An N × N Multiplier-Based Multi-Bit Strong PUF Using Path Delay Extraction"
- "On Fully Differential Incremental ΔΣ ADC With Initial Feedback Zeroing and 1.5-Bit Feedback"

The 46th Annual Conference of the IEEE Industrial Electronics Society (IECON 2020), Singapore, **Oct. 2020**
- "Parameter Design of Second Order Sliding Mode Controller for LC-coupling Hybrid Power Filter Based on Describing Function"
- "A Unity-Power-Factor Inductive Power Transfer Converter with Inherent CC-to-CV Transition Ability for Automated Guided Vehicle Charging"

63rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2020), Springfield, MA, USA, **Aug. 2020**
- "A 0.024-mm^2 45.4-GHz-Bandwidth Unity-Gain Output Driver with SDD$_{22}$<-10dB up to 35 GHz"

IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2020), Los Angeles, California, USA, **Aug. 2020**
- "A 0.082mm^2 24.5-to-28.3GHz Multi-LC-Tank Fully-Differential VCO Using Two Separate Single-Turn Inductors and a 1D-Tuning Capacitor Achieving 189.4dBc/Hz FOM and 200±50kHz 1/f^3 PN Corner"

SCI Journals – 70 Papers

- "A Leg Phantom Model Based on the Visible Human Data for Intra-Body Communication," ***IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology***, **Dec. 2020.**
- "An 8-Bit 10-GS/s 16× Interpolation-Based Time-Domain ADC with <1.5-ps Uncalibrated Quantization Steps," ***IEEE Journal of Solid-State Circuits***, **Dec. 2020.**
- "LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter with Ripple Calibration," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Dec. 2020.**
- "An Inertial Rotary Energy Harvester for Vibrations at Ultra-Low Frequency with High Energy Conversion Efficiency," ***Applied Energy***, **Dec. 2020.**
- "A Calibration-Free, Reference-Buffer-Free, Type-I Narrow-Pulse-Sampling PLL with -78.7-dBc REF Spur, -128.1-dBc/Hz Absolute In-Band PN and -254-dB FOM," ***IEEE Solid-State Circuits Letters***, **Dec. 2020.**
- "A Deadbeat Current Controller of LC-Hybrid Active Power Filter for Power Quality Improvement," ***IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE)***, **Dec. 2020.**
- "Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter," ***IEEE Transactions on Industrial Electronics*** , **Dec. 2020.**
- "A Multiband FDD SAW-Less Transmitter for 5G-NR Featuring a BW-Extended N-Path Filter-Modulator, a Switched-BB Input, and a Wideband TIA-Based PA Driver," ***IEEE Journal of Solid-State Circuits***, **Dec. 2020.**
- "Digital Battery Management Unit with Built-In Resistance Compensation, Modulated Frequency Detection and Multi-Mode Protection for Fast, Efficient and Safe Charging," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "A 0.5-V Supply, 36 nW Bandgap Reference with 42 ppm/°C Average Temperature Coefficient Within −40 °C to 120 °C," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "A -40°C - 125°C, 1.08 ppm/°C, 918 nW Bandgap Voltage Reference with Segmented Curvature Compensation," ***Microelectronics Journal***, **Nov. 2020.**
- "An NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28-nm CMOS," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter with Seamless Mode Selection for IoT Application," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "Near-Optimal Decoding of Incremental Delta-Sigma ADC Output," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "A 108 F²/Bit Fully Reconfigurable RRAM PUF Based on Truly Random Dynamic Entropy of Jitter Noise," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "A Comparative Study of Digital Low Dropout Regulators," ***Journal of Semiconductors***, **Nov. 2020.**
- "A 0.04% BER Strong PUF with Cell-Bias-Based CRPs Filtering and Background Offset Calibration," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "Preface to the Special Issue on Advanced Analog and Mixed-Mode Integrated Circuits," ***Journal of Semiconductors***, **Nov. 2020.**
- "A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-Only Switched-Capacitor Arrays with a 187.6-dBc/Hz FOM," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "A Calibration-Free Ring-Oscillator PLL With Gain Tracking Achieving 9% Jitter Variation Over PVT," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2020.**
- "A Switched-Capacitor Power Converter with Unequal Duty Cycle for Ripple Reduction and Efficiency Improvement," ***Elsevier Microelectronics Journal***, **Oct. 2020.**
- "A VHF Wide-Input Range CMOS Passive Rectifier with Active Bias Tuning," ***IEEE Journal of Solid-State Circuits***, **Oct. 2020.**
- "Photocatalytic Ozonation for Sea Water Decontamination," ***Journal of Water Process Engineering***, **Oct. 2020.**
- "A Novel and Robust Single-Cell Trapping Method on Digital Microfluidics," ***Bio-protocol***, **Oct. 2020.**
- "Design of Compact Dual-Band RF Rectifiers for Wireless Power Transfer and Energy Harvesting," ***IEEE Access***, **Oct. 2020.**
- "Turning On/Off Satellite Droplet Ejection for Flexible Sample Delivery on Digital Microfluidics," ***Lab on a Chip***, **Oct. 2020. [Inside Front Cover]**
- "Effects of Parasitic Resistances on Magnetically Coupled Impedance-Source Networks," ***IEEE Transactions on Power Electronics*** , **Sep. 2020.**
- "A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging," ***IEEE Transactions on Power Electronics*** , **Sep. 2020.**
- "A Two-Phase Three-Level Buck DC–DC Converter with X-Connected Flying Capacitors for Current Balancing," ***IEEE Solid-State Circuits Letters***, **Sep. 2020.**
- "Self-Powered Implantable Medical Devices: Photovoltaic Energy Harvesting Review, Advanced Healthcare Materials," ***Advanced Healthcare Materials***, **Sep. 2020.**
- "A SAR-ADC-Assisted DC-DC Buck Converter with Fast Transient Recovery," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Sep. 2020.**
- "A 65.5-dB SNDR 8.1-11.1-nW ECG SAR ADC with Adaptive-Latching OSC-Based Comparator and DAC Calibration," ***IEEE Solid-State Circuits Letters***, **Sep. 2020.**
- "Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier with Capacitor Reuse for Input Power Adaptation," ***IEEE Journal of Solid-State Circuits***, **Aug. 2020.**
- "A Single-Pin Antenna Interface RF Front-End using a Single-MOS DCO-PA and a Push-Pull LNA," ***IEEE Journal of Solid-State Circuits***, **Aug. 2020.**
- "Parallel Architecture to Accelerate Superparamagnetic Clustering Algorithm," ***Electronics Letters***, **Jul. 2020.**
- "A 5 GS/s 29 mW Interleaved SAR ADC with 48.5 dB SNDR Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications," ***IEEE Access***, **Jul. 2020.**
- "An Analog-Proportional Digital-Integral Multiloop Digital LDO with PSR Improvement and LCO Reduction," ***IEEE Journal of Solid-State Circuits***, **Jun. 2020.**
- "A 100-MHz BW 72.6-dB-SNDR CT ΔΣ Modulator Utilizing Preliminary Sampling and Quantization," ***IEEE Journal of Solid-State Circuits***, **Jun. 2020.**
- "A Multiphase Switched-Capacitor Converter for Fully Integrated AMLED Microdisplay System," ***IEEE Transactions on Power Electronics***, **Jun. 2020.**
- "A Nano-Watt Dual-Output Subthreshold CMOS Voltage Reference," ***IEEE Open Journal of Circuits and Systems***, **Jun. 2020.**
- "Photovoltaic Power Harvesting Technologies in Biomedical Implantable Devices Considering the Optimal Location," ***IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology***, **Jun. 2020.**
- "Clip-to-Release on Amplification (CRoA): A Novel DNA Amplification Enhancer On and Off Microfluidics," ***Lab on a Chip***, **Jun. 2020. [Outside Back Cover]**
- "A Fully Dynamic Multi-Mode CMOS Vision Sensor with Mixed-Signal Cooperative Motion Sensing and Object Segmentation for Adaptive Edge Computing," ***IEEE Journal of Solid-State Circuits***, **Jun. 2020.**
- "Constant-Frequency Non-Communication-Based Inductive Power Transfer Converter for Battery Charging," ***IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE)***, **Jun. 2020.**
- "A 1-V 4-mW Differential-Folded Mixer with Common-Gate Transconductor Using Multiple Feedback Achieving 18.4-dB Conversion Gain, +12.5-dBm IIP3, and 8.5 -dB NF," ***IEEE Transactions on VLSI Systems***, **May 2020.**
- "Design, Control and Comparative Analysis of an LCLC Coupling Hybrid Active Power Filter," ***IET Power Electronics***, **May 2020.**
- "A 4-μm Diameter SPAD Using Less-Doped N-Well Guard Ring in Baseline 65-nm CMOS," ***IEEE Transactions on Electron Devices***, **May 2020.**
- "Cascaded Form Sparse FIR Filter Design," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **May 2020.**
- "Design of Galvanic Coupling Intra-Body Communication Transceiver Using Direct Sequence Spread Spectrum Technology," ***IEEE Access***, **Apr. 2020.**
- "A Fully Integrated LDO with 50-mV Dropout for Power Efficiency Optimization," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Apr. 2020.**
- "A 1.6GS/s 12.2mW 7-/8-way Split Time-Interleaved SAR ADC achieving 54.2-dB SNDR with Digital Background Timing Mismatch Calibration," ***IEEE Journal of Solid-State Circuits***, **Mar. 2020. [Invited Special Issue of CICC]**
- "A 3.15-mW +16.0-dBm IIP3 22-dB CG Inductively Source Degenerated Balun-LNA Mixer with Integrated Transformer-Based Gate Inductor and IM2 Injection Technique," ***IEEE Transactions on VLSI Systems***, **Mar. 2020.**
- "Aberration-Free Aspherical In-Plane Tunable Liquid Lenses by Regulating Local Curvatures," ***Lab on a Chip***, **Mar. 2020.**
- "A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-bit CT Sturdy MASH with DAC Non-Linearity Tolerance," ***IEEE Journal of Solid-State Circuits***, **Feb. 2020.**
- "Experimental Characterization of an Embossed Capacitive Micromachined Ultrasonic Transducer Cell," ***Micromachines***, **Feb. 2020.**
- "Subtraction-Mode Switched-Capacitor Converters with Parasitic Loss Reduction," ***IEEE Transactions on Power Electronics***, **Feb. 2020.**
- "A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC with Dynamic Gm-R-Based Amplifier," ***IEEE Journal of Solid-State Circuits***, **Feb. 2020.**
- "A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC," ***IEEE Journal of Solid-State Circuits***, **Feb. 2020.**
- "A 2.4-GHz Mid-Field CMOS Wireless Power Receiver Achieving 46% Maximum PCE and 163-mW Output Power," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Feb. 2020.**
- "Rotational Electromagnetic Energy Harvester for Human Motion Application at Low Frequency," ***Applied Physics Letters***, **Feb. 2020.**
- "Analysis, Design and Control of an Integrated Three-Level Buck Converter Under DCM Operation," ***Journal of Circuits, Systems and Computers***, **Feb. 2020.**
- "A Digital Microfluidic System with 3D Microstructures for Single-Cell Culture," ***Microsystems & Nanoengineering (Nature Publishing Group)***, **Jan. 2020.**
- "Portable NMR with Parallelism," ***ACS Analytical Chemistry***, **Jan. 2020.**
- "A 0.096-mm^2 1-to-20-GHz Triple-Path Noise-Canceling Common-Gate Common-Source LNA with Complementary pMOS-nMOS Configuration," ***IEEE Transactions on Microwave Theory and Techniques***, **Jan. 2020.**
- "A 10.6-mW 26.4-GHz Dual-Loop Type-II Phase-Locked Loop Using Dynamic Frequency Detector and Phase Detector," ***IEEE Access***, **Jan. 2020.**
- "Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Jan. 2020.**
- "Nondestructive and Objective Assessment of The Vestibular Function in Rodent Models: A Review," ***Neuroscience Letter*** , **Jan. 2020.**
- "Automatic Range Adjustment of the Fluorescence Immunochromatographic Assay Based on Image Processing," ***Sensors***, **Jan. 2020.**
- "Microfluidic Immobilized Enzyme Reactors for Continuous Biocatalysis," ***Reaction Chemistry and Engineering***, **Jan. 2020.**