澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

SKL 2010DP
模拟与混合信号
超大规模集成电路
国家重点实验室
（澳门大学）
State Key Laboratory of Analog and Mixed-Signal VLSI
(University of Macau)
中华人民共和国科学技术部
The Ministry of Science and Technology of the People's Republic of China

模擬與混合信號超大規模集成電路
國家重點實驗室
State Key Laboratory of
Analog and Mixed-Signal VLSI

State Key Lab of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) Newsletter

Motto: "Locally, from (World) Quality towards (National) Quantity"

座右銘:立足本土、人才培養, 以世界級質量創建國家級規模

Year 9
No . 9

March 2020

2019 Milestones

Co-Funded by
Macao Science and Technology Development Fund (FDCT)

Events

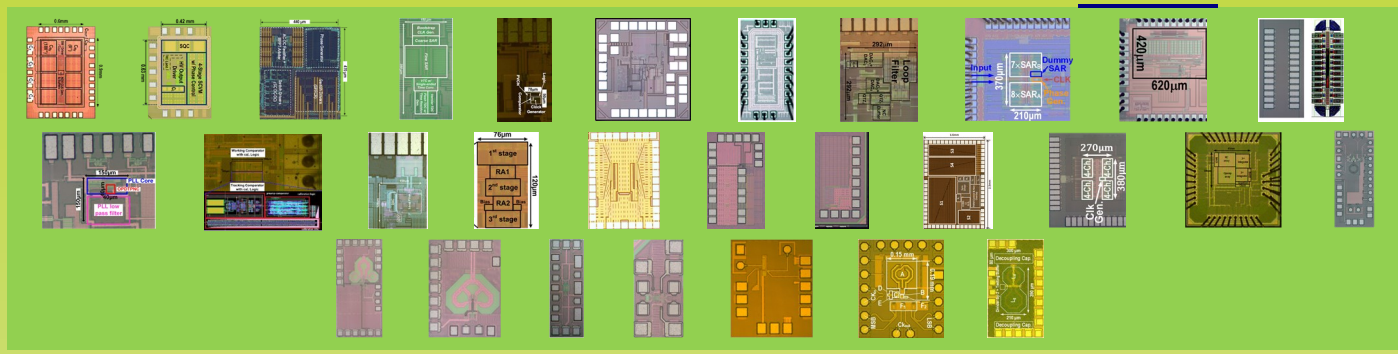
State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) co-organised the 1st Workshop on IC Advances in China (ICAC Workshop) held in Chengdu, Sichuan, China, April 10-12, 2019.

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) jointly held the "Advanced IC Summer Course" for people from the Greater Bay Area (GBA) and beyond during 2019 summer.

Institute of Microelectronics (IME) held a three-day Integrated Circuit (IC) Experience Summer Camp for Macao secondary school students during 2019 summer.

Prof. U Seng Pan and Prof. Mak Pui In received Commemorative Medals for PRC's 70th anniversary.

State-of-the-Art Chips - Designed and Tested in 2019 (29 chips)



ISSCC 2020

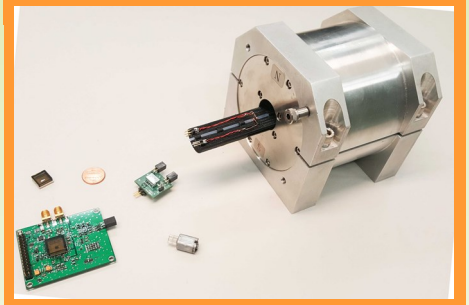
A team of faculty members and students from the SKL AMS-VLSI and ECE/FST, University of Macau (UM) published their results to the 66th IEEE International Solid-State Circuits Conference (**ISSCC**) in **February 2020** in San Francisco, CA, USA, the most competitive conference in the world in the field of chip design. However, due to the Outbreak of the New Corona Virus followed by the Declaration of Public Health Emergency of International Concern by World Health Organization, the SKL AMS-VLSI delegation was reluctantly absent from this significant event in the area this year.

This year, 6 papers/chips in areas of Data Converters, RF and Power Management were accepted at ISSCC 2020, with the following title,"A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration", "A 1.4-to-2.7GHz FDD SAW-Less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, an Isolated-BB Input and a Wideband TIA-Based PA Driver Achieving <-157.5dBc/Hz OB Noise", "A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5", "A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input", "A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation", "A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA". Besides, the SKLab PhD students received 1 Student Research Preview and Prof. Prof. Man-Kay Law originally planned to deliver a tutorial on "Capacitive Sensor Interfaces".

SKL AMS-VLSI team Stepped Up Development of Coronavirus Detection System to Tackle Epidemic Outbreak

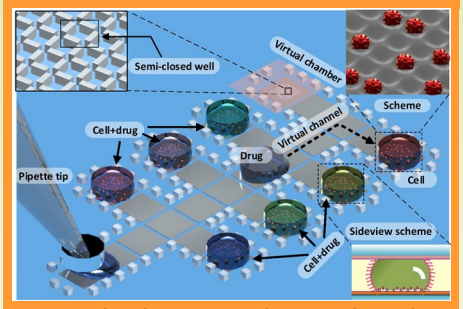
In order to speed up the detection of novel coronavirus, AMSV has stepped up the development of a digital-microfluidic-chip-based system to help tackle the epidemic outbreak. With the help of 'Virus Hunter', a rapid test kit developed with UM patented technology, the whole virus detection process can be completed within 30 minutes. The study was conducted by a team formed by researchers from UM's State Key Laboratory of Analog and Mixed-Signal VLSI (AMS-VLSI) and PhD graduates. The research team has been in touch with relevant medical units and the system will be available to frontline medical personnel upon verification.

SKL AMS-VLSI and Harvard's Collaboration Slashed Cost and Time of NMR Tests with Electronic Chips



The State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) and Harvard University have developed a portable nuclear magnetic resonance (NMR) platform by using advanced integrated circuits technology. The platform not only can significantly improve the efficiency and effectiveness of NMR tests; it can also be applied in biological diagnostic tests. For instance, conducting blood and protein tests with this platform is much cheaper and faster than using the traditional NMR testing method.

UM Researchers in Biology/Electronics Diagnosis Develop New Cancer Drug Screening Method



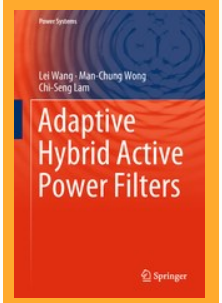
An interdisciplinary research team from the University of Macau (UM) developed a new screening method for cancer drugs. Using a digital microfluidic system, the research team can run single cell drug screening tests with a limited number of biopsy samples. As an efficient and precise method, the screening process for a cancer patient can be completed within 24 hours, which can help provide timely guidance for doctors on medication prescription. The research results have been published by the authoritative international journal Microsystems & Nanoengineering under Nature Publishing Group.

6 New PhD Graduates

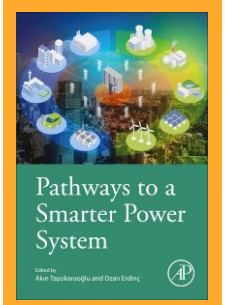
6. **Xiaofeng Yang,** *Inductor-less Low Jitter Clock Circuit Techniques and Design Considerations,* **2019**
5. **Wei Wang,** *Design of Low-Power Mega to Hundred Mega Hz Bandwidth CTDSM,* **2019**
4. **Liang Qi,** *Low-Power Cascaded Delta-Sigma Modulator for Wideband Telecommunication Applications,* **2019**
3. **Biao Wang,** *Resolution Enhancement Techniques for Multi-Bit Incremental ADC,* **2019**
2. **Shiheng Yang,** *Power-Efficient Analog and Digital Frequency Synthesizers in Nanoscale CMOS,* **2019**
1. **Haidong Yi,** *Ultra-Low-Voltage Analog and RF Circuit Techniques for Short-Range Wireless Radios in Nanoscale CMOS,* **2019**

Prof. Jia Yanwei received awards at International Multidisciplinary Conference on Optofluidics

A Book by Springer



A Joint-Chapter in a Book by Elsevier



27.3 A Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3× Energy-Extraction Improvement

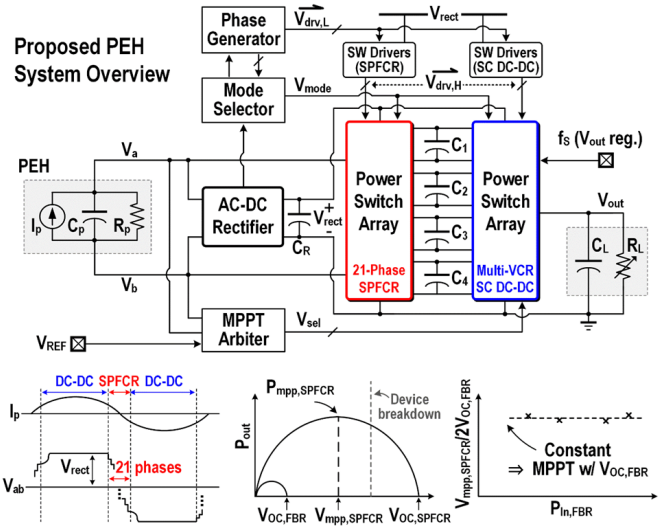
Zhiyuan Chen, Yang Jiang, Man-Kay Law, Pui-In Mak, Xiaoyang Zeng, and Rui P. Martins

From Wireless research line

Motivation

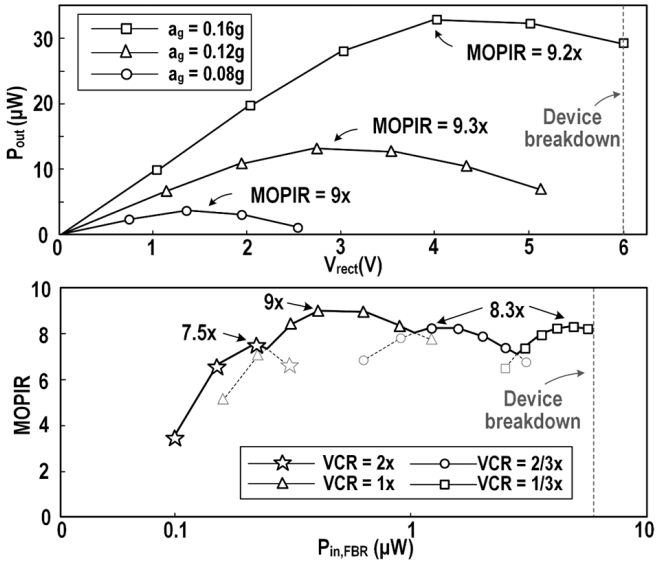
Piezoelectric energy harvesters (PEH) exhibit promising features to scavenge the ambient vibration energy for ubiquitous miniaturized Internet of Things (IoT) devices. For the traditional PEH using the full-bridge rectifier (FBR), the PEH inherent capacitance (C_p) limits the extractable AC-DC electrical power. Even though PEH interfaces employing non-linear techniques such as the parallel-synchronized-switch harvesting-on-inductor (P-SSHI) can increase the harvestable energy by extending the damping duration, they typically require bulky external high-Q inductors to enhance the extracted power. Recently, various inductor-less PEH interfaces exploiting only capacitors for flipping the PEH voltage during the zero-crossing of the PEH current (I_p) have been reported. However, their achievable energy extraction improvement highly depends on the number of flipping phases. This work proposes a split-phase flipping-capacitor rectifier (SPFCR) implementation entailing only 4 capacitors, while achieving the highest number of phases (21) when compared with the recent art. To resolve the lack of input power (P_{in}) adaptability, this work proposes a capacitor-reuse multiple voltage conversion ratio (VCR) switched-capacitor (SC) DC-DC converter to reduce the charge redistribution loss. Maximum power point tracking (MPPT) is also accomplished using the fractional FBR open circuit voltage ($V_{OC,FBR}$) for relaxed voltage tolerance, while raising the PEH extracted energy. This work demonstrates a measured 9.3x energy-extraction improvement when compared with the conventional FBR interface.

Architecture



Result I

Verification:



Result II

Performance Comparisons:

	This work	JSSC'17 [4]	JSSC'17 [2]	ISSCC'18 [3]	ISSCC'16 [1]
Technology	**0.18 μm**	0.35 μm	0.18 μm	0.18 μm HV	0.35 μm
Energy Extraction Technique	**SPFCR**	SSHC	FCR	SE-SSHC	P-SSHI
Piezoelectric Harvester	**MIDE PPA1021**	MIDE V21BL	Piezo Systems Inc. (P5A4E @ 5mm^3)	Custom MEMS	MIDE V21B & V22B
Key Component	**4 Capacitors 21 phase**	8 capacitors 17 phase	4 Capacitors 7 phase	8 Capacitors 17 phase	Inductor
MOPIR	**9.3x**	9.7x	4.83x	8.21x	6.81x
P_{in} adaptation	**Capacitor-reuse Multi-VCR SC DC-DC**	no	no	no	Shared inductor
MPPT	**yes**	no	no	no	yes
Chip Size	**0.2 mm^2**	2.9 mm^2	1.7 mm^2	5.3 mm^2	0.72 mm^2
Output Power	**0.5 to 64 μW**	161.8 μW	50.2 μW	186 μW	160.7 μW
Operating Freq.	**200Hz**	92 Hz	110 kHz	219Hz	225 Hz

In ISSCC 2019 and JSSC 2020

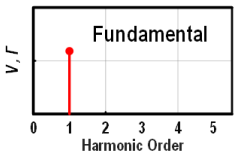
A Millimeter-Wave Multi-Resonant-RLCM-Tank VCO Exploiting a Single-Turn Multi-Tap Inductor and CM-Only Switched-Capacitor Arrays

Hao Guo, Yong Chen, Pui-In Mak, and Rui P. Martins

From Wireless research line

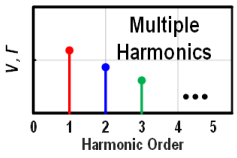
Motivation

This paper reports an area-efficient millimeter-wave VCO featuring a multi-resonant Resistor-Inductor-Capacitor-Mutual inductance (RLCM) tank to improve the phase-noise performance at low power. Specifically, we incorporate a single-turn multi-tap inductor with common-mode (CM)-only switched-capacitor arrays to generate and align the 1st, 2nd and 3rd harmonic resonances; all with high intrinsic quality factor and impedance. Prototyped in 65-nm CMOS technology, the VCO achieves a $FOM_{@1MHz}$ up to 191.6 dBc/Hz over a 16% tuning range (25.5 to 29.9 GHz), while exhibiting a low $1/f^3$ phase noise corner between 130 to 230 kHz. The die area is 0.08 mm^2.



Single-Tank LC Oscillator :

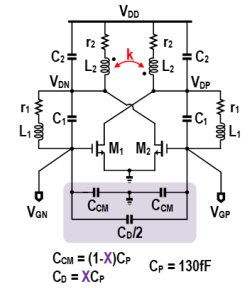
- Sinusoidal ISF, $2\Gamma^2_{rms} = 1$

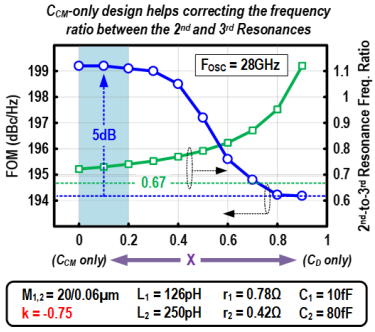


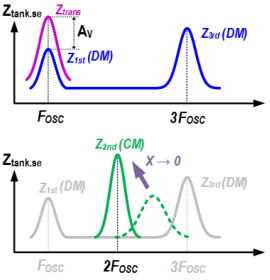
Multi-Resonant LC Oscillator :

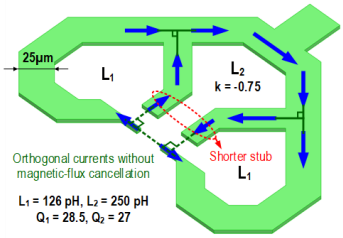
- Non-sinusoidal ISF, $2\Gamma^2_{rms} < 1$
- Flicker noise reduction by optimizing $\Gamma_{1/f,eff}$
- Potential voltage gain from drain to gate

Architecture

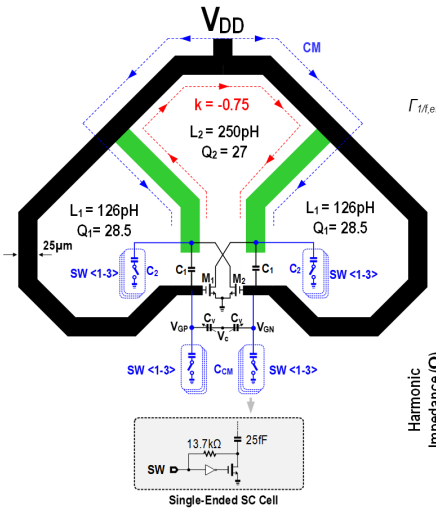








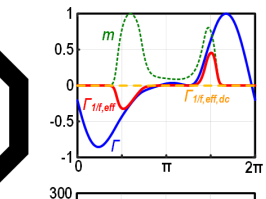
Implementation

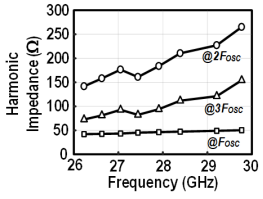


$$\Gamma(t) = \sum_i \Gamma_{H,i} \cdot \cos(i \cdot 2\pi F_{OSC} t + \varphi_i^{(i)})$$

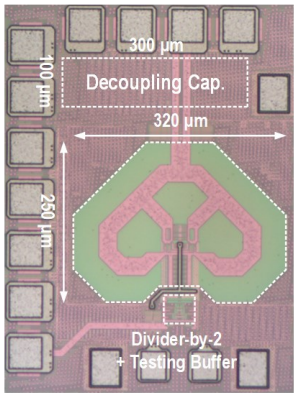
$$m(t) = \sum_i m_{H,i} \cdot \cos(i \cdot 2\pi F_{OSC} t + \varphi_m^{(i)})$$

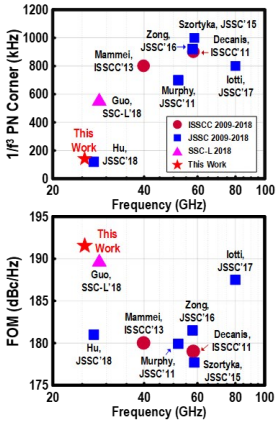
$$\Gamma_{1/f,eff,dc} = \frac{1}{2} \sum_{i=1}^{3} \Gamma_{H,i} \cdot m_{H,i} \cdot \cos(\varphi_i^{(i)} - \varphi_m^{(i)}) \approx 0$$





Verification





Parameters		This Work		JSSC'2018 [8]		SSCL'18 [17]	ISSCC'18 [14]
Key Techniques		Multi-Resonant RLCM tank: Single-Turn Multi-Tap Inductor + CM-only Tunable Capacitors		Implicit Class-F_{23} + 3rd-Harmonic Extraction		Class-F_{23A} + DM Tunable Capacitors	Class-C + Quad-Core Coupling
Supply Voltage (V)		0.48		1		0.55	3
Tuning Range (TR) (F_{min} to F_{max}GHz)		16% (25.48 to 29.92)		14% (27.3 to 31.2)		15.7% (25.2 to 29.5)	16% (11.8 to 15.6)
Output Frequency (GHz)		25.48 (12.74 *)	29.92 (14.96 *)	27.3	31.2	28.466 (14.233 *)	15
PN	@ 1MHz Δf	-115.27	-112.31	-106	-104	-114.7	-124
(dBc/Hz)	@ 10MHz Δf	-134.00	-130.77	-126	-125	-131.9	-142.6
Power Consumption P_{DC} (mW)		3.8	4	22 [&]	23 [&]	6.6	72
FOM	@ 1MHz Δf	**191.6**	**189.8**	181	180	189.59	189
(dBc/Hz)	@ 10MHz Δf	**190.3**	**188.2**	181 [&]	181 [&]	186.79	187.6
FOM_T	@ 1MHz Δf	**195.7**	**193.9**	184	183	193.51	193
(dBc/Hz)	@ 10MHz Δf	**194.4**	**192.3**	184 [&]	184 [&]	190.71	191.6
$1/f^3$ PN Corner (kHz)		**130**	**230**	120	210	550	<50
Die Area (mm^2)		0.08		0.15		0.083	1
Technology		65nm CMOS		28nm CMOS		65nm CMOS	130nm BiCMOS

FOM = |PN| + $20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{DC}/1mW)$ **FOM_T** = FOM + $20\log_{10}$(TR/10) * after on-chip divider-by-2 [&] Included the power of the first-stage O/P buffer [8]

In ISSCC 2020

A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration

Yan Song, Yan Zhu, Chi Hang Chan, Rui P. Martins

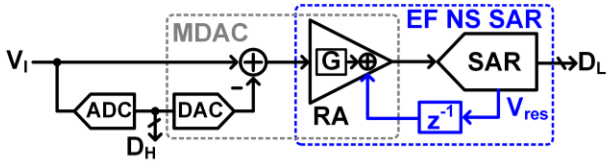
From Data Conversion and Signal Processing research line

Motivation

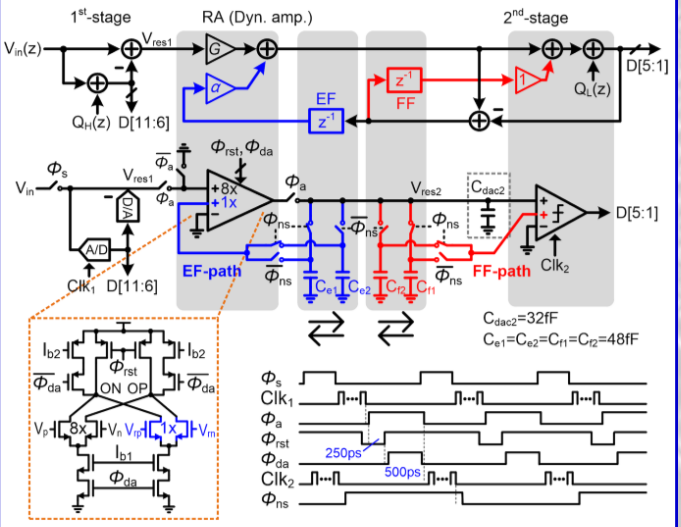
SAR-Assisted NS Pipeline ADC

High speed structure, reused RA for high power & NS efficiency

- Enhance NTF at low OSR for high speed
- Break speed bottleneck in the 1st-stage limited by the single channel structure
- Improve overall power efficiency confined by the power hungry residue amplifier
- Introduce low cost DAC mismatch, inter-stage offset, & stage-gain error calibrations with small speed penalty



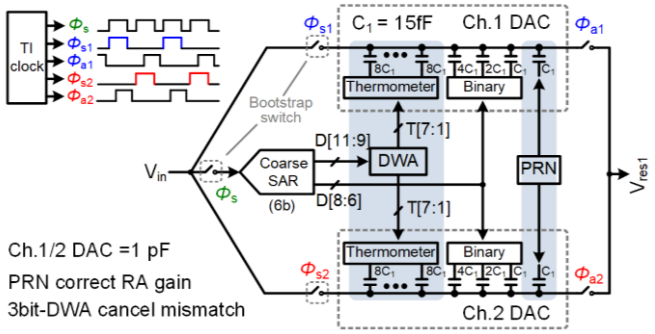
Architecture



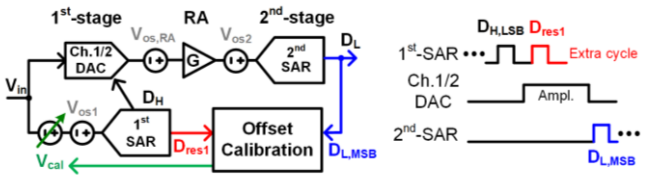
Performance Enhanced Techniques

- EF-FF NS structure
- Dynamic amplifier based RA
- Partial-interleaved 1st-stage

Implementation



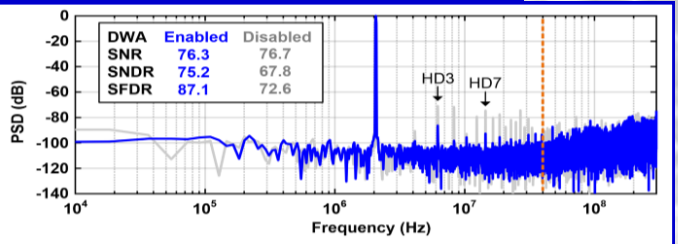
Partial-interleaving with coarse-SAR enhancing conversion speed

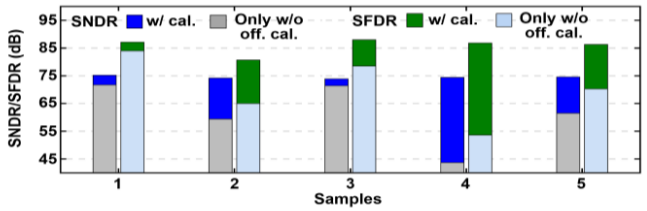


D_{res1} / $D_{L,MSB}$	0	1
0	×	V_{cal} ↑
1	V_{cal} ↓	×

Low cost inter-stage offset calibration

Verification





	ISSCC'19 Lin	ISSCC'19 Jie	VLSI'18 Song	VLSI'17 Lim	This Work
Technology [nm]	14	40	65	40	28
Architecture	PNS SAR	TI NS SAR	NS Pipe-SAR	Pipe-SAR	NS Pipe-SAR
Fs [MHz]	320	400	200	100	600
BW [MHz]	40	50	12.5	50	40
SNDR [dB]	66.6	70.4	77.1	73.2	75.2
Power [mW]	1.25	13	4.5	2.3	2.56
FoM_W [fJ/step]	8.9	48.1	30.8	6	6.8
FoM_S [dB]	171.7	166.3	171.5	176.6	177.1
Area [mm^2]	0.0021	0.061	0.014	0.068	0.016
Offset calibration	Free	Free	Off-chip	Off-chip	On-chip

In ISSCC 2019 and JSSC 2020

A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS

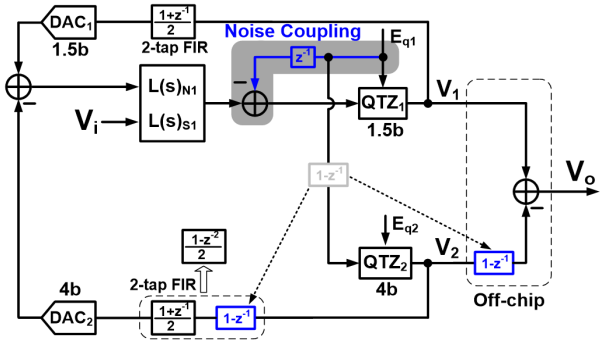
Liang Qi, Ankesh Jain, Dongyang Jiang, Sai-Weng Sin, Rui P. Martins, Maurits Ortmanns

From Data Conversion and Signal Processing research line

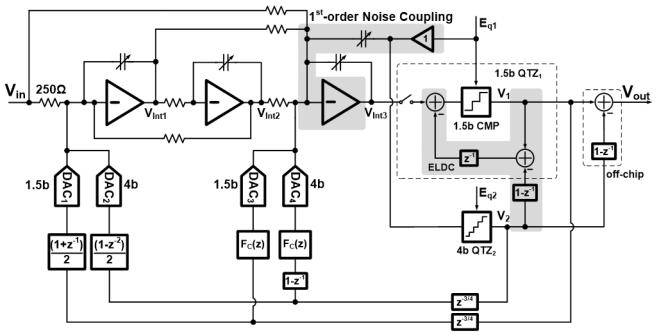
Motivation

This work presents a dual-loop noise-coupling-assisted continuous time (CT) sturdy multi-stage noise shaping (SMASH) ΔΣ modulator (DSM), employing 1.5bit/4bit quantizers, respectively. The proposed SMASH can equivalently work as an overall fourth-order DSM with 4bit internal quantization. The noise coupling applied in this CT SMASH DSM whitens the 1.5bit quantization noise and further reduces its in-band tone power, while a finite impulse response filter integrated into the outermost feedback path suppresses the out-of-band noise power of the multibit DAC input. Together, they avoid any linearization technique for the multibit DAC. Sampled at 1.2GHz, the 28nm CMOS experimental prototype measures an SNDR of 76.6dB and an SFDR of 87.9dB over a 50MHz bandwidth, consuming 29.2mW from 1.2V/1.5V supplies and occupying an active area of 0.085mm2. It exhibits a Schreier figure-of-merit (SNDR) of 168.9dB.

Architecture

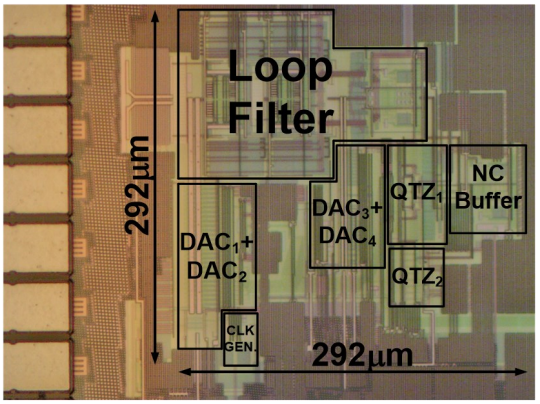


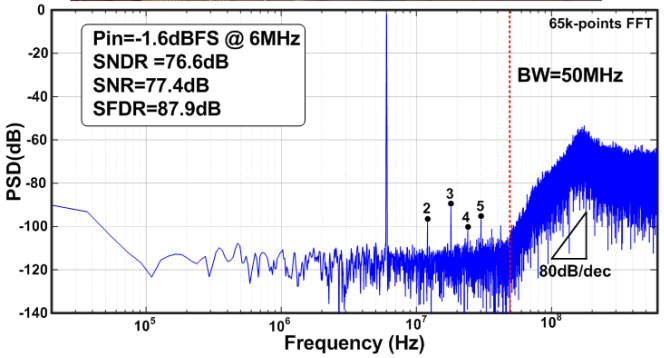
Block diagram of the proposed CT dual-loop Sturdy MASH.



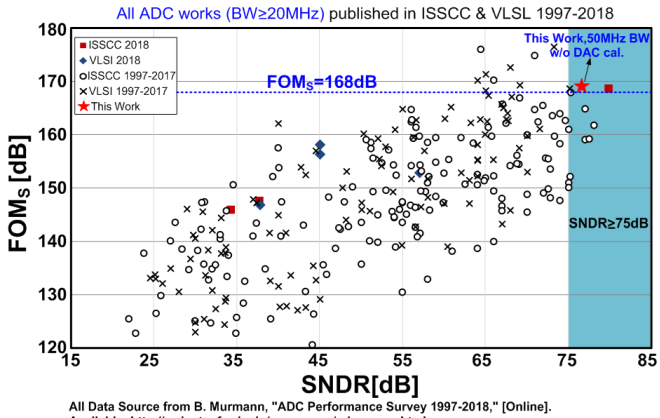
Circuit Implementation

Implementation





Verification



All Data Source from B. Murmann, "ADC Performance Survey 1997-2018," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

	This Work	ISSCC'18 He	ISSCC'17 Huang	ISSCC'16 Wu	ISSCC'15 Yoon	VLSI'15 Loeda
Architecture	**SMASH 4th-order 1.5b/4b**	Single-loop 4th-order **4b**	Single-loop 4th-order **7b**	Single-loop 6th-order **4b**	SMASH 4th-order **4b/4b**	Single-loop 4th-order **1b**
Process (nm)	**28**	28	16	65	28	40
Fs (GHz)	**1.2**	2	2.15	0.9	1.8	2.4
BW (MHz)	**50**	50	125	45	50	40
SNDR (dB)	**76.6**	79.8	71.9	75.3	74.6	66.9
SFDR (dB)	**87.9**	95.2	N/A	83	89.3	N/A
THD (dBc)	**-83.9**	-94.1	-80	-78.1	-79.9	N/A
Power (mW)	**29.2**	64.3	54	24.7	78	5.25
Area (mm^2)	**0.085**	0.25	0.217	0.16	0.34	0.02
DAC Calibration	**W/o**	**W/ on-chip**	**W/ on-chip**	**W/ off-chip**	**W/ on-chip**	**W/o**
FOM_W(fJ/conv.-step)	**52.8**	80.5	67.2	57.7	177.7	36.3
FOM_S(dB)	**168.9**	168.7	165.5	167.9	162.7	165.7

$FOM_W = P/(2*BW*2^{(SNDR-1.76)/6.02})$ $FOM_S = SNDR+10\log10(BW/P)$

In PLOS ONE 2019

Low-Latency Single Channel Real-Time Neural Spike Sorting System Based on Template Matching

Pan Ke Wang, Sio Hang Pun, Chang Hao Chen, Elizabeth A. McCullagh, Achim Klug, Anan Li, Mang I. Vai, Peng Un Mak, Tim C. Lei

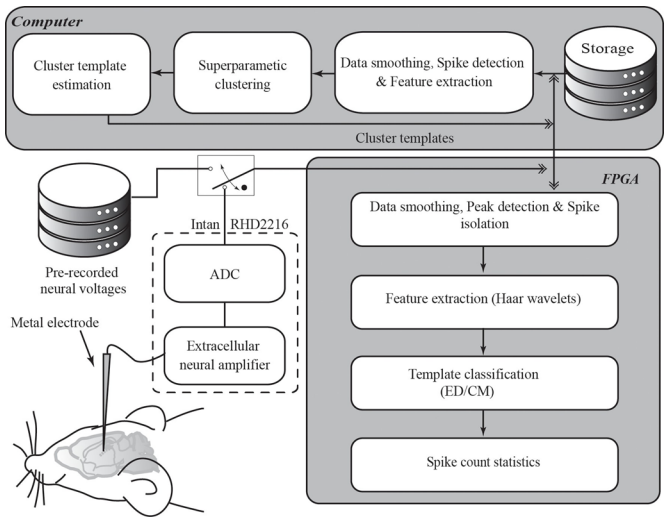
From Biomedical research line

Motivation

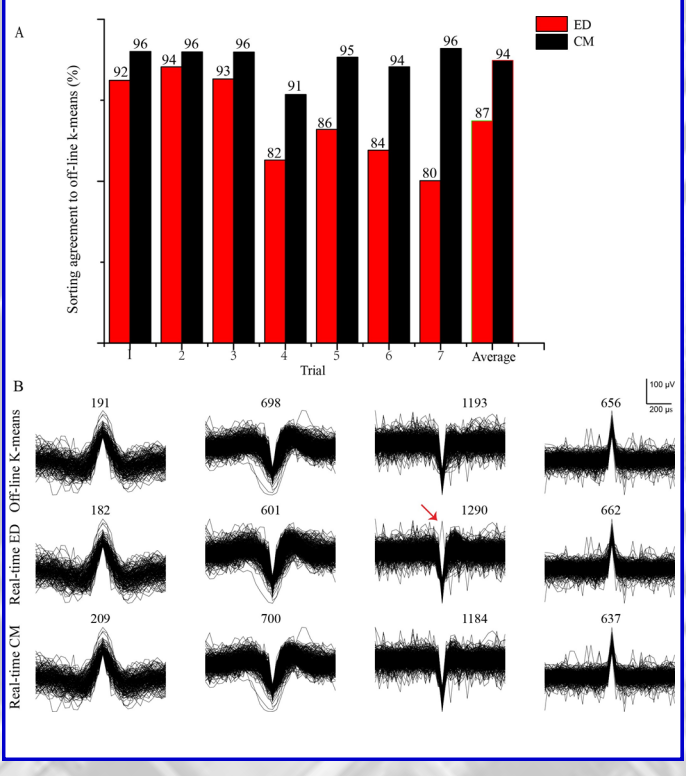
In this work, a rapid spike sorting system was developed based on template matching to rapidly calculate instantaneous firing rates for each neuron in a multi-unit extracellular recording setting. Cluster templates were first generated by a desktop computer using a non-parameter spike sorting algorithm (Super-paramagnetic clustering) and then transferred to a field-programmable gate array digital circuit for rapid sorting through template matching. Two different matching techniques–Euclidean distance (ED) and correlational matching (CM)–were compared for the accuracy of sorting and the performance of calculating firing rates.

The performance of the system was first verified using publicly available artificial data and was further confirmed with pre-recorded neural spikes from an anesthetized Mongolian gerbil. Real-time recording and sorting from an awake mouse were also conducted to confirm the system performance in a typical behavioral neuroscience experimental setting. Experimental results indicated that high sorting accuracies were achieved for both template-matching methods, but CM can better handle spikes with non-Gaussian spike distributions, making it more robust for in vivo recording. The technique was also compared to several other off-line spike sorting algorithms and the results indicated that the sorting accuracy is comparable but sorting time is significantly shorter than these other techniques. A low sorting latency of under 2 ms and a maximum spike sorting rate of 941 spikes/second have been achieved with our hybrid hardware/software system. The low sorting latency and fast sorting rate allow future system developments of neural circuit modulation through analyzing neural activities in real-time.

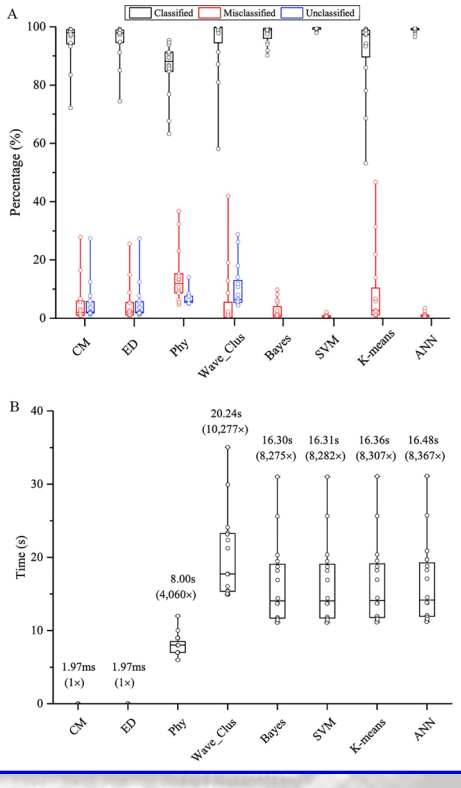
Architecture



Verification I



Verification II



In CICC 2019 and JSSC 2020

An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction

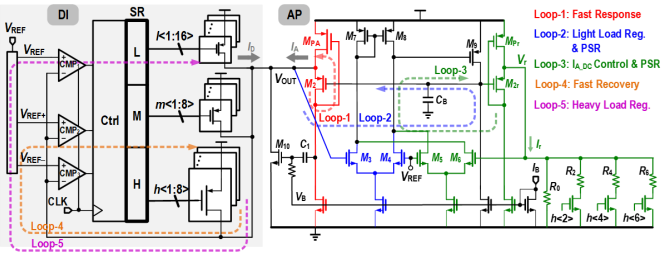
Mo Huang, Yan Lu, and Rui P. Martins

From Integrated Power research line

Motivation

In granular power management for SoCs, a low central supply is generated by a switching converter first, and then distributed to fine-grained voltage domains using low-dropout regulators (LDOs). For a high power efficiency, a small dropout voltage of LDO is needed. Moreover, power supply rejection (PSR) to the ripple up to several MHz is required. Good PSR can be achieved by analog LDO only under a high supply voltage. By contrast, digital LDO is suitable for low supply voltage, but suffers from poor PSR, slow transient response and steady-state limit cycle oscillation (LCO). This work incorporates both schemes and proposes a hybrid LDO with analog-P and digital-I controls for a fast response, improved PSR and reduced LCO at a low supply voltage.

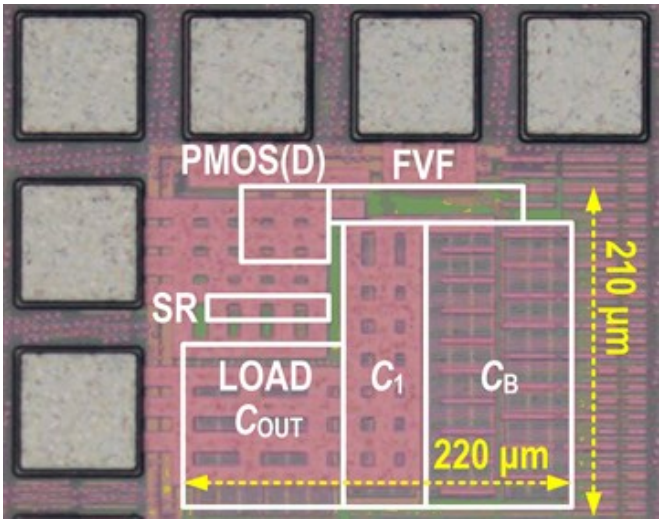
Architecture



Five-loop hybrid LDO is implemented. Loop-1 is the main analog-P path for fast response. Loop-2 is useful for light load regulation and PSR. Loop-3 is the replica loop of Loop-1 and -2 to bias Loop-1 and offer 6dB PSR improvement. Loop-4 and -5 are digital-I paths for coarse and fine tuning, respectively.

Implementation

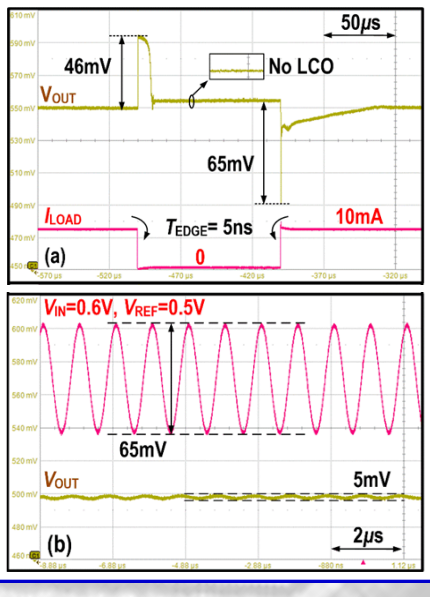
The proposed hybrid LDO was fabricated in a 65nm CMOS process.



Verification

(a) Measured transient response with the load current changing from 0 to 10mA within an edge time of 5ns. A maximum 65mV output variation is observed, and no LCO at the steady state.

(b) A −22dB measured power supply rejection (PSR) under a 65mV, 1MHz input voltage ripple.



In Sensors and Actuators B: Chemical 2019

Hydrodynamic-Flow-Enhanced Rapid Mixer for Isothermal DNA Hybridization Kinetics Analysis on Digital Microfluidics Platform

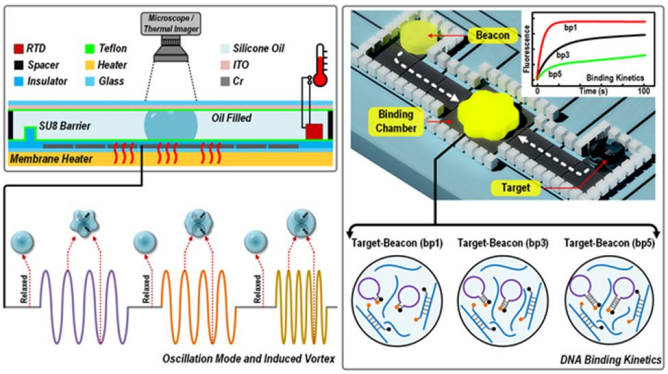
Mingzhong Li, Cheng Dong, Man-Kay Law, Yanwei Jia, Pui-In Mak and Rui P. Martins

From Multidisciplinary Research Area (Microfluidics)

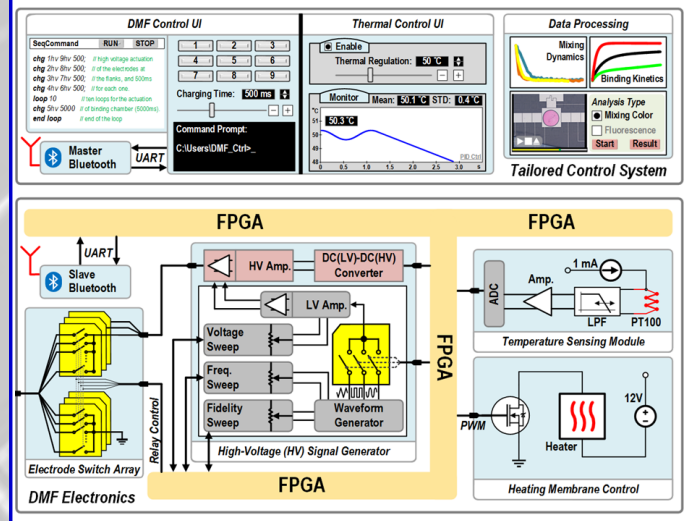
Motivation

DNA hybridization kinetics has been playing a critical role in molecular diagnostics for binding discrimination, but its study on digital microfluidic (DMF) systems is ultimately restrained by the laminar flow condition. The kinetic mixing technique is widely employed to ensure a fast reaction rate, but poses intrinsic risk in cross contamination and exhibits instable fluorescence intensity during the droplet transportation. While the electrothermal technique can provide stationary droplet mixing through the established thermal gradient within the hybridization solution, the significant increase in the droplet temperature will inevitably undermine the hybridization equilibrium and jeopardize the binding discrimination. To enhance the hybridization efficiency while ensuring a stable droplet temperature (within ±0.1°C), this paper presents a DMF platform that can perform isothermal hydrodynamic-flow-enhanced droplet mixing. Specifically, with a single electrode, droplet-boundary oscillation under a slow AC actuation is studied for improving the reaction rate. The dependencies between the mixing efficiency and the actuation voltage, actuation frequency and the spacer thickness are also systematically studied. Reliable mixing efficiency improvement is further validated over a wide range of solute concentrations. The results from real-time on-chip DNA hybridization kinetics with stationary droplets using the complete sandwiched DMF system shows that the proposed rapid mixer can achieve the same hybridization equilibrium with >13 times faster reaction rate when compared to the reference one through pure diffusion, while preventing biased hybridization kinetics as demonstrated in the electrothermal technique.

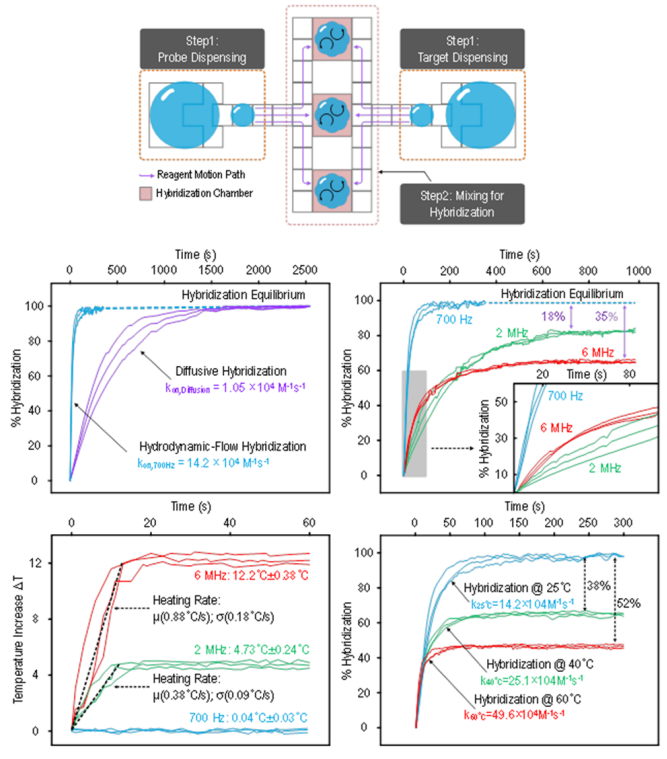
Architecture



Implementation



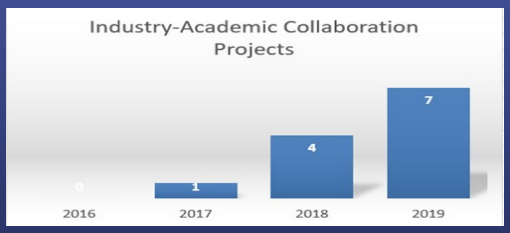
Verification



Technology Transfer Office and Commercialization Activities

China has been the largest consuming country for more than ten years. However, large increases in IC production and design within China have not immediately followed. For the purpose of deeper understanding of the interdependencies between design and production, a lot of research cooperation projects have been introduced to professors and students by Technology Transfer Office(TTO). Most of the projects are sponsored from industry. The cooperation partners are not only from Greater Bay area, but also from other China developed cities, such as Shanghai, Beijing, etc. With the high level R&D capability of SKL-ASMV, more than ten new cooperation projects will be on schedule in 2020.

A delegation from Hisilicon visited SKL AMSV to discuss



Number of industry-Academic Project has rapidly grown in past three years

Increase Guangdong-Hong Kong-Macau Greater Bay Area's Competitiveness

Macao, where land resources are limited, have greatly expanded the development space through different dimensions. One effective way is to extend cooperation and accelerate integration with the cities in Guangdong. As one of the most promising R&D design center, SKL-AMSV has organized and participated in many kinds of international forums in 2019. With good communication and organization, SKL-AMSV try to establish the bridge between academia and industry. In order to provide better service and creative environment, IME has been established in Zhuhai UM Science and Technology Research Institute as a branch. United Lab will be jointly built by university and companies in the coming year, which will continue to focus on research and innovation of new IC products.

The establishment of Guangdong-Hong Kong-Macau Semiconductor Industry Alliance, with delegations from Hong Kong, Macau, Shenzhen, Guangzhou and Zhuhai.

Seminar on Macau-Hengqin Industry-University Research Cooperation, with delegations from UM and Industry

US and International Patents Granted in 2019

1. "Palm-size μ NMR relaxometer using a digital microfluidic (DMF) device and a semiconductor transceiver for chemical/biological diagnosis," US Patent, US10436726B2, **Oct. 2019.**
2. "Reconfigurable bidirectional wireless charging transceiver," US Patent, US10256661B1, **Apr. 2019.**

Upholding Scientific Leadership in ISSCC Benchmark in Terms of State-of-The-Art Chips

Academy in China	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	Total
University of Macau ★	2	1	1	3	2	3	6	7	8	6	39
HKUST	1	1	2	3	4	3	4	2	1	1	22
Fudan Univ.	1	1	2	1				2	3	1	11
Tsinghua Univ.	1			2		1			2	5	11
Chengdu UESTC								1		3	4
Chinese Acad. Sci.	1		1	1							3
Peking Univ.								1		1	2
SJTU									1	1	2
Southeast U.									1	1	2
Tianjin University										1	1
Xi'an Jiaotong U.										1	1

★ **Awards and Student Research Previews (PhD) in 2011 - 2020:**

1 x Far-East Best Paper Award (First in China)
7 x SSCS Pre-Doctoral Achievement Awards
2 x ISSCC Silkroad Awards
1 x ISSCC Student Research Preview Award
14 x ISSCC Student Research Preview

New Academics Joined SKL AMS-VLSI in 2019

Assistant Professor

Mo Huang received the B. Sc., M. Sc., and Ph.D. degrees in microelectronics and solid-state electronics from Sun Yat-sen University, Guangzhou, China, in 2005, 2008, and 2014, respectively. He is currently an Assistant Professor at SKL AMS-VLSI.

Research Interests: Power management integrated circuits, Energy harvesting, Wireless power transfer.

Assistant Professor

Ka-Meng Lei received the B.Sc. degrees in electrical and electronics engineering and Ph.D. degree in electrical and computer engineering from the University of Macau (UM), Macao, China, in 2012 and 2016, respectively. He is currently an Assistant Professor at SKL AMS-VLSI.

Research Interests: Ultra-low-voltage analog IC design, Miniaturized nuclear magnetic resonance system, Sensors and analog front-end interfaces.

Events and Visits

Visit by a Delegation of China Ministry of Science and Technology (MOST)

Visit by a Delegation of China National Development and Reform Commission (NDRC)

Visit by a Delegation of China Academy of Science (CAS)

Visit by a Delegation of State-owned Assets Supervision and Administration Commission of the State Council (SASAC)

Distinguished Lectures and Workshops

"Biology and Reliable Detection of Human and Animal Parasitic Protozoan" by
Dr. LUN Zhao-Rong,
Professor, Sun Yat-Sen University

"Nitrided and Fluorinated Graphene for the Applications on High Mobility Graphene Transistor, Memory and Chemical Sensors" by
Prof. Chao-Sung LAI,
Professor, Dean of Engineering College of Chang Gung University

"Challenges and Designs of Domain-specific Processors; Introduction of School of Microelectronics Science and Technology of Sun Yat-sen University" by
Prof. YU Zhiyi,
Professor, Sun Yat-sen University

SKL-AMSV-IME Sports Day

Commemorative Block Stamp with SKLab Chips' Features for 20th Anniversary of The Reunification of Macao with The Motherland

Book

- *"Adaptive Hybrid Active Power Filters, Series of Power Systems,"* ***Springer*****, 2019.**

Book Chapter

- *"Pathways to a Smarter Power System,"* ***Elsevier Academic Press*****, 2019.**

SCI Journals – 40 Papers

- "A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS," ***IEEE Transactions on Circuits and Systems I: Regular Papers*****, Dec. 2019.**
- "A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques," ***IEEE Journal of Solid-State Circuits*****, Dec. 2019.**
- "CMOS Cross-Coupled Differential-Drive Rectifier in Subthreshold Operation for Ambient RF Energy Harvesting — Model and Analysis," ***IEEE Transactions on Circuits and Systems II: Express Briefs*****, Dec. 2019.**
- "Brain Rhythm Sequencing Using EEG Signals: A Case Study on Seizure Detection," ***IEEE Access*****, Nov. 2019.**
- "Algebraic Series-Parallel-Based Switched-Capacitor DC–DC Boost Converter With Wide Input Voltage Range and Enhanced Power Density," ***IEEE Journal of Solid-State Circuits*****, Nov. 2019.**
- "A -12.3 dBm Passive Sense Tag for Grid Thermal Monitoring," ***IEEE Transactions on Industrial Electronics*****, Nov. 2019.**
- "An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery," ***IEEE Journal of Solid-State Circuits*****, Oct. 2019.**
- "A 0.0071-mm² 10.8ps_{pp}-Jitter 4 to 10-Gb/s 5-Tap Current-Mode Transmitter Using a Hybrid Delay Line for Sub-1-UI Fractional De-Emphasis," ***IEEE Transactions on Circuits and Systems I: Regular Papers*****, Oct. 2019.**
- "Analysis and Verification of Jitter in Bang-Bang Clock and Data Recovery Circuit With a Second-Order Loop Filter," ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems*****, Oct. 2019.**
- "Instantaneous Power Quality Indices Detection Under Frequency Deviated Environment," ***IET Science, Measurement & Technology*****, Oct. 2019.**
- "Background Offset Calibration for Comparator Based on Temperature Drift Profile," ***IEEE Transactions on Circuits and Systems II: Express Briefs*****, Oct. 2019.**
- "Design of KY Converter with Constant On-Time Control Under DCM Operation," ***IEEE Transactions on Circuits and Systems II: Express Briefs*****, Oct. 2019.**
- "Fully Integrated High Voltage Pulse Driver Using Switched-Capacitor Voltage Multiplier and Synchronous Charge Compensation in 65-nm CMOS," ***IEEE Transactions on Circuits and Systems II: Express Briefs*****, Oct. 2019.**
- "Data-driven Distributed Optical Vibration Sensors: A Review," ***IEEE Sensors Journal*****, Sep. 2019.**
- "Continuous Artificial Synthesis of Glucose Precursor Using Enzyme-Immobilized Microfluidic Reactors," ***Nature Communications*****, Sep. 2019.**
- "Microfluiidc Immobilized Enzyme Reactors for Continuous Biocatalysis," ***Reaction Chemistry and Engineering*****, Sep. 2019.**
- "A Reconfigurable Cross-Connected Wireless- Power Transceiver for Bidirectional Device-to-Device Wireless Charging," ***IEEE Journal of Solid-State Circuits*****, Sep. 2019.**
- "A 4-b 7-μW Phase Domain ADC With Time Domain Reference Generation for Low-Power FSK/PSK Demodulation," ***IEEE Transactions on Circuits and Systems I: Regular Papers*****, Sep. 2019.**
- "A 0.0018-mm² 153% Locking-Range CML-Based Divider-by-2 with Tunable Self-Resonant Frequency Using an Auxiliary Negative-g_m Cell," ***IEEE Transactions on Circuits and Systems I: Regular Papers*****, Sep. 2019.**
- "A 0.12-mm² 1.2-to-2.4-mW 1.3-to-2.65-GHz Fractional-N Bang-Bang Digital PLL with 8-μs Settling Time for Multi-ISM-Band ULP Radios," ***IEEE Transactions on Circuits and Systems I: Regular Papers*****, Sep. 2019.**
- "Suppression of Coffee-ring Effect via Periodic Oscillation of Substrate for Ultra-sensitive Enrichment towards Surface-enhanced Raman Scattering," ***Nanoscale*****, Aug. 2019.**
- "Cell-Based Drug Screening on Microfluidics," ***Trends in Analytical Chemistry, Elsevier*****, Aug. 2019.**
- "A Reconfigurable Bidirectional Wireless Power Transceiver for Battery-to-Battery Wireless Charging," ***IEEE Transactions on Power Electronics*****, Aug. 2019.**
- "Computationally Inexpensive Enhanced Growing Neural Gas Algorithm for Real-Time Adaptive Neural Spike Clustering," ***Journal of Neural Engineering*****, Jul. 2019.**
- "A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS," ***IEEE Journal of Solid-State Circuits*****, May 2019.**
- "A Coin-Battery-Powered LDO-Free 2.4-GHz Bluetooth Low Energy/ZigBee Receiver Consuming 2mA," ***Integration, the VLSI Journal, Elsevier*****, May 2019.**
- "A 6.5x7 μm² 0.98-to-1.5 mW NonSelf-Oscillation-Mode Frequency Divider-by-2 Achieving a Single-Band Untuned Locking Range of 166.6% (4–44 GHz)," ***IEEE Solid-State Circuits Letters*****, May 2019.**
- "Hydrodynamic-Flow-Enhanced Rapid Mixer for Isothermal DNA Hybridization Kinetics Analysis on Digital Microfluidics Platform," ***Sensors and Actuators B: Chemical, Elsevier*****, May 2019.**
- "A 550-μW 20-kHz BW 100.8-dB SNDR Linear-Exponential Multi-Bit Incremental Σ Δ ADC With 256 Clock Cycles in 65-nm CMOS," ***IEEE Journal of Solid-State Circuits*****, Apr. 2019.**
- "A Comparative Study of 8-Phase Feedforward-Coupling Ring VCOs," ***IEEE Transactions on Circuits and Systems II: Express Briefs*****, Apr. 2019.**
- "A 13-bit 8-kS/s ΔΣ Readout IC Using the ZCB Integrators with an Embedded Resistive Sensor Achieving 1.05-pJ/conversion-step and 65-dB PSRR," ***IEEE Transactions on VLSI systems*****, Apr. 2019.**
- "An Analytical Model for Bandwidth Enhancement of Air-Coupled Unsealed Helmholtz Structural CMUTs," ***Journal of Sensors*****, Apr. 2019.**
- "Multi-Functional Hybrid Structure of SVC and Capacitive Grid Connected Inverter (SVC//CGCI) for Active Power Injection and Non-Active Power Compensation," ***IEEE Transactions on Industrial Electronics*****, Mar. 2019.**
- "Micro-and Nanofabrication NMR Technologies for Point-of-Care Medical Applications–A Review," ***Microelectronic Engineering, Elsevier*****, Mar. 2019.**
- "Minimizing Inverter Capacity Design and Comparative Performance Evaluation of SVC-Coupling Hybrid Active Power Filters," ***IEEE Transactions on Power Electronics*****, Feb. 2019.**
- "A 5.1-to-7.3 mW, 2.4-to-5 GHz Class-C Mode-Switching Single-Ended-Complementary VCO Achieving >190 dBc/Hz FoM," ***IEEE Transactions on Circuits and Systems II: Express Briefs*****, Feb. 2019.**
- "A 0.5-V 0.4-to-1.6-GHz 8-Phase Bootstrap Ring-VCO Using Inherent Non-Overlapping Clocks Achieving a 162.2-dBc/Hz FoM," ***IEEE Transactions on Circuits and Systems II: Express Briefs*****, Feb. 2019.**
- "Design of a High-Speed Time-Interleaved Sub-Ranging SAR ADC with Optimal Code Transfer Technique," ***IEEE Transactions on Circuits and Systems I: Regular Papers*****, Feb. 2019.**
- "Accuracy-Enhanced Variance-Based Time-Skew Calibration using SAR as Window Detector," ***IEEE Transactions on VLSI systems: Transactions Briefs*****, Feb. 2019.**
- "Low DC Voltage PV Generation System With Power Factor Correction and Harmonic Suppression Capability in a Distribution Network," ***IET Generation, Transmission & Distribution*****, Jan. 2019.**

Major IEEE Solid-State Circuits Conferences – 12 Papers

IEEE Symposium on VLSI Circuits (VLSIC), Kyoto, Japan, **Jun. 2019**

- "A 29mW 5GS/s Time-Interleaved SAR ADC Achieving 48.5dB SNDR With Fully-Digital Timing-Skew Calibration Based on Digital-Mixing"

IEEE Custom Integrated Circuits Conference (CICC), Hilton Austin, Austin, USA, **Apr. 2019**

- "A 1.6GS/s 12.2mW 7/8-way Split Time-interleaved SAR ADC with Digital Background Mismatch Calibration"
- "An Analog-Proportional Digital-Integral Multi-Loop Digital LDO with Fast Response, Improved PSR and Zero Minimum Load Current"
- "Magnetic-Tuning Millimeter-Wave CMOS Oscillators" **[Invited Paper]**

IEEE International Solid-State Circuits Conference (ISSCC 2019), San Francisco, CA, USA, **Feb. 2019**

- "A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS"
- "A Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3× Energy-Extraction Improvement"
- "A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier"
- "A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques"
- "A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM With Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ"
- "A –246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT"
- "A 25.4-to-29.5GHz 10.2mW Isolated-Sub-Sampling PLL (iSS-PLL) Achieving -252.9dB Jitter-Power FOM and -63dBc Reference Spur"
- "A 0.08mm² 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6-dBc/Hz FOM and 130kHz 1/f_3 PN Corner"
- "A 0.23-to-2.4V Input Fully Integrated Buck-Boost SC DC-DC Converter with Cell-Spliced Power Stage and Domain-Adaptives Switch Driver" **[Student Research Preview]**
- "A 550nW MEMS Readout Interface Using an Iterative-Incremental ADC Achieving Energy-Efficient Capactiance(1.2pJ/conv.-Step) and Temperature (3.6nJ%2) Sensing" **[Student Research Preview]**

IEEE Conferences – 20 Papers

2019 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), Macao, China, **Dec. 2019**

- "Self-Contained Solar-Powered Inductive Power Transfer System for Wireless Electric Vehicle Charging"

IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2019), Bangkok, Thailand, **Nov. 2019**

- "A Reconfigurable Switched-Capacitor DC-DC Converter and Cascode LDO for Dynamic Voltage Scaling and High PSR"
- "An Overview of Digital Low Drop-out Regulator Design"

2019 IEEE Vehicle Power and Propulsion Conference (VPPC), Hanoi, Vietnam, **Oct. 2019**

- "Design of Series/Series-Parallel Compensated Inductive Power Transfer Converter as Wireless Grid to Vehicle Interface"

The Second Symposium for Cell Analysis on Micro/Nanofluidics, Beijing, China, **Sep. 2019**

- "Cell-Based Drug Screening on Microfluidics, Keynote Speaker"

2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, **Sep. 2019**

- "Efficiency Optimization of Series/Series-Parallel IPT System with Load-Independent Output Voltage and Zero Input Phase Angle"

15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2019), Lausanne, Switzerland, **Jul. 2019**

- "Using EDA Tools to Push the Performance Boundaries of an Ultralow-Power IoT-VCO at 65nm"
- "The Second Symposium for Cell Analysis on Micro/Nanofluidics"
- "Cell-Based Drug Screening on Microfluidics"

2019 IEEE International Conference on Computational Intelligence and Virtual Environments for Measurement Systems and Applications (CIVEMSA), Tianjin, China, **Jun. 2019**

- "EEG-Based Emotion Recognition Under Convolutional Neural Network with Differential Entropy Feature Maps"

The 9th International Multidisciplinary Conference on Optofluidics (IMCO2019), Kowloon East, Hong Kong S.A.R., China, **Jun. 2019**

- "Electric-Controlled Precise and Flexible Sample Delivery on DMF, Oral Presentation"
- "Hairpin-Structured PCR Enhancer for Digital Microfluidic Systems, Poster Presentation"
- "Digital Microfluidics for Disease Diagnostics" **[Invited Speaker]**
- "Digital Microfluidic System for Single Cell Culture and Drug Screening, Poster Presentation"

IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Xian, China, **Jun. 2019**

- "A 0.45-V 70-nW QRS Detector Using Decimated Quadratic Spline Wavelet Transform and Window-Based Extrema Difference Techniques"
- "A Curvature Compensated BJT-Based Time-Domain Temperature Sensor With An Inaccuracy of ±0.7°C From -40°C to 125°C"
- "PID Control Considerations for Analog-Digital Hybrid Low-Dropout Regulators" **[Invited Paper]**

IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Hokkaido, Japan, **May 2019**

- "A Fast-Transient-Response Fully-Integrated Digital LDO With Adaptive Current Step Size Control"

2019 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Guangzhou, Guangdong, China, **May 2019**

- "Wideband MM-Wave CMOS VCOs - Switched Inductor, Mode-Switching Inductive Tuning, and Harmonic Extraction Techniques"

9th International IEEE EMBS Conference on Neural Engineering (NER'19), San Francisco, CA, USA, **Mar. 2019**

- "A Spiking Neural Network Model Mimicking the Olfactory Cortex for Handwritten Digit Recognition"