澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

2010DP
模拟与混合信号
超大规模集成电路
国家重点实验室
（澳门大学）
State Key Laboratory of Analog and Mixed-Signal VLSI
(University of Macau)
中华人民共和国科学技术部
The Ministry of Science and Technology of the People's Republic of China

模擬與混合信號超大規模集成電路
國家重點實驗室
State Key Laboratory of
Analog and Mixed-Signal VLSI

State Key Lab of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) Newsletter

Motto: "Locally, from (World) Quality towards (National) Quantity"

座右銘:立足本土、人才培養, 以世界級質量創建國家級規模

Year 8
No . 8

2018 Milestones

March 2019

Co-Funded by
Macao Science and Technology Development Fund (FDCT)

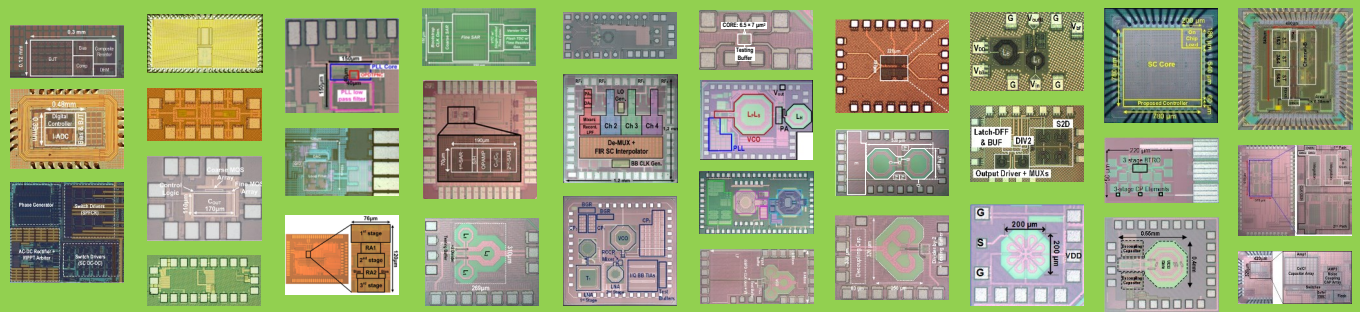
Events

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) participated in the 12th Annual Meeting of the Committee for China and Macao Cooperation in Science and Technology held in Wuhan, Hubei, China, November 14, 2018.

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) held the 3rd Academic Committee meeting on June 12, 2018.

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) signed a Memorandum of Understanding (MOU) with International Iberian Nanotechnology Laboratory (INL) from Braga, Portugal, on March 21, 2018.

State-of-the-Art Chips - Designed and Tested in 2018 (32 chips)



ISSCC 2019

A team of faculty members and students from the SKL AMS-VLSI and ECE/FST, University of Macau (UM) attended the 66th IEEE International Solid-State Circuits Conference (**ISSCC**) in **February 2019** in San Francisco, CA, USA, the most competitive conference in the world in the field of chip design.

8 papers from SKL AMS-VLSI in areas of Data Converters, RF and Power Management were accepted and presented at ISSCC 2019, ranking the university second in the world in microelectronics research, along with the University of Michigan - Ann Arbor, next only to Intel. This shows the international recognition of UM and its leading position in the field in Asia. Besides, the SKLab PhD students received 1 Predoctoral Achievement Award, 1 Student Research Preview Award, 2 Student Research Previews and 1 onsite demonstration. In addition, Prof. Pui-In Mak received his IEEE fellow certificate at the conference, for his contributions to the fields of radio frequency and analog circuits. He is the first native of Macao to receive such prestigious honor.

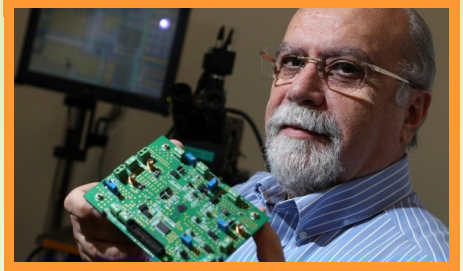
Pui-In Mak Becomes the 1st Macao Native Elected IEEE Fellow

The Institute of Electrical and Electronics Engineers (IEEE) has released its 2019 fellow list. Prof. Pui-In Mak from State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) has made the list, *for his contributions to the fields of radio frequency and analog circuits*. He is the first native of Macao to receive this prestigious honor. The 2019 list includes 295 new fellows, 30 of whom are scientists from China. Prof. Mak belongs to the youngest category (in the 31-39 age bracket), which is a very rare accomplishment.

Pui-In Mak Appointed by the Chinese Academy of Sciences as Overseas Expert

Pui-In Mak, Associate Director (research) of the University of Macau (UM) State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI), who is also a professor in the Department of Electrical and Computer Engineering, Faculty of Science and Technology, attended an event for participants in the 100 and the 1,000 Experts Programs held in Beijing last year. During the event, he was appointed a member of the overseas expert panel of the Chinese Academy of Sciences (CAS).

Macau, 'Las Vegas of Asia', Trades in Casino Chips for Microchips as Part of China's Tech Ambitions



"Macau is best known for its casino chips, now it is also known for its electronics chips," said Rui P. Martins, the vice-rector for research at the University of Macau, which plays host to the city's two State Key Laboratories – institutes that China relies on to conduct scientific research crucial to national development. "We hope with this system, with some time, the know-how will be in China … In 10 years' time, probably you don't need to import from the United States," Martins believes that in time, Macau could change the balance of power between China and the US. SKL AMS-VLSI has been one of the Asian institutions with the most inventions at the IEEE ISSCC, also known as the "Chips Olympics", in San Francisco.

— in HK SCMP, 16 Jun, 2018

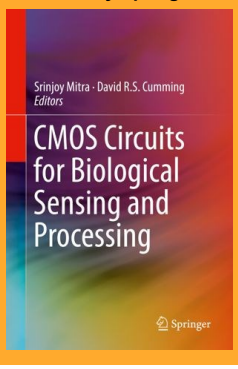
6 New PhD Graduates

6. **Yang Jiang**, *Design of Fully Integrated Fine-Grained Switched-Capacitor DC-DC Topologies in Bulk CMOS*, **Jan. 2019**.
5. **Liu Jianwei**, *Design Techniques for Energy Efficient ADCs*, **Jan. 2019**.
4. **Xing Dezhi**, *Advanced Techniques in Analog to Digital Converters*, **Jan. 2019**.
3. **Da Feng**, *Polyphase Decomposition for Sigma-Delta A/D Converters*, **Aug. 2018**.
2. **Tantan Zhang**, *Nano-Watt Class CMOS Interface Circuits for Wireless Sensor Nodes*, **Jun. 2018**.
1. **Zhiyuan Chen**, *Efficient Power Management Design for Energy Harvesting Biomedical Applications*, **Apr. 2018**.

Pui-In Mak Appointed as Associate Editor of the IEEE Journal of Solid-State Circuits

Man-Kay Law Selected as IEEE CASS Distinguished Lecturer 2019-2020

A Joint-Chapter with University of Harvard in a Book by Springer



Selected works from each research line

In ISSCC 2018 and Invited JSSC 2018

An Inverse-Class-F CMOS VCO with Intrinsic-High-Q 1st- and 2nd-Harmonic Resonances for 1/f^2-to-1/f^3 Phase-Noise Suppression Achieving 196.2dBc/Hz FOM

Chee-Cheow Lim, Jun Yin, Pui-In Mak, Harikrishnan Ramiah, and Rui P. Martins

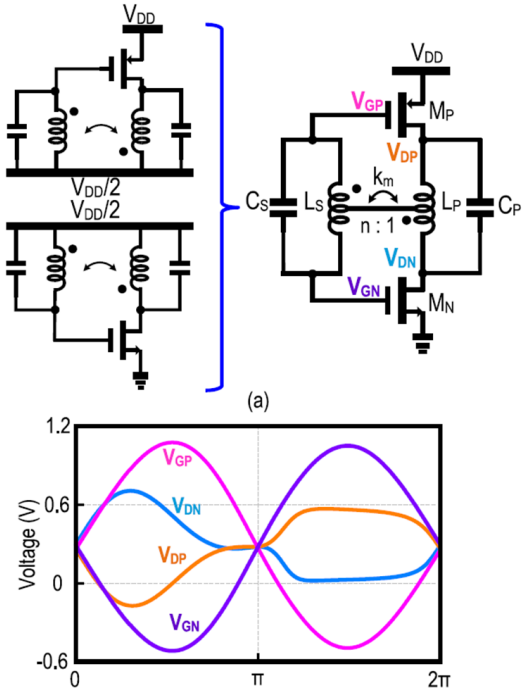
From Wireless research line

Motivation

This work is an inverse-class-F (class-F^{-1}) CMOS oscillator. It features: 1) a single-ended PMOS-NMOS-complementary architecture to generate the differential outputs and 2) a transformer-based two-port resonator to boost the drain-to-gate voltage gain (AV) while creating two intrinsic-high-Q impedance peaks at the fundamental (f_{LO}) and double ($2f_{LO}$) oscillation frequencies. The enlarged second harmonic voltage extends the flat span in which the impulse sensitivity function (ISF) is minimum, and the amplified gate voltage swing reduces the current commutation time, thereby lowering the –gm transistor's noise-to-phase noise (PN) conversion. Prototyped in 65-nm CMOS, the class-F^{-1} oscillator at 4 GHz exhibits a PN of –144.8 dBc/Hz at a 10-MHz offset, while offering a tuning range of 3.5–4.5 GHz. The corresponding figure of merit (FoM) is 196.1 dBc/Hz, and the die area is 0.14 mm^2.

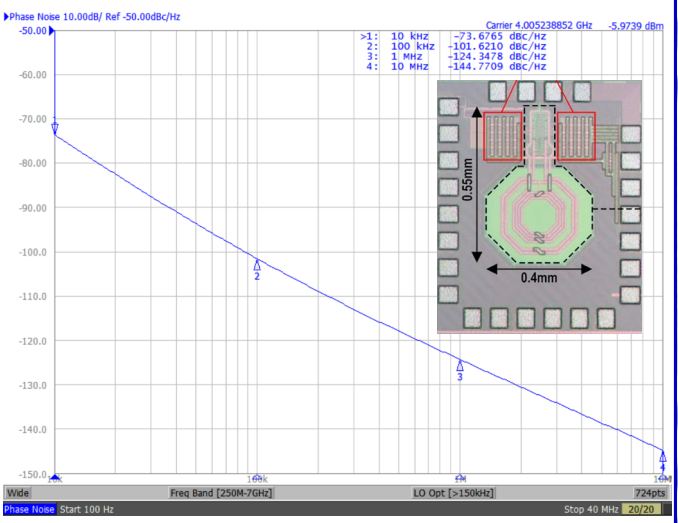
Architecture

VCO Topology and Key Waveforms



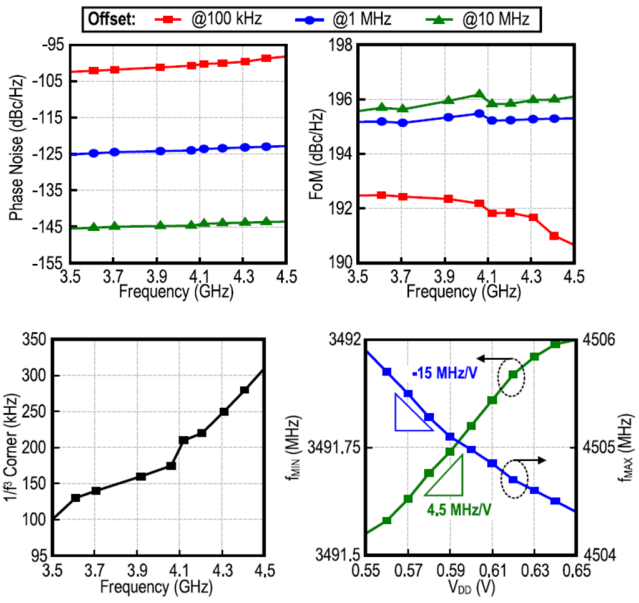
Implementation

Chip Photo and Measurement Results



Verification

Key Measured Performances



In ISSCC 2018 and Invited JSSC 2018

A 0.22-to-2.4V-Input Fine-Grained Fully Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Achieving 84.1% Peak Efficiency at 13.2mW/mm^2

Yang Jiang, Man-Kay Law, Pui-In Mak, and Rui P. Martins

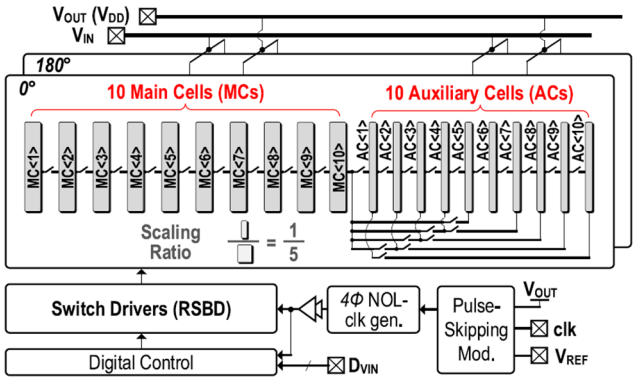
From Wireless research line

Motivation

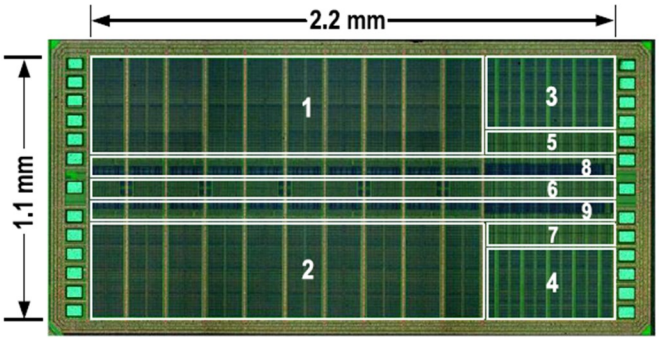
This work proposes an algorithmic voltage-feed-in (AVFI) topology capable of systematic generation of any arbitrary buck–boost rational ratio with optimal conduction loss while achieving reduced topology-level parasitic loss among the state-of-the-art works. By disengaging the existing topology -level restrictions, we develop a cell-level implementation using the extracted Dickson cell (DSC) and charge-path-folding cell (QFC) to minimize the power-stage parasitic loss, exhibiting a Dickson-like switching pattern. The proposed partitionable main cell (MC) and auxiliary cell (AC) architecture achieves fined-grained voltage conversion ratio (FVCR) reconfiguration with optimal power cell utilization and reduced control complexity. Implemented in 65-nm bulk CMOS, the fully integrated switched-capacitor power converter (SCPC) using 10 MCs and 10 ACs executes a total of 24 VCRs (11 buck and 13 boost) with wide-range efficient buck–boost operations through the proposed reference-selective bootstrapping driver (RSBD). Based on the AVFI topology, the chip prototype reaches a measured peak efficiency of 84.1% at a power density of 13.4 mW/mm^2 over a wide range of input (0.22–2.4 V) and output (0.85–1.2 V).

Architecture

Architecture of the Proposed Buck-Boost SC DC-DC Converter



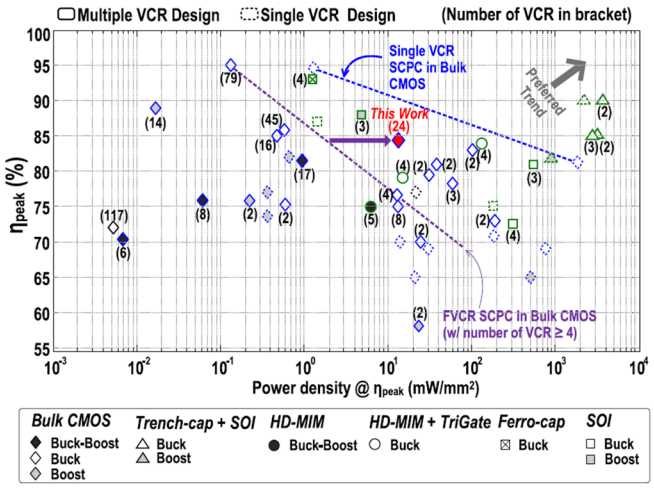
Implementation



1~2) 10 MCs in 0° and 180°
3~4) 10 ACs in 0° and 180°
5~7) RSBDs + digital control
8~9) Power switches

Result

State-of-the-Art Comparison



In ISSCC 2019

A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques

Minglei Zhang, Chi-Hang Chan, Yan Zhu, Rui P. Martins

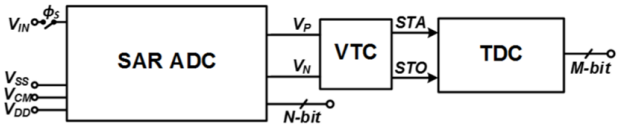
From Data Conversion and Signal Processing research line

Motivation

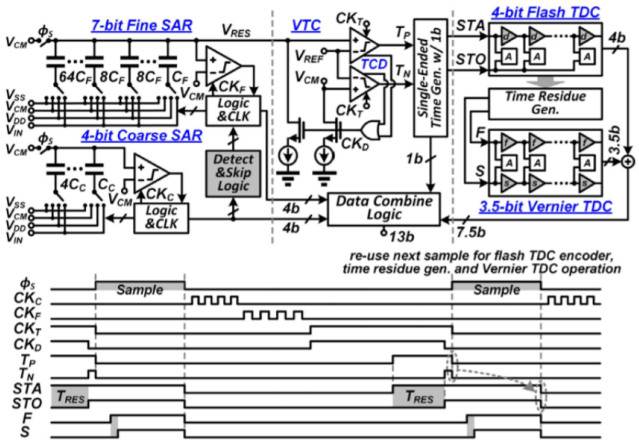
Two-Step TDC-Assisted SAR ADC

High speed & resolution, low power and small calibration effort @ low V_{DD}

- Reduce PVT sensitivity due to VTC and time-domain operation
- Improve SAR speed and CDAC switching linearity while avoiding calibration
- Keep large bits for high resolution but reduce number of delay cells for high speed and low power, and avoid complex calibration



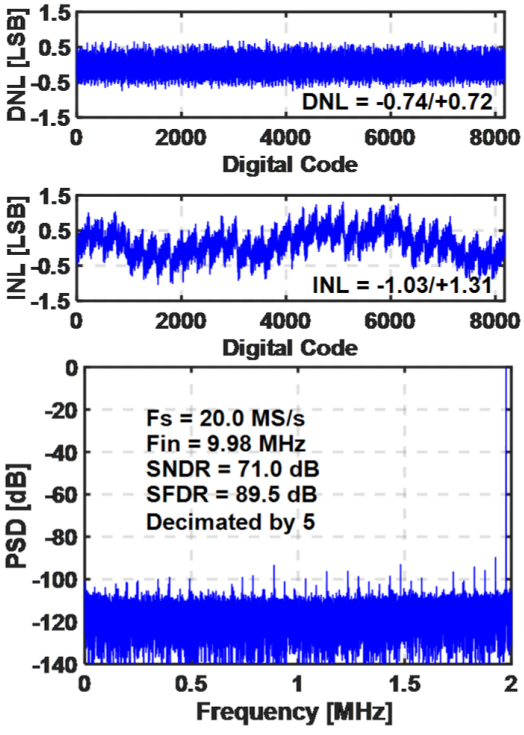
Architecture



Speed Enhanced Techniques

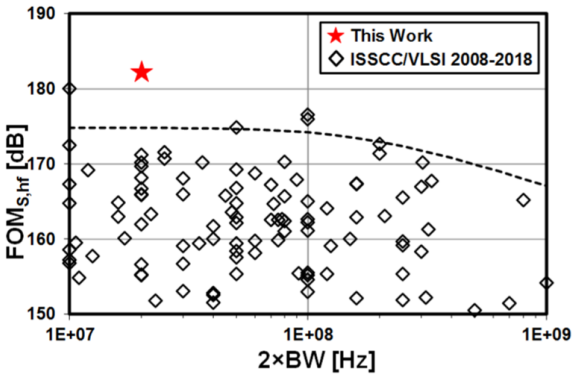
- Subranging SAR ADC
- High-speed VTC
- Two-step TDC
- TDC period extension

Implementation



Verification

ADC: SNDR > 60dB & BW > 5MHz



	This Work	[1] JSSC16	[2] ISSCC15	[3] ISSCC15	[4] VLSI16
Architecture	SAR-TDC	SAR-TDC	Pipe-SAR	SAR	SAR-VCO
Technology	65nm	90nm	65nm	40nm	40nm
Resolution [bits]	13	10	13	13	-
Active Area [mm²]	0.053	0.041	0.054	0.068	0.030
Power Supply [V]	0.6	0.6	1.2	1.0	1.1
Sample Rate or 2×BW[MS/s]	20	2	50	6.4	6
SNDR @ Nyq. [dB]	71.0	54.5	70.9	64.1	71.4
SFDR @ Nyq. [dB]	89.5	82.3	84.6	81.9	-
Total Power [μW]	82	4.6	1000	46	350
FoM_W @ Nyq. [fJ/conv.step]	1.4	4.0	7.0	5.5	18.5
FoM_S @ Nyq. [dB]	181.9	167.9	174.9	172.5	170.7

In VLSI 2018 and JSSC 2019

A 550mW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental SD ADC with 256 clock cycles in 65nm CMOS

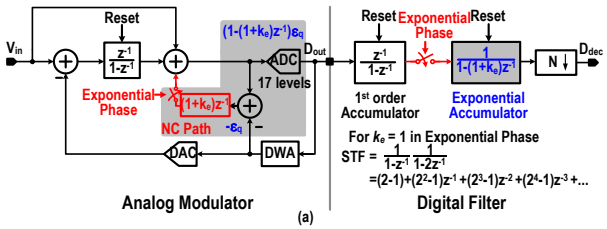
Biao Wang, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, Rui P. Martins

From Data Conversion and Signal Processing research line

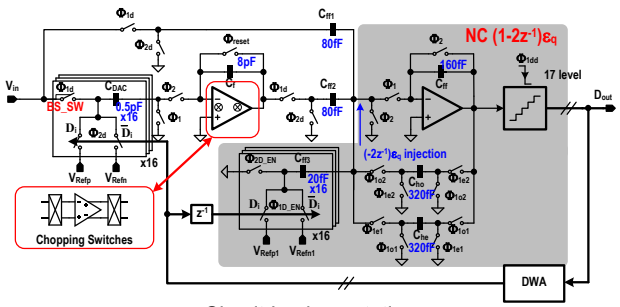
Motivation

This work presents an incremental analog-to-digital converter (IADC) with a two-phase linear-exponential accumulation loop. In the linear phase, the loop works as a first-order structure. The noise-coupling path is then enabled in the exponential phase thus boosting the SQNR exponentially with a few number of clock cycles. The two-phase scheme combines the advantages of the thermal noise suppression in the 1st-order IADC and SQNR boosting in the exponential mode. The uniform-exponential weight function allows the data weighted averaging (DWA) technique to work well, leading to the rotation of the multi-bit DAC mismatch error. Meanwhile, this scheme does not destroy the notches, which can be utilized to suppress the line noise. Implemented in 65nm CMOS under 1.2V supply, the ADC achieves an SNDR/DR of 100.8dB/101.8dB with 20kHz BW, 550μW & 0.134mm^2, resulting in Walden/Schreier FoM$_W$/FoM$_S$ of 153fJ/176.4dB, respectively. The differential and integral nonlinearities are +0.27/-0.27 and +0.84/-0.81 LSBs, respectively.

Architecture

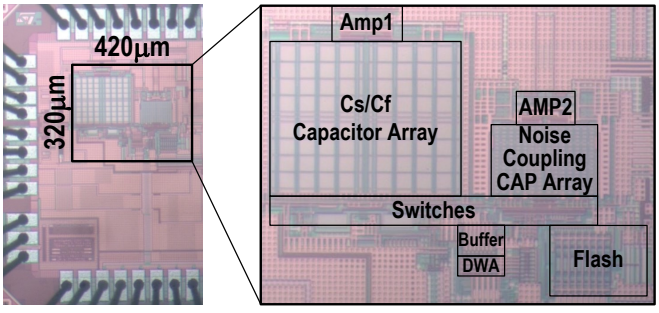


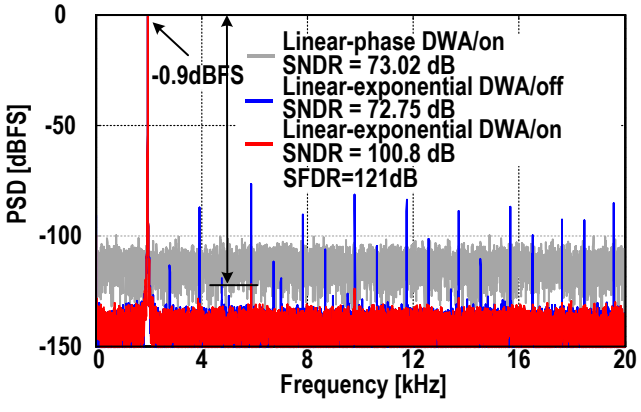
Proposed Linear-Exponential Multi-Bit Incremental ADC and its timing



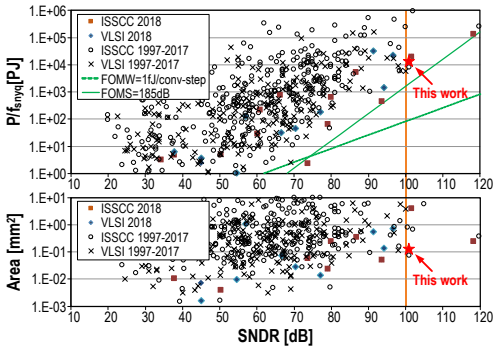
Circuit Implementation

Implementation





Verification



Data Source from B. Murmann, "ADC Performance Survey 1997-2018," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

	This Work	ISSCC 18	JSSC 15	JSSC 17	ISSCC 18	VLSI 17	ISSCC 16
Architecture	Linear-exponential Incremental	3rd-order Incremental	Two-step Incremental	Multi-step Incremental	Zoom ADC	Pipelined-SAR	Oversampling SAR
Process	**65nm**	180nm	65nm	180nm	160nm	180nm	55nm
Supply	**1.2V**	3V	1.2V	1.5V	1.8V	1.8V/5V	1.2V
Fs	**10.24MHz**	30MHz	192kHz	642kHz	2MHz	2MHz	1MHz
Bandwidth	**20kHz**	100kHz	250Hz	1kHz	1kHz	1MHz	1kHz
Power	**550μW**	1.098mW	10.7μW	34.6μW	0.28mW	11.35mW	15.7μW
Peak SNDR	**100.8dB**	86.6dB	90.8dB	96.8dB	118.1	99.2dB	101dB
Dynamic Range	**101.8dB**	91.5	99.8dB	99.7dB	120.3	100.5dB	N/A
FoM$_W$(pJ/conv.)#	**0.153**	0.314	0.76	0.32	0.21	0.07	0.0856
FoM$_S$(dB)#	**176.4**	166.2	164.5	171.4	183.6	178.7	179
Area [mm^2]	**0.134**	0.36	0.2	0.5	0.25	3.87	0.072

FoM$_W$ = Power/(2^{ENOB}*2*BW) ; FoM$_S$ = SNDR+10log$_{10}$(BW/Power)

In IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control 2018
[Editor's Selection of Articles — December 2018]

Monolithic Multiband CMUTs for Photoacoustic Computed Tomography With In Vivo Biological Tissue Imaging

Sio Hang Pun, Yuanyu Yu, Jian Zhang, Jiujiang Wang, Ching-Hsiang Cheng, Kin Fong Lei, Zhen Yuan and Peng Un Mak

From Biomedical research line

Motivation

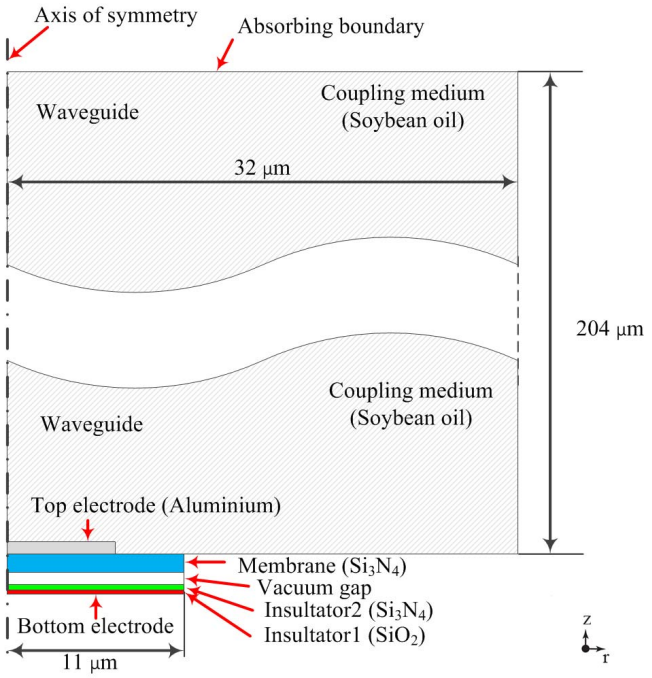
In this paper, a monolithic multiband capacitive micromachined ultrasonic transducer (CMUT) array was designed and fabricated for the reception of the wideband PA signals so as to provide high-resolution images with high-frequency CMUT arrays and present the high signal-to-noise-ratio major structure with low-frequency CMUT arrays.

To demonstrate its performance, a phantom experiment was conducted to show and evaluate the various qualities of multiresolution images.

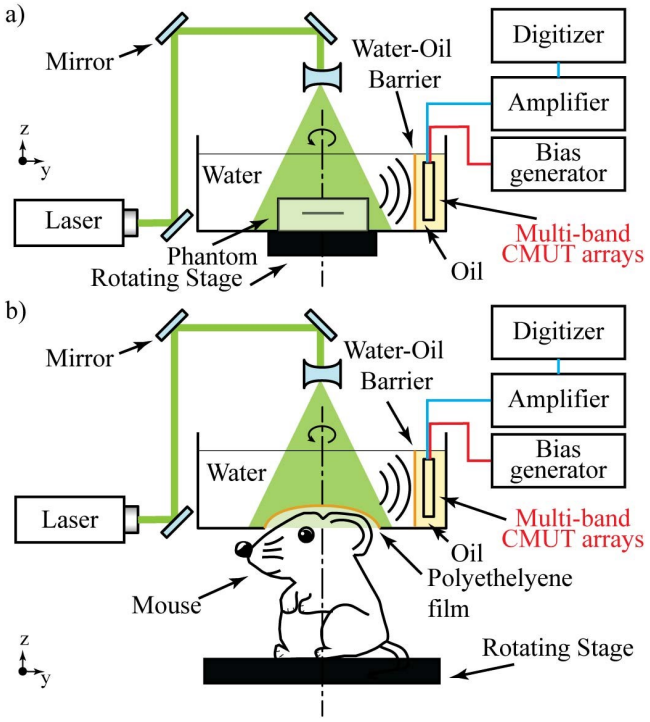
In addition, an in vivo mouse model experiment was also carried out for revealing the multiscale PA imaging capability with the multiband CMUTs on biological tissues. From the obtained results, the images from different CMUT arrays could show the structures of the mouse brain in different scales.

In addition, the images from the high-frequency CMUT arrays were able to reveal the major blood vasculatures, whereas the images from low-frequency CMUT arrays showed the gross macroscopic anatomy of the brain with higher contrast.

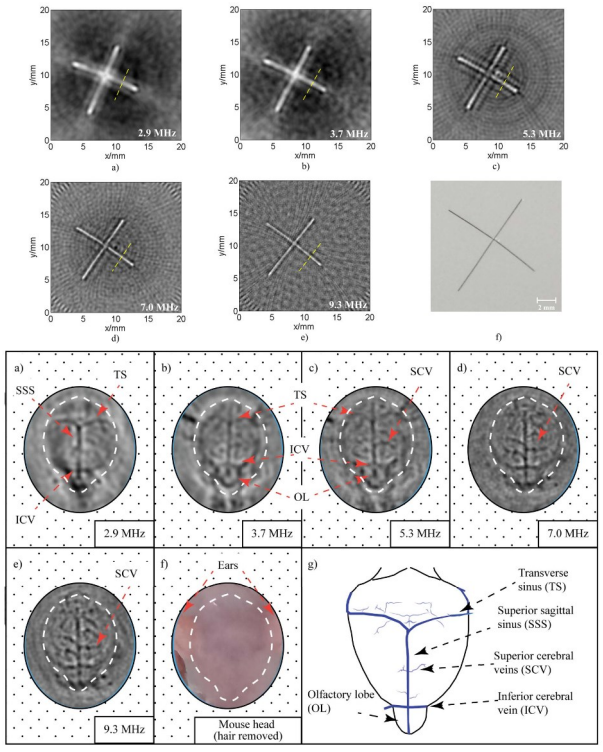
Architecture



Implementation



Verification



In ISSCC 2018

Reconfigurable X-Connected Wireless Power Transceiver for Device-to-Device Wireless Charging

Fangyu Mao, Yan Lu, Seng-Pan U, and Rui P. Martins

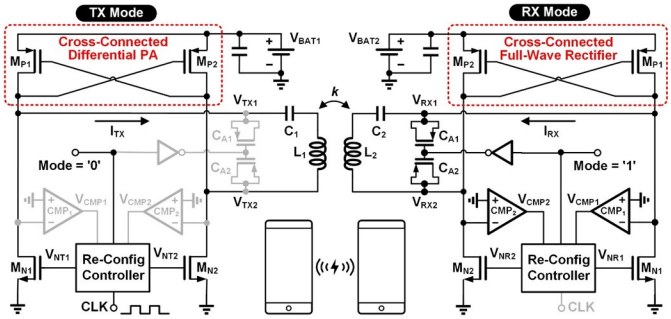
From Integrated Power research line

Motivation

Wireless power transfer (WPT) via inductive coupling is a convenient way to charge the power-starving portable/wearable devices. Recently, device-to-device (D2D) wireless charging was demonstrated, which expands the WPT applications. Different from the traditional wireless charging which gets energy from the AC mains and has unlimited energy, the D2D charging sources power from an energy-constrained battery. Therefore, achieving the maximum efficiency transfer is a key design issue. This work proposes an X-connected wireless power TRX with near-optimum switch-timing-control schemes, which not only reduces the circuit components but also greatly improves the power efficiency.

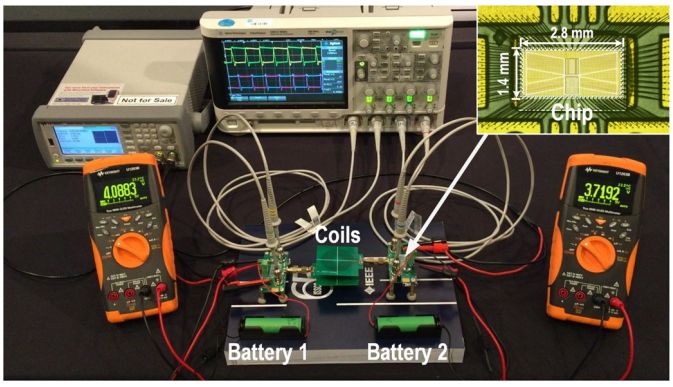
Architecture

Now, the power PMOS transistors in both TX and RX modes are X-connected, forming a fully-symmetrical structure. Then, the gate-drive switching loss of the power PMOS transistors is recycled by the LC tank.



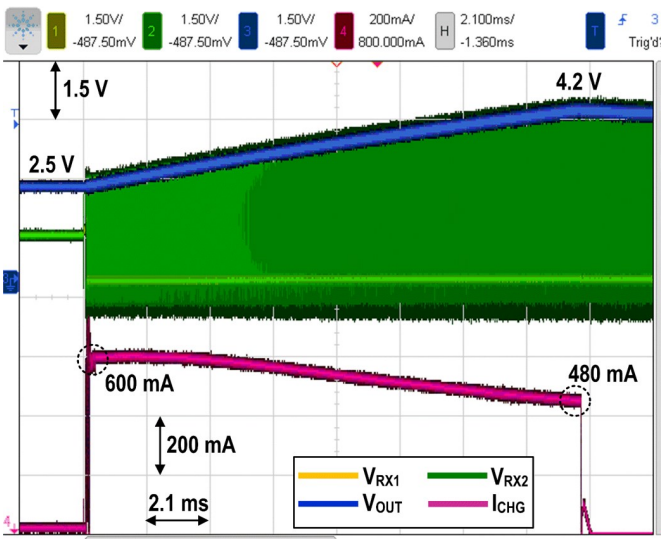
Implementation

The proposed reconfigurable X-connected wireless power TRX was fabricated in a 0.35-μm CMOS process with thick metal-4 option. The complete system with one battery charging another was demonstrated on ISSCC 2018, San Francisco, USA.



Verification

Measured AC input voltage, charging current and output voltage when charging a 4.7-mF capacitor. The maximum charging current is 0.6A.



In Springer Biomedical Microdevices 2019

LampPort - A Handheld Digital Microfluidic Device for Loop-Mediated Isothermal Amplification (LAMP)

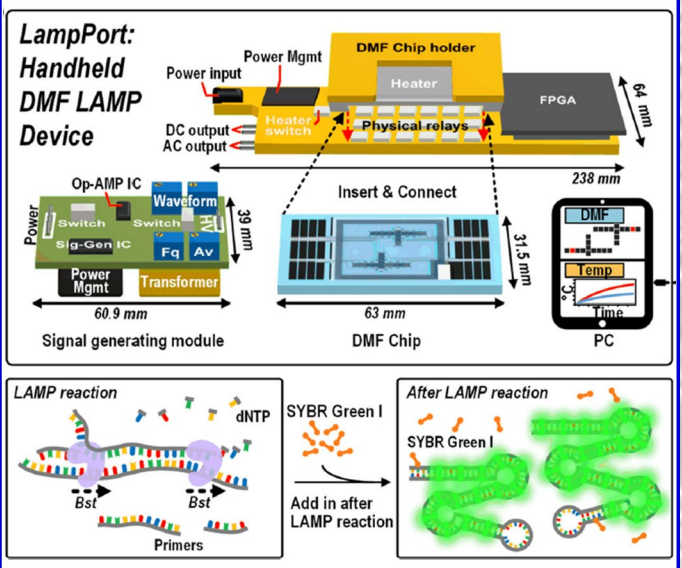
Liang Wan, Jie Gao, Tianlan Chen, Cheng Dong, Haoran Li, Yan-Zi Wen, Zhao-Rong Lun, Yanwei Jia, Pui-In Mak, and Rui P. Martins

From Multidisciplinary Research Area (Microfluidics)

Motivation

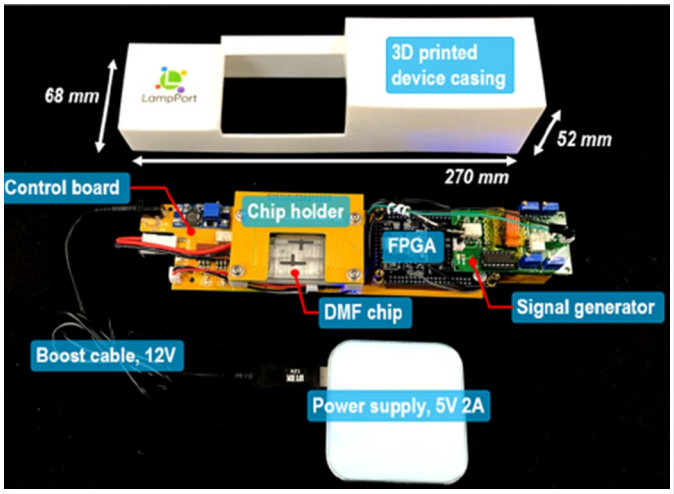
This work is a handheld, automatic and detection system-free thermal digital microfluidic (DMF) device for DNA detection by loop-mediated isothermal amplification (LAMP). Droplet manipulation and real-time temperature control systems were integrated into a handheld device. The control software could be installed into any tablet and communicate with the device via Bluetooth. In the experimentation, we loaded 2-μl samples with an electrowetting force into sandwich-structured DMF chips, thereby considerably reducing reagent consumptions. After an on-chip LAMP reaction, we added a highly concentrated SYBR Green I droplet and mixed it with a reaction droplet to enable product detection with the naked eye. This step prevented aerosol contamination by avoiding the exposure of the reaction droplet to the air. Using a blood parasite Trypanosoma brucei as a model system, this system showed similar results as a commercial thermal cycler and could detect 40 copies per reaction of the DNA target. This low-cost, compact device removed the bulky optical system for DNA detection, thus enabling it to be well suited for POC testing.

Architecture

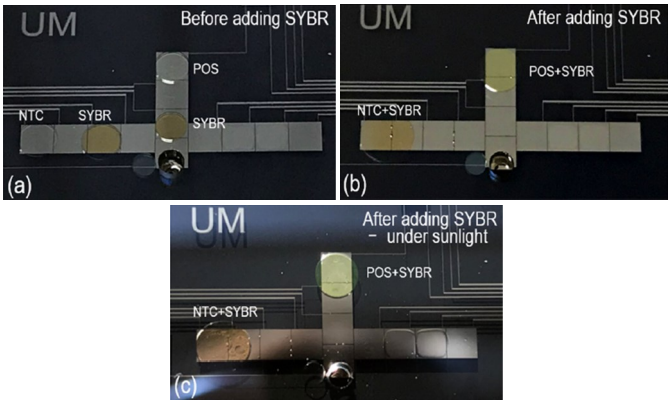


Overview of a handheld digital microfluidic (DMF) device for loop-mediated isothermal amplification (LAMP).

Implementation



Result

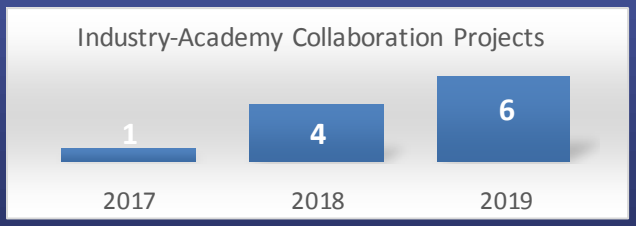


End-point evaluation of on-chip LAMP reactions (a) before and (b) after adding SYBRGreen I. These images were captured using iPhone 6 (a, b) under the ambient light and (c) under the sunlight. The SYBR Green I concentration in (a) was 1000×. A black adhesive tape was attached to the bottom of the DMF chip to enhance the naked-eye visualisation. NTC: no-template control. POS: positive sample

Technology Transfer Office and Commercialization Activities

2018 was the 3rd year after the creation of the Technology Transfer Office (TTO). Over the past three years, due to tremendous efforts from TTO on establishing good interaction with the IC design industry, the number of cooperation research projects between SKL-AMSV and companies has grown consistently. The amount of research funding from industry is estimated to be more than ten times from 2017 to 2019. The industry partners are from Greater Bay area cities such as Shenzhen, Guangzhou, Zhuhai and also from Beijing. The mainland largest IC design company is one of SKL-AMSV's cooperation partner.

A delegation from Huawei visited SKL AMSV for discussions



Number of Industry-Academy Projects has rapidly grown

Contributing to the Development of Guangdong-Hong Kong-Macau Greater Bay Area

Integrated Circuit Design is one of the strategic key industries in China. At the same time, our state plans to drive Guangdong-Hong Kong-Macau Greater bay area into an innovation-oriented economic system in 2035. As a State Key Laboratory, SKL-AMSV responds to the development direction of the country with specific actions. In addition to disseminate our technology to regional companies, SKL-AMSV has also participated in the establishment of Guangdong- Hong Kong-Macau Semiconductor Industry Alliance becoming its founding member. Moreover, more resources from SKL-AMSV will be allocated to setup the SKL-AMSV design center in Hengqin.

The establishment of Guangdong-Hong Kong-Macau Semiconductor Industry Alliance, with delegations from Hong Kong, Macau, Shenzhen, Guangzhou and Zhuhai.

Seminar on Macau-Hengqin Industry-University Research Cooperation, with delegations from UM and Industry

US and International Patents Granted in 2018

1. "A Method for On-Chip Precise Sample Delivery in a Microfluidic System," International Patent, PCT/UMPT161-2018, **Jul. 2018.**
2. "Cooperative-Electrode Driving Technique for Droplet-Velocity Improvement of Digital Microfluidic Systems," US Patent, No. 10,016,759, **Jul. 2018.**
3. "A Hybrid STATCOM with Wide Compensation Range and Low DC-Link Voltage," US Utility patent, No. 9,751,083, **Jun. 2018.**
4. "一种检测和分析 DNA 的方法," International Patent, PCT/CN2018/088762, **May 2018.**
5. "Design of a Thyristor Controlled LC Compensator," US Utility Patent, No. 9,960,599, **May. 2018.**
6. "Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators," US Patent, No. 9946281, **Apr. 2018.**

Upholding Scientific Leadership in ISSCC Benchmark in Terms of State-of-The-Art Chips

Academy in China	2011	2012	2013	2014	2015	2016	2017	2018	2019	Total
University of Macau ★	2	1	1	3	2	3	6	7	8	33
HKUST	1	1	2	3	4	3	4	2	1	21
Fudan Univ.	1	1	2	1				2	3	10
Tsinghua Univ.	1			2		1			2	6
Chinese Acad. Sci.	1		1	1						3
Peking Univ.								1		1
Chengdu UESTC								1		1
SJTU									1	1
Southeast U.									1	1

★ **Awards and Student Research Previews (PhD) in 2011 - 2019:**

1 x Far-East Best Paper Award (First in China)
7 x SSCS Pre-Doctoral Achievement Awards
2 x ISSCC Silkroad Awards
1 x ISSCC Student Research Preview Award
14 x ISSCC Student Research Preview

New Academics Joined SKL AMS-VLSI in 2018

Assistant Professor

Ka-Fai Un received the B.Sc. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2007, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau (UM), Macao, China. He is currently a Assistant Professor at SKL AMS-VLSI. He was a Macau Fellow holding a visiting positon in the University College Dublin.

Research Interests: Wireless integrated circuits design, Mathematics.

Lecturer (Macao Fellow)

Weihan Yu received the B.Sc. and M.Sc. degrees in electrical and electronics engineering and Ph.D. degree in electrical and computer engineering from the University of Macau (UM), Macao, China. He is currently a Lecturer (Macao Fellow) at SKL AMS-VLSI. He will be a Visiting Scholar in the Stanford University.

Research Interests: Wireless integrated circuits design.

Events and Visits

Visit by a Delegation of China Ministry of Science and Technology (MOST)

Visit by a Delegation of Guangzhou Science, Technology and Innovation Commission

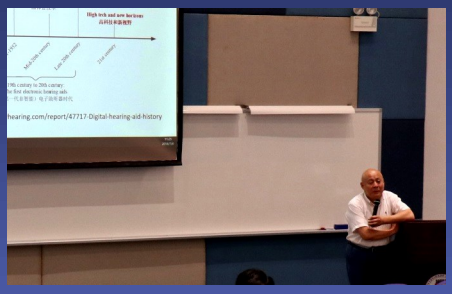
Visit by Wang Lixin, Vice Mayor of Shenzhen Government, China

Visit by Yan Wu, Vice Mayor of Shenzhen Government, China

Distinguished Lectures and Workshops

"Machine Learning Today and Tomorrow: Technology, Circuits and System" by
Prof. Boris Murmann,
IEEE Fellow, Professor of Electrical Engineering, Stanford University, USA

"Software Defined IC and Artificial Intelligence" by
Prof. Wei Shaojun,
IEEE Fellow, Dean of Institute of Microelectronics, Tsinghua University, China



"Binaural Hearing Aid System and the Intelligent Acoustic Signal Processing" by
Prof. Wang Zhihua,
IEEE Fellow, Professor of Tsinghua University, China

Publications

Book

- *"Handheld Total Chemical and Biological Analysis Systems,"* ***Springer*****, 2018.**

Book Chapter

- *"CMOS Circuits for Biological Sensing and Processing Systems - Micro-NMR on CMOS for Biomolecular Sensing,"* ***Springer*****, 2018.**

IEEE Conferences – 14 Papers

22nd International Conference on Miniaturized Systems for Chemistry and Life Sciences (μTAS 2018), Kaohsiung, Taiwan, China, **Nov. 2018**

- "3D Microstructures to Realize Single Cell Culture on Digital Microfluidic Chip for Precision Medicine"
- "On-Chip Pico-Pipette: A Method for Precise Delivery in a DMF system"

44th Annual Conference of the IEEE Industrial Electronics Society (IECON 2018), Washington D.C., USA, **Oct. 2018**

- "DC-Link Voltage Reduction Design Method for Three-Phase Four-Wire LC-Hybrid Active Powers under Reactive and Unbalanced Current Compensation"
- "Voltage Mode Controller Design and Experimental Verification of a Three-Phase Capacitive-Coupling Grid Connected Inverter in PV System"
- "A Power Quality Indexes Measurement System Platform with Remote Alarm Notification"
- "Selective Power Management Control for Hybrid Active Power Filter"
- "Comparisons of Different Hybrid Inverters for Power Quality Compensation with/without Active Power Injection"
- "Design and Analysis of Single-Phase Adaptive Passive Part Coupling Hybrid Active Power Filter (HAPF)"

10th IEEE PES Asia-Pacific Power and Engineering Conference (APPEEC 2018), Sabah, Malaysia, **Oct. 2018**

- "The Analysis of DC-Link Voltage, Compensation Range, Cost, Reliability and Power Loss for Shunt (Hybrid) Active Power Filters"

15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2018), Prague, Czech Republic, **Jul. 2018**

- "Design and Optimization of a Class-C/D VCO for Ultra-Low-Power IoT and Cellular Applications"

9th Asia-Pacific Conference of Transducers and Micro-Nano Technology (APCOT 2018), Hong Kong, China, **Jun. 2018**

- "In-Minutes Polymerase Chain Reaction with Specific DNA Amplification On Digital Microfluidics with Sloppy Temperature Control"

IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Shenzhen, China, **Jun. 2018**

- "In-Minutes Polymerase Chain Reaction with Specific DNA Amplification On Digital Microfluidics with Sloppy Temperature Control"

2018 International Symposium on VLSI Design, Automation and Test (2018 VLSI-DAT), Hsinchu, Taiwan, China, **Apr. 2018**

- "A 6.78 MHz Active Voltage Doubler with Near-Optimal On/Off Delay Compensation for Wireless Power Transfer Systems"

23rd Asia and South Pacific Design Automation Conference (ASP-DAC 2018), Jeju City, South Korea, **Jan. 2018**

- "A Dual-Output SC Converter with Dynamic Power Allocation for Multi-Core Application Processors" **[University LSI Design Contest Special Feature Award]**

SCI Journals – 54 Papers (6 in 2019)

- "LampPort: A Handheld Digital Microfluidic Device for Loop-Mediated Isothermal Amplification (LAMP)," ***Biomedical Microdevices***, **Jan. 2019.**
- "A 0.044-mm^2 0.5-to-7-GHz Resistor-Plus-Source-Follower-Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3±0.45 dB," ***IEEE Transactions on CAS II: Express Briefs***, **Jan. 2019.**
- "A 0.0056-mm^2 -4249-dB-FoM All-Digital MDLL using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs," ***IEEE Journal of Solid-State Circuits***, **Jan. 2019.**
- "Many-Objective Sizing Optimization of a Class-C/D VCO for Ultralow-Power IoT and Ultralow-Phase-Noise Cellular Applications," ***IEEE Transactions on Very Large Scale Integration (TVLSI) Systems***, **Jan. 2019.**
- "Analysis of Reference Error in High-Speed SAR ADCs with Capacitive DAC," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Jan. 2019.**
- "Experimental Verifications of Low Frequency Path Gain (PG) Channel Modeling for Implantable Medical Device (IMD)," ***IEEE Access***, **Jan. 2019.**
- "Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck-Boost Switched-Capacitor DC-DC Converters," ***IEEE Journal of Solid-State Circuits***, **Dec. 2018.** **[Invited Paper]**
- "An Inverse-Class-F CMOS Oscillator with Intrinsic-High-Q First Harmonic and Second Harmonic Resonances," ***IEEE Journal of Solid-State Circuits***, **Dec. 2018.**
- "Process Compensated BJT-Based CMOS Temperature Sensor with a ±1.5 °C (3σ) Batch-to-Batch Inaccuracy," ***IET Electronics Letters***, **Nov. 2018.**
- "Nano-Ampere Low-Dropout Regulator Designs for IoT Devices," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2018.**
- "A 0.19 mm^2 10b 2.3 GS/s 12-Way Time-Interleaved Pipelined-SAR ADC in 65-nm CMOS," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2018.**
- "Missing-Code-Occurrence Probability Calibration Technique for DAC Nonlinearity with Supply and Reference Circuit Analysis in a SAR ADC," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Nov. 2018.**
- "Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled mm-wave VCO Using a Single-Center-Tapped Switched Inductor," ***IEEE Journal of Solid-State Circuits***, **Nov. 2018.**
- "A 220-MHz Bondwire-Based Fully-Integrated KY Converter with Fast Transient Response under DCM Operation," ***IEEE Transactions on CAS I: Regular Papers***, **Nov. 2018.**
- "Gain Error Calibrations for Two-Step ADCs: Optimizations Either in Accuracy or Chip Area," ***IEEE Transactions on Very Large Scale Integration (TVLSI) Systems***, **Nov. 2018.**
- "A Wideband Inductorless dB-Linear Automatic Gain Control Amplifier Using a Single-Branch Negative Exponential Generator for Wireline Applications," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Oct. 2018.**
- "A Fully Integrated Low-Dropout Regulator with Differentiator-Based Active Zero Compensation," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Oct. 2018.**
- "A Low-Power Compression-Based CMOS Image Sensor with Microshift-Guided SAR ADC ," ***IEEE Transactions on Circuits and Systems – Part II: Express Briefs*** , **Oct. 2018.**
- "A 5.35-mW 10-MHz Single-Opamp Third-Order CT ΔΣ Modulator with CTC Amplifier and Adaptive Latch DAC Driver in 65-nm CMOS," ***IEEE Journal of Solid-State Circuits***, **Oct. 2018.**
- "A 10-MHz Bandwidth Two-Path Third-Order ΣΔ Modulator with Cross-Coupling Branches," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Oct. 2018.**
- "A 14-bit Split-Pipeline ADC with Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Oct. 2018.**
- "A Reconfigurable and Extendable Digital Architecture for Mixed Signal Power Electronics Controller," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Oct. 2018.**
- "Review and Selection Strategy for High Accuracy Modeling of PWM Converters in DCM," ***Hindawi Journal of Electrical and Computer Engineering***, **Oct. 2018.**
- "Advanced Power Electronic Converters and Power Quality Conditioning," ***Journal of Electrical and Computer Engineering***, **Oct. 2018.**
- "0.45-V 5.4-nW Switched-Capacitor Bandgap Reference with Intermittent Operation and Improved Supply Immunity," ***IET Electronics Letters***, **Oct. 2018.**
- "Ambient RF Energy Harvesting System: A Review on Integrated Circuit Design," ***Springer Analog Integrated Circuits and Signal Processing***, **Sep. 2018.**
- "A 36-Gb/s 1.3-mW/Gb/s Duobinary-Signal Transmitter Exploiting Power-Efficient Cross-Quadrature Clocking Multiplexers with Maximized Timing Margin," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Sep. 2018.**
- "A Regulation-Free Sub-0.5 V 16-/24-MHz Crystal Oscillator with 14.2-nJ Startup Energy and 31.8-μW Steady-State Power," ***IEEE Journal of Solid-State Circuits***, **Sep. 2018.**
- "A Coin-Battery-Powered LDO-Free 2.4-GHz Bluetooth Low-Energy Transmitter with 34.7% Peak System Efficiency," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Sep. 2018.**
- "A Hardware-Efficient Feedback Polynomial Topology for DPD Linearization of Power Amplifiers: Theory and FPGA Validation," ***IEEE Transactions on CAS I - Regular Papers***, **Sep. 2018.**
- "Analysis, Control, and Design of a Hybrid Grid-Connected Inverter for Renewable Energy Generation with Power Quality Conditioning," ***IEEE Transactions on Power Electronics***, **Aug. 2018.**
- "An Assay for Systematically Quantifying the Vestibulo-Ocular Reflex to Assess Vestibular Function in Zebrafish Larvae," ***Frontiers in Cellular Neuroscience***, **Aug. 2018.**
- "Hybrid Structure of Static VAR Compensator and Hybrid Active Power Filter (SVC//HAPF) for Medium Voltage Heavy Loads Compensation," ***IEEE Transactions on Industrial Electronics (TIE)***, **Jun. 2018.**
- "A 0.18-V 382-μW Bluetooth Low-Energy Receiver Front-End with 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS," ***IEEE Journal of Solid-State Circuits***, **Jun. 2018.**
- "A Digital LDO with Co-SA Logics and TSPC Dynamic Latches for Fast Transient Response," ***IEEE Solid-State Circuits Letters***, **Jun. 2018.**
- "Design Considerations of Distributed and Centralized Switched-Capacitor Converters for Power Supply On-Chip," ***IEEE Journal of Emerging and Selected Topics in Power Electronics***, **Jun. 2018.**
- "Overview of Recent Development on Wireless Sensing Circuits and Systems for Healthcare and Biomedical Applications," ***IEEE Journal on Emerging and Selected Topics in Circuits and Systems***, **Jun. 2018.**
- "Hybrid Structure of Static VAR Compensator and Hybrid Active Power Filter (SVC//HAPF) for Medium Voltage Heavy Loads Compensation," ***IEEE Transactions on Industrial Electronics***, **Jun. 2018.**
- "Analysis of Common Mode Interference and Jitter of Clock Receiver Circuits with Improved Topology," ***IEEE Transactions on Circuits and Systems I - Regular Papers***, **Jun. 2018.**
- "Multi-Functional Hybrid Structure of SVC and Capacitive Grid Connected Inverter (SVC//CGCI) for Active Power Injection and Non-Active Power Compensation," ***IEEE Transactions on Industrial Electronics (TIE)***, **May 2018.**
- "A SAW-Less Tunable RF Front End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-LC N-Path LNA," ***IEEE Journal of Solid-State Circuits*** , **May 2018.**
- "Turning On/Off The Anti-Tumor Effect of the Au Cluster via Atomically Controlling Its Molecular Size," ***ACS Nano***, **Apr. 2018.**
- "Minimizing Inverter Capacity Design and Comparative Performance Evaluation of SVC-Coupling Hybrid Active Power Filters," ***IEEE Transactions on Power Electronics (TPEL)***, **Apr. 2018.**
- "Nano-Watt Class Energy-Efficient Capacitive Sensor Interface with On-Chip Temperature Drift Compensation," ***IEEE Sensors Journal*** , **Apr. 2018.**
- "A 0.083-mm^2 25.2-to-29.5 GHz Multi-LC-Tank Class-F_{234} VCO with a 189.6-dBc/Hz FOM," ***IEEE Solid-State Circuits Letters***, **Apr. 2018.**
- "A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC with Background Offset Calibration," ***IEEE Journal of Solid-State Circuits***, **Mar. 2018.**
- "Monolithic Multiband CMUTs for Photoacoustic Computed Tomography With In Vivo Biological Tissue Imaging," ***IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control***, **Mar. 2018.**
- "Quick and Cost-Efficient A/D Converter Static Characterization using Low-Precision Testing Signal," ***Microelectronics Journal - Elsevier***, **Feb. 2018.**
- "A 0.032-mm^2 0.15-V 3-Stage Charge-Pump Scheme Using a Differential Bootstrapped Ring-VCO for Energy-Harvesting Applications," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, **Feb. 2018.**
- "Passive Noise Shaping in SAR ADC with Improved Efficiency," ***IEEE Transactions on VLSI Systems***, **Feb. 2018.**
- "Analysis in the Effects of Operation Voltage Range in Flexible DC Control on Railway HPQC Compensation Capability in High-Speed Co-Phase Railway Power," ***IEEE Transactions on Power Electronics***, **Feb. 2018.**
- "Time-Efficient BER Estimation Approach Using Jitter Characteristics for HBC Channel," ***IET Science, Measurement & Technology***, **Jan. 2018.**
- "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," ***IEEE Journal of Solid-State Circuits***, **Jan. 2018.**
- "A 0.7–2.5 GHz, 61% EIRP System Efficiency, Four-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, **Jan. 2018.**

Major IEEE Solid-State Circuits Conferences – 21 Papers

IEEE Asian Solid-State Circuits Conference (ASSCC 2018), Tainan, Taiwan, China, **Nov. 2018**

- "A 7b 2 GS/s Time-Interleaved SAR ADC with Time Skew Calibration Based on Current Integrating Sampler" **[Highlighted Paper]**
- "A 2.4-GHz Single-Pin Antenna Interface RF Front-End with a Function-Reuse Single-MOS VCO-PA and a Push-Pull LNA"
- "An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery"

IEEE European Solid-State Circuits Conference (ESSCIRC 2018), Dresden, Germany, **Sep. 2018**

- "A 39mW 7b 8GS/s 8-way TI ADC with Cross-linearized Input and Bootstrapped Sampling Buffer Front-end"

IEEE Symposium on VLSI Circuits (VLSIC), Honolulu, USA, **Jun. 2018**

- "A 77dB SNDR 12.5MHz Bandwidth 0-1 MASH ΣΔ ADC Based on the Pipelined-SAR Structure"
- "A 2pJ/Pixel/Direction MIMO Processing Based CMOS Image Sensor for Omnidirectional Local Binary Pattern Extraction and Edge Detection"
- "A 550μW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65nm CMOS" **[Travel Grant Award] [Invited Special Issue in JSSC]**

IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, **May 2018**

- "Design and Control of an Integrated 3-Level Boost Converter under DCM Operation"
- "A Single-Stage Current-Mode Active Rectifier with Accurate Output-Current Regulation for IoT"
- "A Dual-Loop Digital LDO Regulator with Asynchronous-Flash Binary Coarse Tuning"
- "A 0.4V 6.4μW 3.3MHz CMOS Bootstrap Relaxation Oscillator with ±0.71% Frequency Deviation from -30°C to 100°C for Wearable and Sensing Applications"

IEEE International Solid-State Circuits Conference (ISSCC 2018), San Francisco, CA, USA, **Feb. 2018**

- "A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS"
- "A 0.22-to-2.4V-Input Fine-Grained Fully-Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Archiving 84.1% Peak Efficiency at 13.2μW/mm^2" **[Invited Special Issue in JSSC]**
- "A Regulation-Free Sub-0.5V 16/24MHz Crystal Oscillator for Energy Harvesting BLE Radios with 14.2nJ Startup Energy and 31.8uW Steady-State Power"
- "A 0.4V 430nA Quiescent Current NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28nm CMOS"
- "A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Charging with 78.1% Total Efficiency"
- "A 0.0056mm^2 All-Digital MDLL Using Edge Re-Extraction, Dual Ring-VCOs and a 0.3mW Block-Sharing Frequency-Tracking Loop Achieving 292fs$_{rms}$ Jitter and -249dB FoM" **[Invited Special Issue in JSSC]**
- "An Inverse-Class-F CMOS VCO with Intrinsic-High-Q 1st- and 2nd-Harmonic Resonances for 1/f^2-to-1/f^3 Phase Noise Suppression Achieving 196.2dBc/Hz FoM" **[Invited Special Issue in JSSC]**
- "A 14-bit Split Pipeline ADC with Self-Adjusted Opamp-Sharing Duty Cycle" **[Student Research Preview]**
- "A Coin-Battery-Powered Regulation-Free 2.4-GHz Bluetooth Low-Energy Transmitter (TX)" **[Student Research Preview]**
- "A 430f$_{rms}$ 2.4GHz Ring-Oscillator PLL with Backend Discrete-Time Phase Noise Cancellation Achieving 240.5dB Jitter-FoM" **[Student Research Preview]**

The first spin-off of the SKLab AMS-VLSI, named Digi Fluidic and led by 2 of our PhD graduates, started operation in Innovalley, Hengqin, China.

State Key Laboratory of Analog and Mixed-Signal VLSI / UM

http://www.amsv.umac.mo