澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

模拟与混合信号
超大规模集成电路
国家重点实验室
（澳门大学伙伴实验室）
State Key Laboratory of Analog and Mixed - Signal VLSI
(Partner Laboratory in University of Macau)
中华人民共和国科学技术部

模擬與混合信號超大規模集成電路
國家重點實驗室
State Key Laboratory of
Analog and Mixed-Signal VLSI

State Key Lab of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) Newsletter

Motto: "Locally, from (World) Quality towards (National) Quantity"

座右銘:立足本土、人才培養, 以世界級質量創建國家級規模

Year 7
No . 7

2017 Milestones

March 2018

Co-Funded by
Macao Science and Technology Development Fund (FDCT)

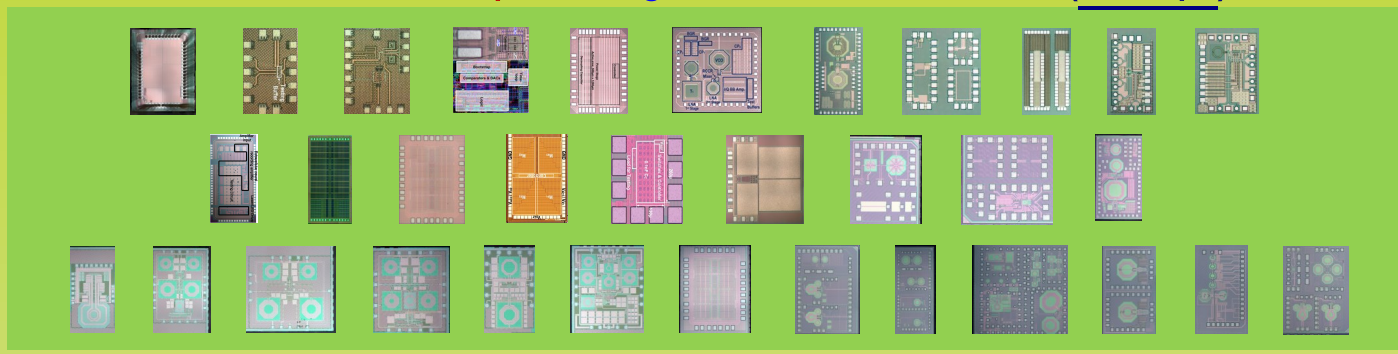
Events

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) participated in the 10th Annual Meeting of the Committee for China and Macao Cooperation in Science and Technology held in Macao, China, November 7, 2017.

State Key Laboratory of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) has passed the 2nd mid-term assessment (6 years) by Ministry of Science and Technology (MOST) of China and Macao FDCT, July 6, 2017.

A delegation from the ITPC of ISSCC 2018, including academics from UM SKL AMS-VLSI, organized ISSCC promotional activities in Wuhan Optical Valley and Nanjing Wireless Valley, China, with over 100 attendees from both academia and industry, June 15, 2017.

State-of-the-Art Chips - Designed and Tested in 2017 (33 chips)



ISSCC 2018

A team of faculty members and students from the SKL AMS-VLSI and ECE/FST, University of Macau (UM) attended the 65th IEEE International Solid-State Circuits Conference (**ISSCC**) in **February 2018**, the most competitive conference in the world in the field of chip design.

7 papers from SKL AMS-VLSI were accepted at this year's conference, making UM one of the top 6 institutions in the world with most papers presented at ISSCC 2018, among which were Samsung, Korean Advanced Institute of Science and Technology, Intel Corporation, Delft University of Technology in the Netherlands and Georgia Institute of Technology in the United States. This reveals international recognition of SKL AMS-VLSI and it's leading position in the field in Asia. Besides, the SKLab PhD students received 1 Pre-doctoral Achievement Award and 3 Student Research Previews. In addition, a team from the SKL AMS-VLSI received the prestigious 2017 Takuo Sugano Award for Outstanding Far-East Paper, which was attributed for the first time to a team from China.

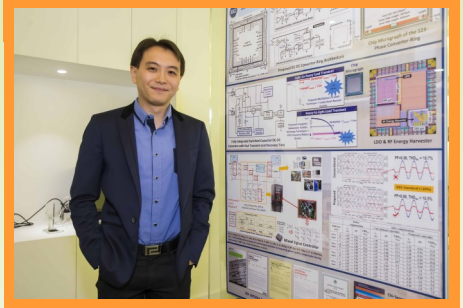
SKL AMS-VLSI Scholar Receives Young Researcher Award

Macao Fellow Dr. Lei Ka Meng received the Young Researcher Award from the International Institute of Macau, for his research project: '*Miniaturized Nuclear Magnetic Resonance Platforms for Chemical/Biological Assays with Customized CMOS Integrated Circuits*'. The awarded project is part of Lei's PhD thesis. Lei received also a Distinguished Design Award at IEEE ASSCC 2015 and a Predoctoral Achievement Award from the IEEE Solid-State Circuits Society at the 64th ISSCC.

SKL AMS-VLSI professor receives Outstanding Young Author Award from IEEE

Assistant Professor Dr. Lu Yan from UM SKL AMS-VLSI received the 2017 Outstanding Young Author Award from the Circuits and Systems (CAS) Society of the Institute of Electrical and Electronics Engineers (IEEE), for his paper titled '*A Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power Supply Rejection*'. This is the second time that a professor from the laboratory has received the award, showing that SKL AMS-VLSI is now in a leading position in the world in microelectronics research.

SKL AMS-VLSI professor receives IEEE PES Outstanding Engineer Award



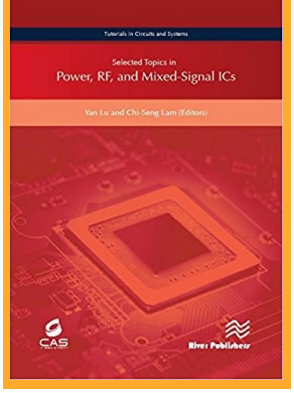
Assistant Professor Dr. Lam Chi Seng received IEEE PES Outstanding Engineer Award 2016. This is the first time that an engineer from Macao has received such an award. There is a consensus in the industry that the award can help the recipients from the fields of electricity and energy in Macao to develop their careers in other parts of the world. In addition, Lam has been invited to join the evaluation committee in Macao for the IEEE PES Outstanding Engineer Award 2017.

4 New PhD Graduates

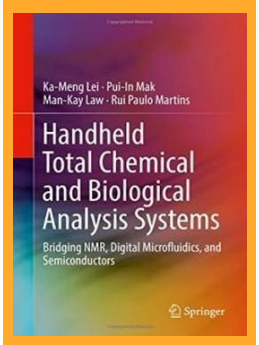
4. **Chen Chang Hao**, *Circuits and Noise Modeling for Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation,* **Oct. 2017.**
3. **Cheang Chak Fong**, *Digital Correction Techniques for I/Q Mismatch, LO Feedthrough and Distortion in Wideband Transmitters,* **Sep. 2017.**
2. **Yu Yuan Yu**, *Design and Characterization of Embossed Membrane CMUTs for Improving Output Pressure,* **Aug. 2017.**
1. **Dong Cheng**, *Electronic-Automated Digital Microfluidic System for Multi-Analysis,* **Jul. 2017.**

ASP-DAC 2018 University LSI Design Contest Special Feature Award

A Book by River Publisher



A Book by Springer



A 1.7mm^2 Inductor-less Fully-Integrated Capacitive-Flip Rectifier (CFR) for Piezoelectric Energy Harvesting with 483% Power Extraction Improvement

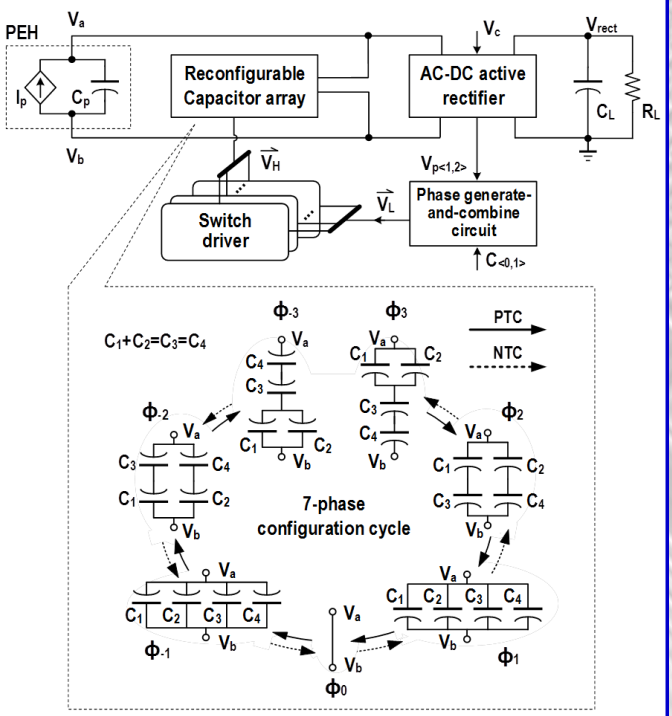
Zhiyuan Chen, Man-Kay Law, Pui-In Mak, Wing-Hung Ki and R. P. Martins

From Wireless research line

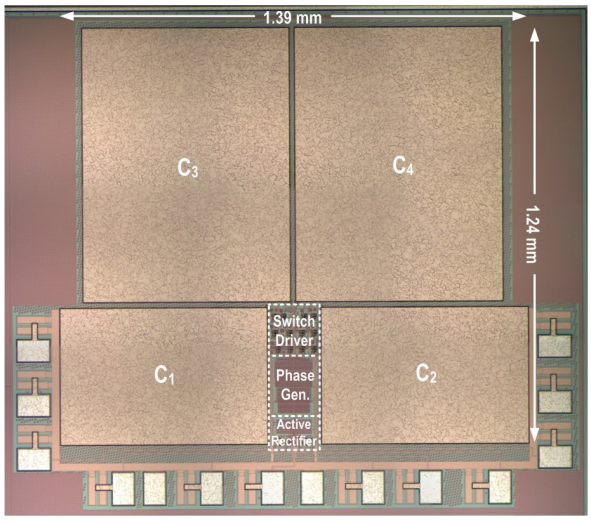
Motivation

This work presents a fully-integrated 7-phase flipping-capacitor rectifier (FCR) for piezoelectric energy harvesting (PEH) targeting for deep-tissue implant applications, where the system volume is of utmost importance. Instead of using an external high-Q inductor as the energy storage element, it achieves voltage reversion across the PEH intrinsic capacitor C_p during the zero crossing of PEH current I_p through an on-chip reconfigurable capacitor array to effectively increase the conduction time, thus realizing a fully-integrated solution. The proposed FCR can deliver 50.2μW with a loading of 680pF//125kΩ at 110kHz. It achieves a high Maximum Output Power Improving Rate (MOPIR) of 4.83x, while requiring zero external components to achieve an ultra-compact form factor when compared with the state of the art.

Architecture



Implementation



Verification

	This work	JSSC'16 [7]	ISSCC'14 [18]	JSSC'14 [15]	JSSC'10 [10]	TCAS-I'17 [16]	JSSC'16 [17]
Technology	**0.18 μm**	0.35 μm	0.35 μm	0.35 μm	0.35 μm	0.25μm Bi	0.35μm HV
Energy Extraction Technique	**Flipping-Capacitor Rectifier**	P-SSHI	Energy Pile-Up	Energy Investment	P-SSHI	P-SSHI	P-SSHI
Piezoelectric Harvester	**Piezo Systems Inc. (P5A4E @ 5mm^3)**	MIDE V21B & V22B	Emulated (Transformer + RC)	MIDE V22B	MIDE V22B	MIDE V22B	MIDE V20W
Key Component	**On-chip MIM Capacitor (C_{total} = 1.44 nF)[a]**	External Inductor (L = 3.3 mH)	External Inductor (L = 10 mH)[b]	External Inductor (L = 330 μH)	External Inductor (L = 47 μH)	External Inductor (L = 220 μH)	External Inductor (L = 20 μH)
Max. Output Power Increasing Rate (MOPIR)	**4.83x 4.78x[c]**	6.81x	4.22x	3.6x	2.8x	2.07x	5x[e]
Max. Voltage Flipping Eff. (η_F)	**0.85**	0.94	0.77[b]	NA	0.75[b]	0.75	0.67[b]
Chip Size	**1.7 mm^2**	0.72 mm^2	5.5 mm^2	2.34 mm^2	4.25 mm^2	0.74 mm^2	0.6 mm^2
Output Power	**50.2 μW**	160.7 μW[d]	87 μW	52 μW	32.5 μW	136 μW	75 μW
Operating Freq.	**110 kHz**	225 Hz	100 Hz	143 Hz	225 Hz	144Hz	82Hz

[a] Total capacitance for C_{1-4}
[b] Estimated from the corresponding literature
[c] Averaged over 4 measured samples
[d] Off-resonance with 3.35g acceleration
[e] FBR output power limited by excessive diode voltage drop

In IEEE ISSCC 2017 and JSSC 2018

A 0.18-V 382-μW Bluetooth Low-Energy (BLE) Receiver with 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS

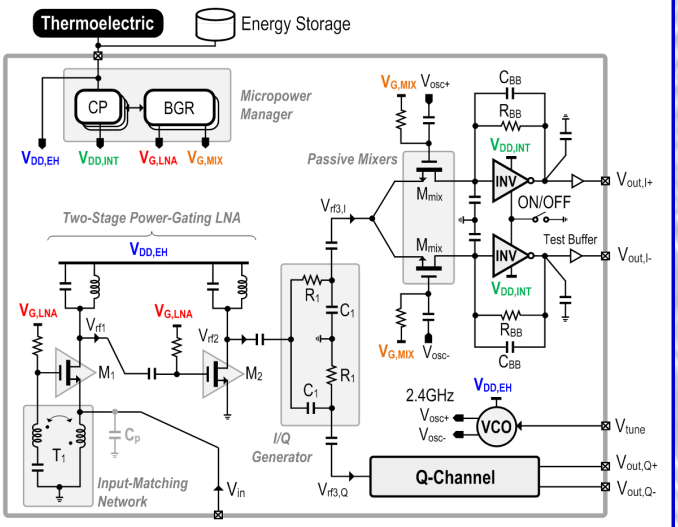
Haidong Yi, Wei-Han Yu, Pui-In Mak, Jun Yin, R. P. Martins

From Wireless research line

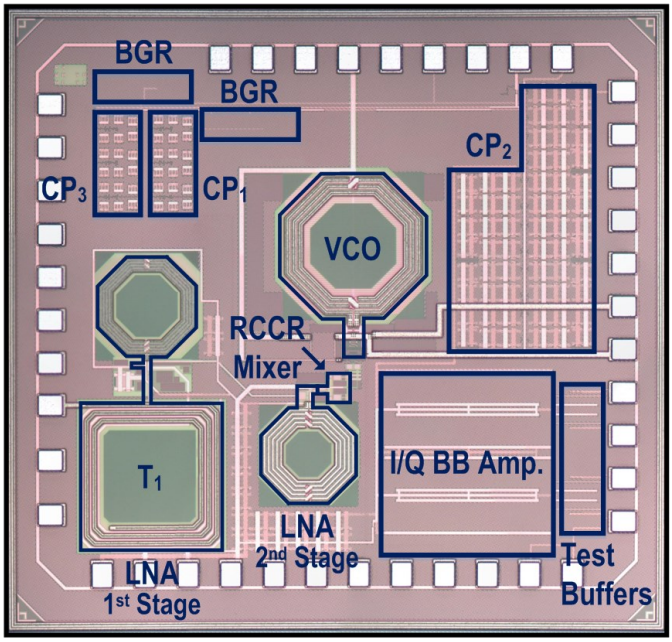
Motivation

This work is an ultra-low-voltage Bluetooth Low-Energy (BLE) receiver (RX) with an on-chip micropower manager (μPM) to customize the internal voltage domains. It aims at direct-powering by the sub-0.5V energy-harvesting sources like the on-body thermoelectric, eliminating the loss and cost of the interim DC-DC converters. Specifically, the RX incorporates: 1) a two-stage power-gating LNA with fully on-chip input-impedance matching and passive gain boosting reducing both the active and sleep power; 2) a class-D VCO in parallel with a class-C starter to secure a fast startup, and 3) a μPM using ring-VCO-locked charge pumps and Bandgap references to withstand the supply-voltage variation (0.18 to 0.3 V). Fabricated in 28-nm CMOS, the RX operates down to a 0.18-V supply, while exhibiting 11.3-dB NF and -12.5-dBm out-of-band IIP3. The VCO shows <-113 dBc/Hz phase noise at 2.5-MHz offset. The active and sleep power are 382 μW and 1.33 nW, respectively.

Architecture



Implementation



Result

	This Work		JSSC'15 [5] [A. Selvakumar, et al.]	JSSC'13 [7] [F. Zhang, et al.]	JSSC'14 [6] [Z. Lin, et al.]
Applications	2.4GHz BLE		2.4GHz BLE	2.4GHz Non-Standard	2.4GHz ZigBee
Key Architecture & Circuit Techniques	Power-Gating LNA + ULV Class-D VCO + Passive I/Q Gen. + Micro-Power Manager		Current-Reuse Quadrature-LNA-Mixer-VCO Cell	Transformer-Coupling LNA and VCO + IF N-Path Filter	Current Reuse RF-to-BB Cell + VCO & DIV-by-4
External Matching	Zero		1 inductor + 1 cap.	1 inductor + 2 caps.	zero
Supply Voltage (V)	0.18	0.3	0.8	0.3	0.6 & 1.2
Active Power (μW)	382	1305	600 [1]	1600	2700 [1]
Sleep Power (nW)	1.33	3.32	N/A	N/A	N/A
NF (dB)	11.3	8.8	15.1 to 15.8	6.1	9
VCO Phase Noise (dBc/Hz) @ Offset	-113 to -115.5 @ 2.5 MHz	-116.6 to -118.9 @ 2.5 MHz	-109 @ 2.5 MHz	-112.8 @ 1 MHz	N/A
	[BLE spec: -102 @ 2.5 MHz] [2]				
Out-of-Band IIP3 (dBm)	-12.5	+4.8	-15.8 to -16.8	-21.5	-6
	[BLE Spec: -30] [2]				
IRR (dB)	26.2	25.1	30.5 to 37.3	N/A (no I/Q)	28
	[BLE Spec: 21] [2]				
Voltage Gain (dB)	34.5	41.3	55.5 to 56.1	83	55
BB Style	With I/Q		With I/Q	Without I/Q	With I/Q
BB Filtering	3 real poles [3]		2 complex poles	2 N-path filters	3 complex poles
Active Area (mm^2)	1.65		0.25	~1.7	0.26
Technology	28nm CMOS		130nm CMOS	65nm CMOS	65nm CMOS

[1] [5]-[6] have not included the loss, power and area of the power-management units if using a sub-0.5V energy-harvesting source.
[2] BLE specifications from [5]. [3] Partial channel-selection filtering.

In IEEE ASSCC 2017

A 5.35 mW 10 MHz Bandwidth CT Third-Order ΔΣ Modulator with Single Opamp Achieving 79.6/84.5 dB SNDR/DR in 65 nm CMOS

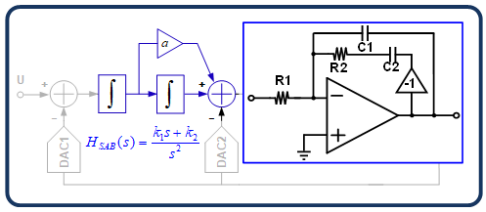
Wei Wang, Yan Zhu, Chi-Hang Chan, Seng-Pan U, R. P. Martins

From Data Conversion and Signal Processing research line

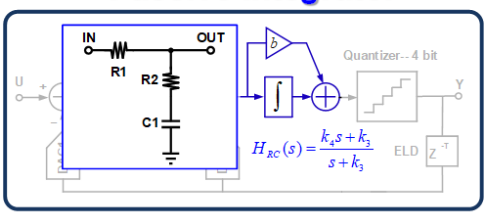
Motivation

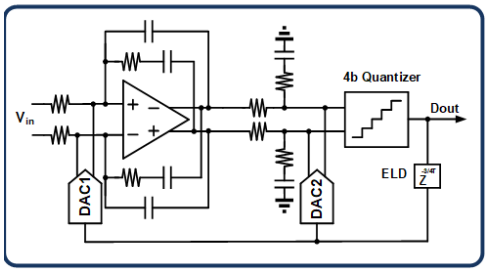
- For the wireless communication and VDSL applications.
- The CT Modulator is a wide used architecture while it has inherent benefit in anti-alias filtering and power efficiency when compared with its discrete-time counterpart.
- The opamp in the wideband CT modulator is often power hungry due to the stringent requirements.
- The SAB allows a single opamp to achieve a second order in the CTDSM. At the same time, the passive filter can also enhance the LF order with a small power overhead.
- In this CT modulator, the SAB integrator and passive integrator are combined to achieve 3rd order noise shaping with only one opamp.

Architecture

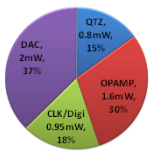


Passive Integrator

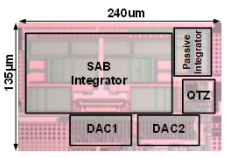


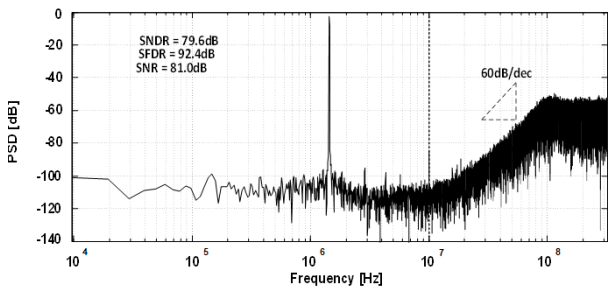


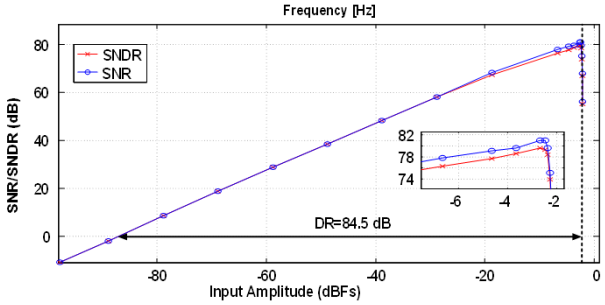
Implementation



Only 30% from Opamp







Verification

	T.Kim ISSCC 2017	T.Kim VLSI 2015	B.N ISSCC 2016	Y.Shu ISSCC 2013	G.Wei VLSI 2015	This work
Area (mm^2)	0.17	0.08	0.027	0.08	0.066	0.033
Technology (nm)	130	130	65	28	28	65
Supply Voltage (V)	1.2	1.2	1.0	1.2/1.5	0.9/1.8	1.2/1.8
Fs (MHz)	640	640	1000	640	432	640
Bandwidth (MHz)	15	10	10	18	5	10
Power (mW)	11.4	7.19	1.57	3.9	3.16	5.35
Peak SNDR (dB)	80.4	75.3	72.2	73.6	80.5	79.6
DR (dB)	82.9	78.5	77	78.1	83.9	84.5
FOMSch/SNDR (dB)	171.6	166.7	170.2	170.2	172.5	172.3
FOMSch/DR (dB)	174.1	169.9	172.0	174.7	175.9	177.2
FoMWa (fJ/conv.step)	44.1	75.9	23.6	27.7	36.5	36.5

In TCAS I 2017

A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing

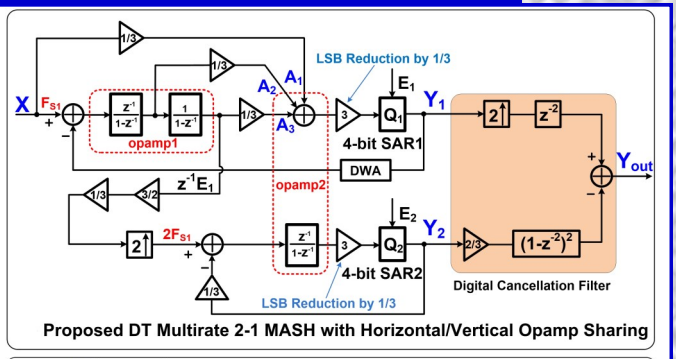
Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, R. P. Martins

From Data Conversion and Signal Processing research line

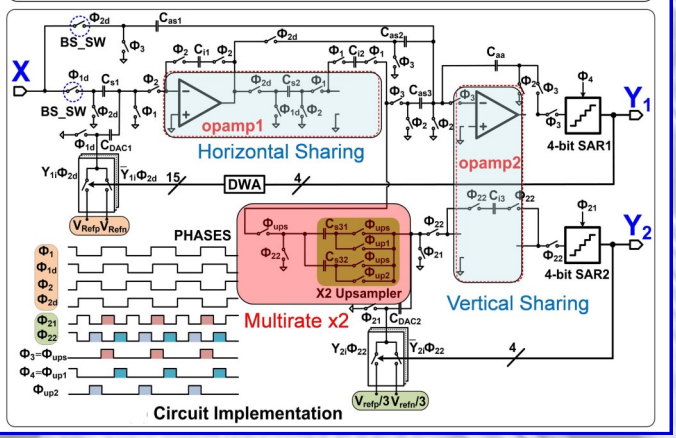
Motivation

This work presents a discrete time (DT) 2-1 MASH Delta-Sigma (ΔΣ) modulator with multirate opamp sharing for Analog-to-Digital Converters (ADC), targeting the optimization of power efficiency in active blocks, like opamps and quantizers. Through the allocation of different settling times to the opamps and by adopting the multirate technique, the power of the shared opamps is utilized more efficiently, and the 4-bit SAR quantizer and the Data Weighted Averaging (DWA) in the first stage enjoy additional operation time. Moreover, a detailed analysis and related simulations are presented to validate the enhanced opamp power efficiency in the proposed sharing scheme. The 65nm CMOS experimental chip running in multirate 120/240MHz achieves a mean SNDR of 77.1dB for a 5MHz bandwidth, consuming 4.2mW from a 1.2V supply and occupying 0.066mm^2 core area. It exhibits a Walden FoM of 69.7fJ/conv-step and a Schreier FoM of 167.9dB based on SNDR.

Architecture

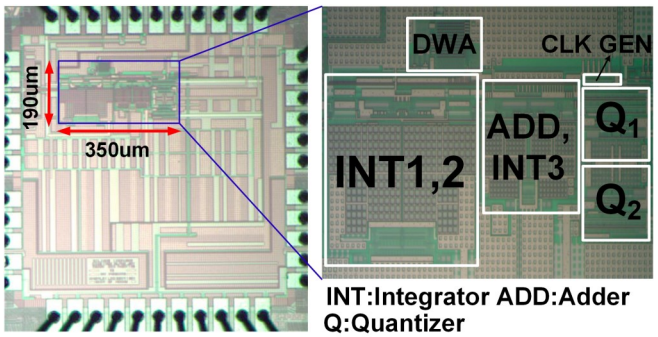


Proposed DT Multirate 2-1 MASH with Horizontal/Vertical Opamp Sharing

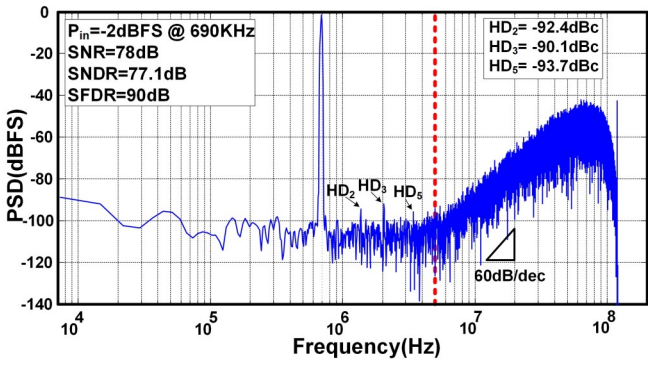


Circuit Implementation

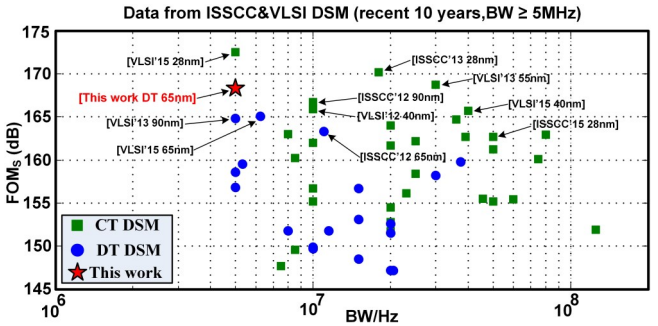
Implementation



INT:Integrator ADD:Adder
Q:Quantizer



Verification



	VLSI'13 Sachin Rao	VLSI'15 [3]	ISSCC'13 [4]	ISSCC'15 [5]	VLSI'15 [6]	This Work
Architecture	DT+VCO	DT NS-SAR*	CT	CT	CT	DT
Technology (nm)	90	65	28	28	28	65
Supply Voltage(V)	1.2/1	0.8	N/A	1.2/1.5	0.9/1.8	1.2
BW(MHz)	5	6.25	18	50	5	5
F_S(MHz)	640	50	640	1800	432	120/240
DR(dB)	77	N/A	78.1	85	83.9	78.5
Peak SNDR(dB)	73.9	58	73.6	74.6	80.5	77.1
Power (mW)	4.1	0.12	3.9	78	3.16	4.2
Active Area (mm^2)	0.16	0.0123	0.08	0.34	0.066	0.05
FOM_W (fJ/Conv.-step)	101	14.9	27.7	177.7	36.5	69.7
FOM_S(dB)	164.8	165.1	170.2	162.7	172.5	167.9

FOM_W=Power/(2*BW*2^{ENOB}) FOM_S=SNDR+10lg(BW/Power)

*DT NS-SAR: DT Noise-Shaping SAR

Data Source from B. Murmann, "ADC Performance Survey 1997-2015," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

In IEEE Transactions on Biomedical Engineering 2017
[Top 50 most accessed paper Mar. 2017 - Apr. 2018 in this journal]

An Integrated Circuit for Simultaneous Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation

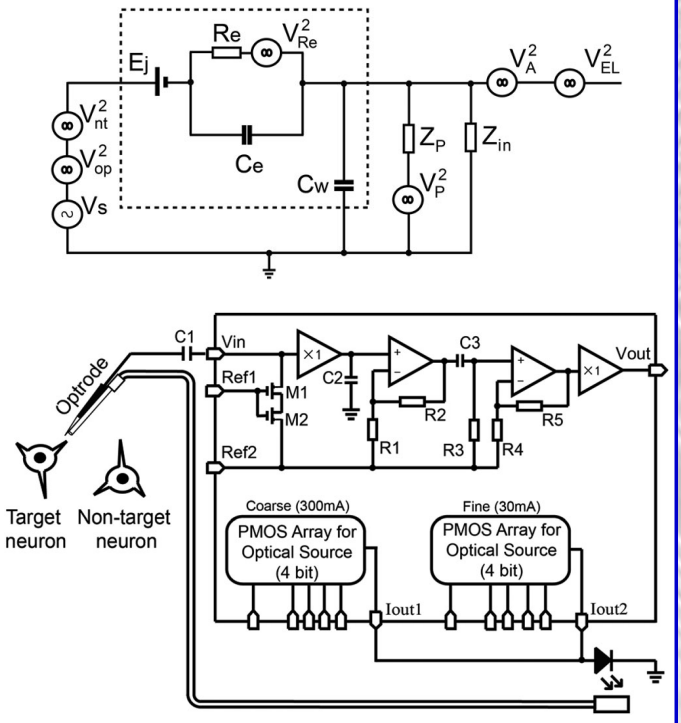
Chang Hao Chen, Elizabeth A. McCullagh, Sio Hang Pun, Peng Un Mak, Mang I Vai, Pui In Mak, Achim Klug, and Tim C. Lei

From Biomedical research line

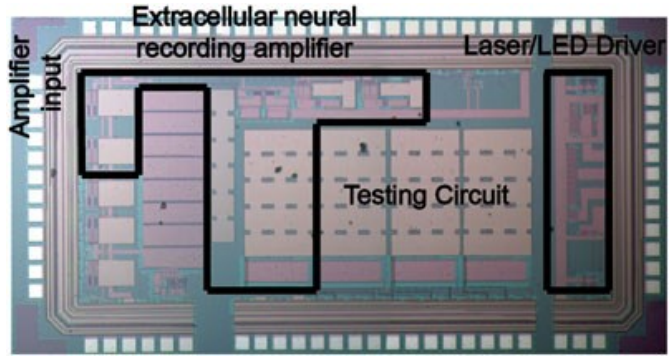
Motivation

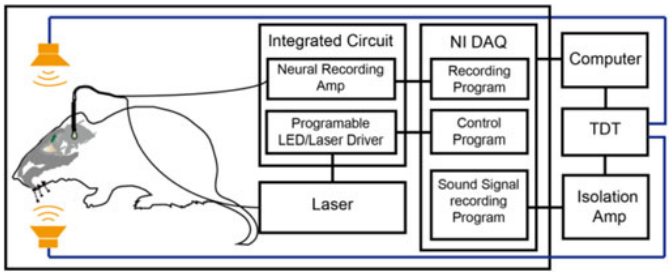
The ability to record and to control action potential firing in neuronal circuits is critical to understand how the brain functions. The objective of this study is to develop a monolithic integrated circuit (IC) to record action potentials and simultaneously control action potential firing using optogenetics.
Methods: A low-noise and high input impedance (or low input capacitance) neural recording amplifier is combined with a high current laser/light-emitting diode (LED) driver in a single IC.
Results: The low input capacitance of the amplifier (9.7 pF) was achieved by adding a dedicated unity gain stage optimized for high impedance metal electrodes. The input referred noise of the amplifier is 4.57 μV_{rms}, which is lower than the estimated thermal noise of the metal electrode. Thus, the action potentials originating from a single neuron can be recorded with a signal-to-noise ratio of at least 6.6. The LED/laser current driver delivers a maximum current of 330 mA, which is adequate for optogenetic control. The functionality of the IC was tested with an anesthetized Mongolian gerbil and auditory stimulated action potentials were recorded from the inferior colliculus. Spontaneous firings of fifth (trigeminal) nerve fibers were also inhibited using the optogenetic protein Halorhodopsin. Moreover, a noise model of the system was derived to guide the design.
Significance: A single IC to measure and control action potentials using optogenetic proteins is realized so that more complicated behavioral neuroscience research and the translational neural disorder treatments become possible in the future.

Architecture

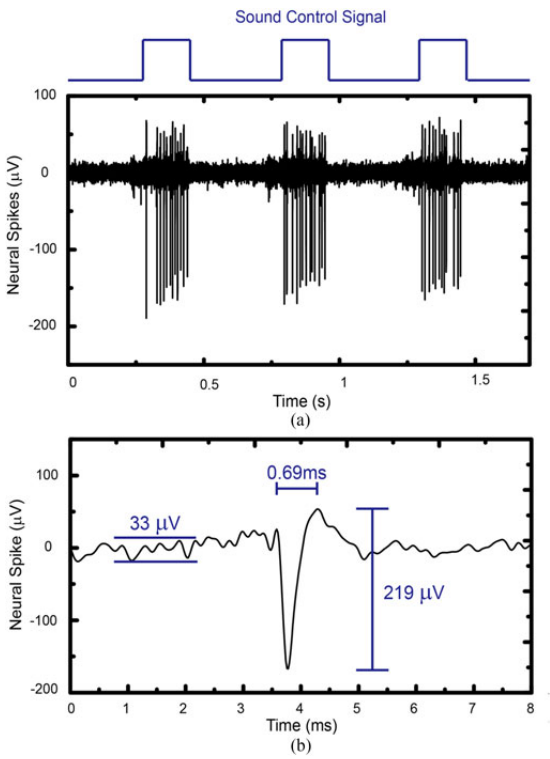


Result I





Result II



In ISSCC 2017

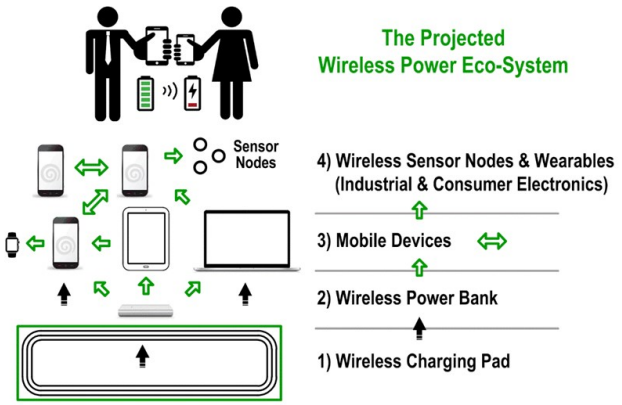
Reconfigurable Bidirectional Wireless Charging Transceiver for Battery-to-Battery Wireless Charging

Mo Huang, Yan Lu, Seng-Pan U, and R. P. Martins

From Integrated Power research line

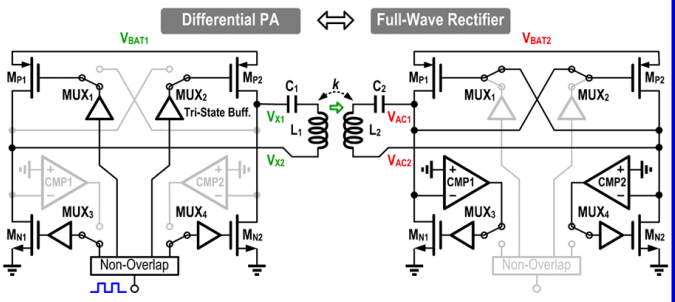
Motivation

Wireless power transfer (WPT) is currently on the critical point of an explosive growth. To enable the mobile devices charging others without additional hardware, we propose a reconfigurable bidirectional WPT transceiver (TRX) that reuses the LC resonant tank and the area consuming power transistors for the Class-D power amplifier (PA) and the AC-DC converter (rectifier).



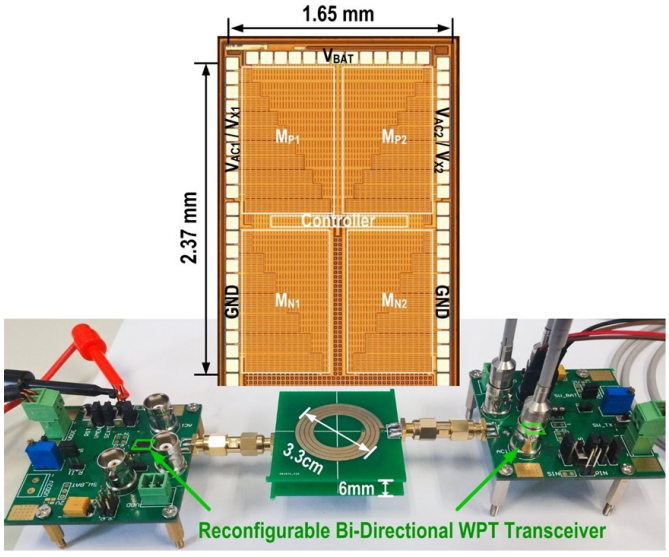
Architecture

Since the power transistors occupy a large silicon area, and the differential Class-D PA and the full-wave active rectifier have very similar symmetrical architectures, The figure shows the proposed reconfigurable WPT TRXs that reuses the power transistors and the series resonant tank. For reconfigurations, we use small size gate-drive multiplexers (MUX1–4) that only deal with signals (not power). In the TX mode, non-overlapping signals control 4 power transistors, which operate as a differential Class-D PA, and drive the LC tank. In the RX mode, we cross-connect MP1 and MP2, while MN1 and MN2 are controlled by the comparators, acting as active diodes.



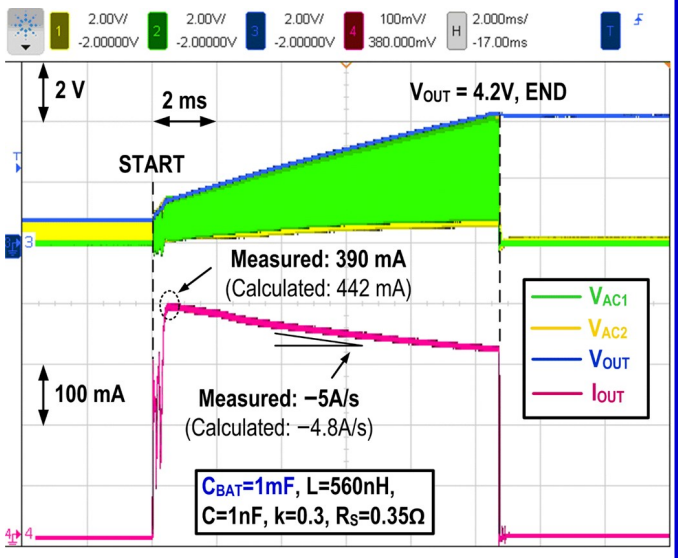
Implementation

The proposed reconfigurable wireless power TRX was fabricated in a 0.35-μm CMOS process with thick metal-4 option.



Verification

Measured AC input voltage, charging current and output voltage when charging a 1-mF capacitor.



In RSC Lab on a Chip 2017

A 3D Microblade Structure for Precise and Parallel Droplet Splitting on Digital Microfluidic Chips

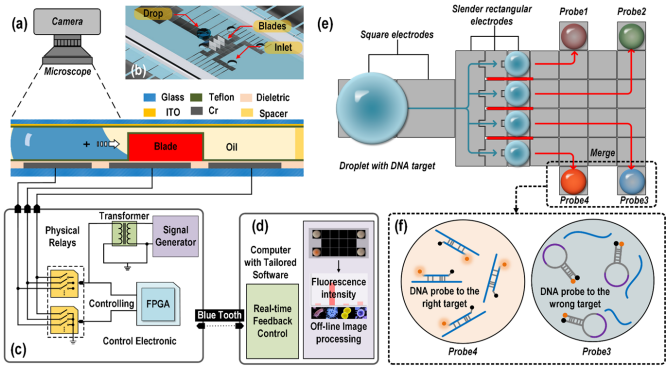
Cheng Dong, Yanwei Jia, Jie Gao, Tianlan Chen, Pui-In Mak, Mang-I Vai, and R. P. Martins

From Multidisciplinary Research Area (Microfluidics)

Motivation

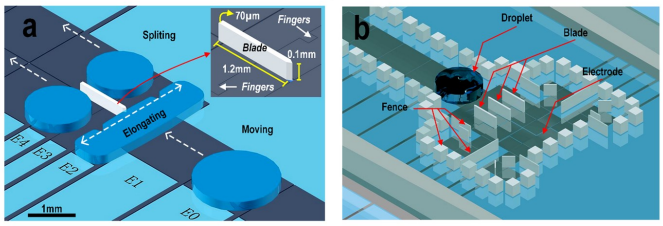
Existing digital microfluidic (DMF) chips exploit the electrowetting on dielectric (EWOD) force to perform droplet splitting. However, the current splitting methods are not flexible and the volume of the droplets suffers from large variation. Herein, we propose a DMF chip featuring a 3D microblade structure to enhance the droplet-splitting performance. By exploiting the EWOD force for shaping and manipulating the mother droplet, we obtain an average dividing error of <2% in the volume of the daughter droplets for a number of fluids such as deionized water, DNA solutions and DNA protein mixtures. Customized droplet splitting ratios of up to 20:80 are achieved by positioning the blade at the appropriate position. Additionally, by fabricating multiple 3D microblades on one electrode, two to five uniform daughter droplets can be generated simultaneously. Finally, by taking synthetic DNA targets and their corresponding molecular beacon probes as a model system, multiple potential pathogens that cause sepsis are detected rapidly on the 3D-blade-equipped DMF chip, rendering it as a promising tool for parallel diagnosis of diseases.

Architecture



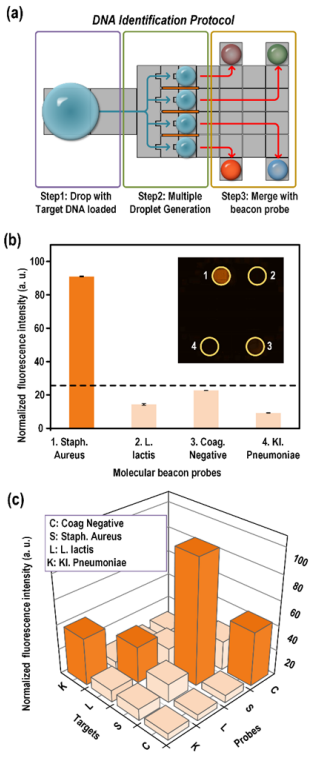
Schematic of the digital microfluidic system for droplet splitting with 3D micro-blade structure. (a) System set up. (b) Schematic of the DMF chip. (c) The electronic module for the DMF chip operation. (d) A computer installed with custom software for droplet control and data analysis. (e) Top view of the blade. (f) Principles of DNA detection.

Implementation



Schematic and operation of a DMF chip fabricated with on-chip microstructures. (a) The DMF chip with a single on-chip blade for 50/50 splitting. (b) The DMF chip fabricated with blades for quarter-splitting and a fence to prevent drifting.

Verification



The system has been successfully utilized in the DNA identification of possible pathogens causing Sepsis

Fast on chip DNA identification using an on-chip blade for the generation of multiple droplets. (a) Protocol of the probe-target hybridization assay. (b) The normalized fluorescence intensity taken from one of the assays, in which the mother droplet contained Staph. Aureus target. (c) Fluorescence profiles of the mixtures of each probe target combination.

Technology Transfer Office and Commercialization Activities

2017 was the 2nd year after the startup of our Technology Transfer Office (TTO). The TTO has made significant effort on building a good connection with strategic partners, coordinating the collaboration projects and supporting the growth acceleration of a future spin-off company, as well as participating in various activities relevant to technology transfer to understand and share experiences with external experts.

Attended AUTM Asia 2017 in HK with UM Colleagues

Invited VIP to participate in the Mainland and HK SAR, Macao SAR Intellectual Property Symposium 2017

Strategic Industrial Partnership

SKL AMS-VLSI has been actively collaborating with Pearl-Delta-Area industrial IC leaders on advancing knowledge and best practice in IC research, design, development and fabrication. In 2017, SKL AMS-VLSI has signed mutual collaboration Memorandum Of Understanding (MOU) with six companies and Zhuhai South IC Design Service Center that cover potential collaborations in integrated power IC design, electronic power, bioelectronics and RF mixed-signals.

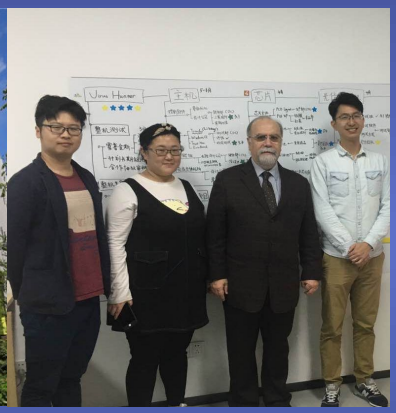
Selected on-going projects

1. Ultra-Low Standby Current DC to DC converter in IoT application.
2. Multi-output Switching Capacitor Type DC to DC converter for Multimedia SoC.

Spin-off Company

Technology Dissemination and Marketing - China High Tech Fair, Shenzhen, 2017

Starting-up activity in UMTEC / Zhuhai UM Research Institute, Inno Valley, Hengqin, China



US Patents Granted in 2017

1. “Electrode-Voltage Waveform for Droplet-Velocity and Chip-Lifetime Improvements of Digital Microfluidic Systems,” US Patent, No. 9,808,800, **Nov. 2017.**
2. “Reagents and Methods of PCR,” US Patent, Granted, No. 9758813, **Sep. 2017.**
3. “Electronic Module for Real-Time Droplet-Position Sensing and Driving in Digital Microfluidic System,” US patent, No. 9,751,083, **Sep. 2017.**
4. “Gain-Boosted N-path Passive-Mixer-First Receiver with a Single-Mixing Step,” US Patent, No. 9,680,448, **Jun. 2017.**
5. “Radio-Frequency-to-Baseband Function-Reuse Receiver with Shared Amplifiers for Common-Mode and Differential-Mode Amplification,” US Patent, No. 9,673,781, **Jun. 2017.**
6. "Mixed signal controller," US Patent, No. 9,692,232, **Jun. 2017.**
7. “Manipulation of Fluids, Fluid Components and Reactions in Microfluidic Systems,” US Patent, No. 9588025, **Mar. 2017.**

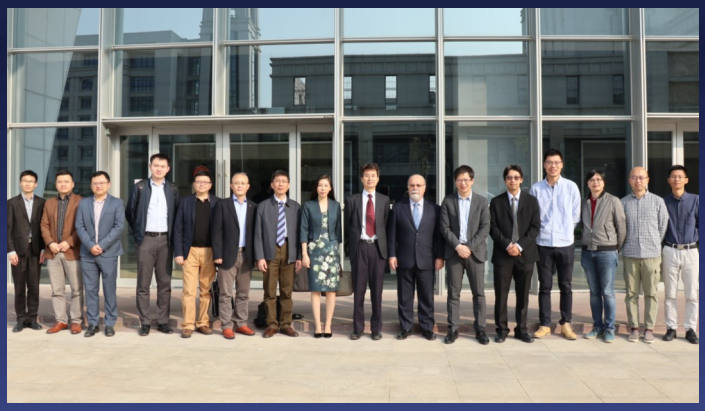
Events and Visits

Visit by Delegation of China Association for Science and Technology (CAST)

Visit by Delegation of China Ministry of Science and Technology (MOST)

Visit by Delegation of Macao Science and Technology Development Fund (FDCT)

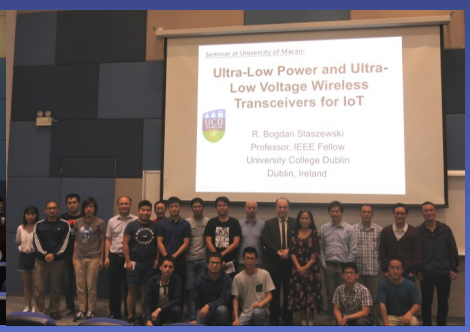
Visit by Chinese Academy of Sciences (CAS)



Distinguished Lectures and Workshops

"Talks by the Chinese Academy of Sciences" by
Prof. CHEN Jie & Prof. YANG Haigang,
Researcher, CAS Institute of Microelectronics
& Researcher, CAS Institute of Electronics

"State Key Laboratory of Analog and Mixed-Signal VLSI: IEEE CAS Seasonal School 2017"
by
Professors, Associate Professors and Assistant Professors from Macao, Hong Kong, Taiwan, China and Japan



"Ultra-Low Power and Ultra-Low Voltage Wireless Transceivers for IoT" by
Prof. Robert Bogdan Staszewski,
IEEE Fellow, University College Dublin

Upholding Scientific Leadership in ISSCC Benchmark in Terms of State-of-The-Art Chips

Academy in China	2011	2012	2013	2014	2015	2016	2017	2018	Total
University of Macau ★	2	1	1	3	2	3	6	7	25
HKUST	1	1	2	3	4	3	4	2	20
Fudan Univ.	1	1	2	1				2	7
Tsinghua Univ.	1			2		1			4
Chinese Acad. Sci.	1		1	1					3
Peking Univ.								1	1
Chengdu UESTC								1	1

★ **Awards and Student Research Previews (PhD) in 2011 - 2018:**

2 ISSCC Silk-Road Awards **5 SSCS Pre-Doctoral Awards**

12 ISSCC Student Research Previews **1 Best Paper Far-East (2018)**

Books (2)

- "*Handheld Total Chemical and Biological Analysis Systems - Bridging NMR, Digital Microfluidics and Semiconductors*," ***Springer***, **2018.**
- "*Tutorials in Circuits and Systems Selected Topics in Power, RF, and Mixed-Signal ICs*," ***River Publishers***, **Dec. 2017.**

Book Chapter

- "Micro-NMR on CMOS for Biomolecular Sensing" in "*CMOS Circuits for Biological Sensing and Processing Systems*", ***Springer***, **2018.**

SCI Journals – 44 Papers (2 in 2018)

- "A 0.7-to-2.5 GHz, 61% EIRP System Efficiency, 4-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and Analog Spatial De-Interleaver," ***IEEE Trans. on CAS I***, **Jan. 2018.**
- "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," ***IEEE Journal of Solid-State Circuits***, **Jan. 2018.**
- "Selective Compensation of Distortion, Unbalanced and Reactive Power of A Thyristor Controlled LC-Coupling Hybrid Active Power Filter (TCLC-HAPF)," ***IEEE Trans. on Power Electronics***, **Dec. 2017.**
- "An Area-Efficient and Tunable Bandwidth-Extension Technique for a Wideband CMOS Amplifier Handling 50+ Gb/s Signaling," ***IEEE Transactions on Microwave Theory and Techniques***, **Dec. 2017.**
- "Fully-Integrated Inductor-less Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting," ***IEEE Journal of Solid-State Circuits***, **Dec. 2017.**
- "A Digital Microfluidic System for Loop-Mediated Isothermal Amplification and Sequence Specific Pathogen Detection," ***Scientific Reports – Nature***, **Nov. 2017.**
- "A High-Voltage-Enabled Class-D Polar PA Using Interactive AM-AM Modulation, Dynamic Matching, and Power-Gating for Average PAE Enhancement," ***IEEE Trans. on CAS I***, **Nov. 2017.**
- "Adaptive Thyristor Controlled LC – Hybrid Active Power Filter for Reactive Power and Current Harmonics Compensation with Switching Loss Reduction," ***IEEE Trans. on Power Electronics***, **Oct. 2017.**
- "A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing," ***IEEE Transactions on Circuits and Systems-I: Regular Papers***, **Oct. 2017.**
- "60-dB SNDR 100-MS/s SAR ADCs With Threshold Reconfigurable Reference Error Calibration," ***IEEE Journal of Solid-State Circuits***, **Oct. 2017.**
- "A 27-Gb/s Time-Interleaved Duobinary Transmitter Achieving 1.44-mW/Gb/s FOM in 65-nm CMOS," ***IEEE Microwave and Wireless Components Letters***, **Sep. 2017.**
- "Drug Screening of Cancer Cell Lines and Human Primary Tumors Using Droplet Microfluidics," ***Scientific Reports – Nature***, **Aug. 2017.**
- "A 0.038mm^2 SAW-less Multi-Band Transceiver Using an N-Path SC Gain Loop," ***IEEE Journal of Solid-State Circuits***, **Aug. 2017.**
- "A 7.8mW 5b 5GS/s Dual-Edges-Triggered Time-Based Flash ADC," ***IEEE Transactions on Circuits and Systems I: Regular paper***, **Aug. 2017.**
- "Digital 2-/3-Phase Switched-Capacitor Converter With Ripple Reduction and Efficiency Improvement," ***IEEE Journal of Solid-State Circuits***, **Jul. 2017.**
- "Exploring the Behavior of Water Nanodroplet on a Coplanar Electrowetting-on-Dielectric: A Molecular Dynamics Approach," ***IET Micro & Nano Letters***, **Jul. 2017.**
- "A 12b 180MS/s 0.068mm^2 with Full-Calibration-Integrated Pipelined-SAR ADC," ***IEEE Transactions on Circuits and Systems I: Regular paper***, **Jul. 2017.**
- "A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) Pout," ***IEEE Journal of SSC***, **Jun. 2017.**
- "Design and Analysis of Energy Recyclable Bidirectional Converter with Digital Controller for Multichannel Microstimulators," ***Springer Analog Integrated Circuits and Signal Processing***, **Jun. 2017.**
- "LC-VCOs Using Spiral Inductors with Single- and Dual-Layer Patterned Floating Shields - A Comparative Study," ***Springer Analog Integrated Circuits and Signal Processing***, **Jun. 2017.**
- "A Sub-1V 78-nA Bandgap Reference with Curvature Compensation," ***Elsevier Microelectronics Journal***, **May 2017.**
- "Analysis in the effect of Co-phase Traction Railway HPQC Coupled Impedance on its Compensation Capability and Impedance-Mapping Design Technique based on Required Compensation Capability for Reduction in Operation Voltage," ***IEEE Transactions on Power Electronics***, **Apr. 2017.**
- "A 0.35-V 520-μW 2.4-GHz Current-Bleeding Mixer with Inductive-Gate and Forward-Body Bias, Achieving >13-dB Conversion Gain and >55-dB Port-to-Port Isolation," ***IEEE Trans. on MTT***, **Apr. 2017.**
- "A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting systems," ***IEEE Trans. on Circuits and Systems – I***, **Apr. 2017.**
- "A 0.45-V 147-to-375 nW ECG Compression Processor with Wavelet Shrinkage and Adaptive Temporal Decimation Architectures," ***IEEE Transactions on VLSI Systems***, **Apr. 2017.**
- "Direct Measurement of Elbow Joint Angle Using Galvanic Couple System," ***IEEE Transactions on Instrumentation and Measurement***, **Apr. 2017.**
- "Modeling and Parameter Design of Thyristor Controlled LC-Coupled Hybrid Active Power Filter (TCLC-HAPF) for Unbalanced Compensation," ***IEEE Transactions on Industrial Electronics***, **Mar. 2017.**
- "AuGd Integrated Nanoprobes for Optical/MRI/CT Triple-Modal in Vivo Tumor Imaging," ***RSC Nanoscale***, **Mar. 2017.**
- "An Integrated Circuit for Simultaneous Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation," ***IEEE Transactions on Biomedical Engineering***, **Mar. 2017.**
  [Top 50 most accessed paper: Mar. 2017 - Apr. 2018]
- "Reconfigurable Mismatch-Free Time-Interleaved Bandpass Sigma-Delta Modulator for Wireless Communications," ***IET Electronics Letters***, **Mar. 30, 2017.**
- "Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial V_{cm}-Based Switching," ***IEEE Transactions on VLSI Systems***, **Mar. 2017.**
- "A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting," ***IEEE Transactions on Circuits and Systems II***, **Feb. 2017.**
- "A Dual-Output Wireless Power Transfer System with Active Rectifier and Three-Level Operation," ***IEEE Transactions on Power Electronics***, **Feb. 2017.**
- "Global Digital Controller for Multi-channel Micro-Stimulator with A 5-Wire Interface Featuring On-the-fly Power-Supply Modulation and Tissue Impedance Monitoring," ***Elsevier Microele. J.***, **Feb. 2017.**
- "A Multiphase Switched-Capacitor DC–DC Converter Ring With Fast Transient Response and Small Ripple," ***IEEE Journal of Solid-State Circuits***, **Feb. 2017.**
- "A 3D Microblade Structure for Precise and Parallel Droplet Splitting on Digital Microfluidic Chips," ***RSC Lab on a Chip***, **Feb. 2017.**
- "DCM Operation Analysis of 3-Level Boost Converters," ***IET Electronics Letters***, **Feb. 2017.**
- "Unbalanced Control Strategy for A Thyristor Controlled LC-Coupling Hybrid Active Power Filter in Three-Phase Three-Wire Systems", ***IEEE Transactions on Power Electronics***, **Feb. 2017.**
- "DCM Operation Analysis of 3-Level Boost Converters," ***IET Electronics Letters***, **Feb. 16, 2017.**
- "A Single-Chip Solar Energy Harvesting IC Using Integrated Photodiodes for Biomedical Implant Applications," ***IEEE Transactions on Biomedical Circuits and Systems***, **Feb. 2017.**
- "Metastability in SAR ADCs," ***IEEE Transactions on CAS – Part II: Express Briefs***, **Feb. 2017.**
- "A Handheld High-Sensitivity Micro-NMR CMOS Platform With B-Field Stabilization for Multi-Type Biological/Chemical Assays," ***IEEE Journal of Solid-State Circuits***, **Jan. 2017.**
- "Active–Passive ΔΣ Modulator for High-Resolution and Low-Power Applications," ***IEEE Transactions on VLSI Systems***, **Jan. 2017.**
- "A 10-bit 500-MS/s Partial-Interleaving Pipelined SAR ADC With Offset and Reference Mismatch Calibrations," ***IEEE Transactions on VLSI Systems***, **Jan. 2017.**

Conferences – 26 Papers (2 in 2018)

Major IEEE solid-state circuits conferences:

IEEE Asian Solid-State Circuits Conference (ASSCC 2017), Grand Hilton Hotel, Seoul, Korea, **Nov. 2017**

- "A 5.35 mW 10 MHz Bandwidth CT Third-Order ΔΣ Modulator with Single Opamp Achieving 79.6/84.5 dB SNDR/DR in 65 nm CMOS"
- "A 5-bit 2 GS/s Binary-Search ADC with Charge-Steering Comparators"

IEEE European Solid-State Circuits Conference (ESSCIRC 2017), Leuven, Belgium, **Sep. 2017**

- "A Missing-Code-Detection Gain Error Calibration Achieving 63dB SNR for An 11-bit ADC"

IEEE International Solid-State Circuits Conference (ISSCC 2017), San Francisco, CA, USA, **Feb. 2017**

- "A 1.7mm^2 Inductor-less Fully-Integrated Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting with 483% Power Extraction Enhancement"
- "A Reconfigurable Bidirectional Wireless Power Transceiver with Maximum Current Charging Mode and 58.6% Battery-to-Battery Efficiency"
- "An Output-Capacitor-Free Analog-Assisted Digital Low-Dropout Regulator with Tri-loop Control"
- "A Dual-Symmetrical-Output Switched-Capacitor Converter with Dynamic Power Cells and Minimized Cross Regulation for Application Processors in 28nm CMOS"
- "A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration"
- "A 0.18V 382μW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS"
- "A 0.23-to-2.4V Input Fully Integrated Buck-Boost SC DC-DC Converter with Cell-Spliced Power Stage and Domain-Adaptive Switch Driver" **[Student Research Preview]**
- "A 550nW MEMS Readout Interface Using an Iterative-Incremental ADC Achieving Energy-Efficient Capacitance (1.2pJ/conv.-Step) and Temperature (3.6nJ%2) Sensing" **[Student Research Preview]**

Other IEEE conferences:

IEEE 1st International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Hamilton, New Zealand, **Jan. 2018**

- "A 97.0% Maximum Efficiency, Fast Response, Low Voltage Ripple KY Boost Converter for Photovoltaic Application"

IEEE Asia and South Pacific Design Automation Conference (ASP-DAC 2018), Jeju, Korea, **Jan. 2018**

- "A Dual-Output SC Converter with Dynamic Power Allocation for Multi-Core Application Processors"

International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS), Savannah, Georgia, USA, **Oct. 2017**

- "Digital Microfluidic Platform for False-Positive-Free Loop-Mediated Isothermal Amplification"

The 43rd Annual Conference of the IEEE Industrial Electronics Society (IECON 2017), Beijing, China, **Oct. 2017**

- "CCM Operation Analysis and Parameter Design of Negative Output Elementary Luo Converter for Ripple Suppression"
- "Delta-Connected Static Var Compensator (SVC) based Hybrid Active Power Filter (SVC-HAPF) and Its Control Method"

IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), Hsinchu, Taiwan, China, **Oct. 2017**

- "A Wide Range High Efficiency Fully Integrated Switched-Capacitor DC-DC Converter with Fixed Output Spectrum Modulation"
- "Ultra-low Power QRS Detection using Adaptive Thresholding based on Forward Search Interval Technique"

IEEE International Symposium on Industrial Electronics (ISIE 2017), Edinburgh, Scotland, UK, **Jun. 2017**

- "A Digital PWM Controlled KY Step-Up Converter based on Frequency Domain ΣΔ ADC"

IEEE International Future Energy Electronics Conference 2017 – ECCE Asia (IFEEC 2017-ECCE Asia), Kaohsiung, Taiwan, China, **Jun. 2017**

- "A Digital PWM Controlled KY Step-Up Converter Based on Passive Sigma-Delta Modulator"

IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, Hawaii, USA, **Jun. 2017**

- "A 0.7 to 1 GHz Switched-LC N-Path LNA Resilient to FDD-LTE Self-Interference at ≥40 MHz Offset"

IEEE Ph.d. Research in Microelectronics and Electronics Conference (PRIME 2017), Taormina, Italy, **Jun. 2017**

- "Split-Based Time-interleaved ADC with Digital Background Timing-skew Calibration"

IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, **May 2017**

- "Piecewise BJT Process Spread Compensation Exploiting Base Recombination Current"
- "A 310nW 14.2-Bit Iterative-Incremental ADC for Wearable Sensing Systems"
- "A 0.4V 4.8μW 16MHz CMOS Crystal Oscillator Achieving 74-Fold Startup-Time Reduction Using Momentary Detuning"

Symposium on Power Electronics and Electrical Drivers (SPEED), Changsha, China, **Apr. 2017**

- "Thyristor Controlled LC Filter and Its Control Method"