澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

模拟与混合信号
超大规模集成电路
国家重点实验室
（澳门大学伙伴实验室）
State Key Laboratory of Analog and Mixed - Signal VLSI
(Partner Laboratory in University of Macau)
中华人民共和国科学技术部

AMSV
State Key Laboratory of
Analog and Mixed-Signal VLSI
模擬與混合信號超大規模集成電路國家重點實驗室

State Key Lab of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) Newsletter

Motto: "Locally, from (World) Quality towards (National) Quantity"

座右銘:立足本土、人才培養, 以世界級質量創建國家級規模

Year 3
No . 3

2013 Milestones

February 2014

Events

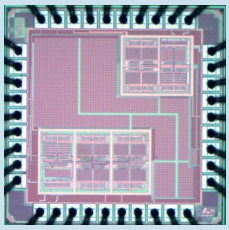
State Key Laboratory of Analog and Mixed-Signal VLSI (AMS-VLSI Lab) has passed the Mid-term Assessment by *Ministry of Science and Technology (MOST)* of the People's Republic of China and Macao *Science and Technology Development Fund (FDCT)*

Prof. Seng-Pan U named 2012 Scientific Chinese

Macao Chapter of IEEE Solid-State Circuits Society received 2012 World Chapter of the Year Award at 60th IEEE *International Solid-State Circuits Conference ISSCC - 2013*

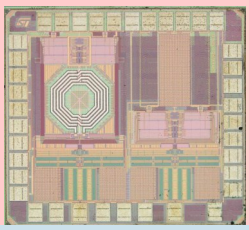
State-of-the-Art Chips - Designed and Tested in 2013 (10 chips)

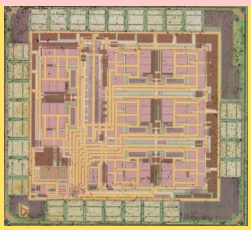
Wireless Chips (65 nm)



High-Performance SC Lowpass Filter

Multi-band ZigBee Receiver

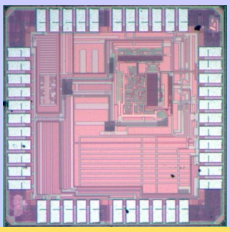


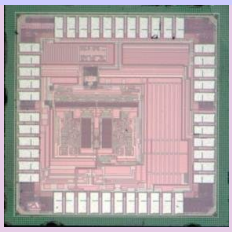


Wideband radio receiver for TV-band application

DCSP Chips (65 nm)

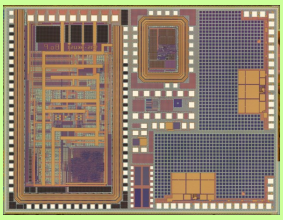
An high resolution pipeline SAR ADC for cable TV system

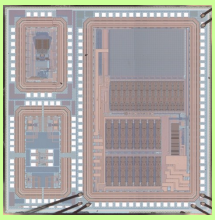


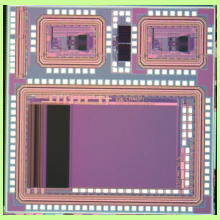


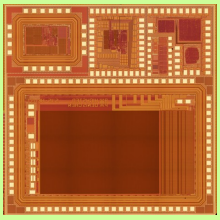
An interleaved pipeline SAR ADC with Flash assigned for broad band

BME (Biomedical Engineering) Chips (0.18 μm)









Biomedical sensor circuits with energy harvesting

ISSCC 2014

Three state-of-the-art chips with outstanding performance in analog, radio frequency, and wireless, co-developed by UM faculty members and students, have been accepted for presentation at the 61st IEEE International Solid-State Circuits Conference (**ISSCC**), which was held in **February 2014**, in San Francisco, United States. ISSCC is internationally recognized as the "**Chip Olympics**", and UM was this year in the top ten universities with more papers at ISSCC.

The 3 papers from UM were "An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF", "A 0.5V 1.15mW 0.2mm^2 Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components", and "A 0.0013mm^2 3.6μW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Loads with >62° Phase Margin". The three related students, **Yan Zushu**, **Lin Fujian** and **Lin Zhicheng**, are supervised by Chair Professor Rui Martins and Prof. Elvis Mak Pui In.

IEEE SSCS Pre-doctoral Achievement Award

For a small number of promising graduate students, IEEE-SSCS Predoctoral Achievement Awards provide a $1000 honorarium and reimbursement for travel expenses (within certain limits) to ISSCC, the Society's flagship conference, which has been taken place on 9 - 13 February 2014. Yan Zushu become one of the winners of **IEEE-SSCS Predoctoral Achievement Awards 2014**, and together with another Ph.D student from HKUST, they were the two first recipients from China, HK and Macao to get this award since 1983.

Applicants must be members of IEEE and the Solid State Circuits Society and have completed at least one year of study in a Ph.D. program in the area of solid-state circuits. Awards are attributed on the basis of academic record and promise, quality of publications, and a graduate study program well matched to the charter of SSCS. Prior winners of the Predoctoral Achievement Award are not eligible. No more than two Awards will be granted in a given year to students of one Principal Advisor.


IEEE Solid-State Circuits Society

is pleased to present a
2013-2014 Pre-Doctoral Achievement Award to

Zushu Yan

Bill Bidermann
President
IEEE Solid-State Circuits Society

IEEE
Advancing Technology for Humanity

Presented February 9, 2014

US Patents granted in 2013

1. **U Fat Chio, He Gong Wei, Yan Zhu, Sai Weng Sin, Seng-Pan U, R. P. Martins, Franco Maloberti**, "Cascade Analog to Digital Converting System", *US Patent*, US 8,466,823 B2, **Jun. 18, 2013**.
2. **He Gong Wei, U Fat Chio, Sai Weng Sin, Seng-Pan U, R. P. Martins**, "Delay Generator", *US Patent*, No. US8,441,295 B2, **May 14, 2013**.
3. **Sai Weng Sin, He Gong Wei, Li Ding, Yan Zhu, Chi Hang Chan, U Fat Chio, Seng-Pan U, R. P. Martins, Franco Maloberti**, "A Time-Interleaved Pipelined-SAR Analog to Digital Converter with Low Power Consumption", *US Patent*, No. 8,427,355, **Apr. 23, 2013**.
4. **Yan Zhu, Chi Hang Chan, U Fat Chio, Sai Weng Sin, Seng-Pan U, R. P. Martins, Franco Maloberti**, "N-Bits Successive Approximation Register Analog-to-Digital Converting System", *US Patent*, US8344931 B2, **Jan. 01, 2013**.

Selected works from each research line *in JSSC 2013*

A 5-bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65nm CMOS

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, Franco Maloberti

Motivation

Low-power for portable devices in Ultra-Wideband (UWB) and Wireless Personal Area Network (WPAN) applications.

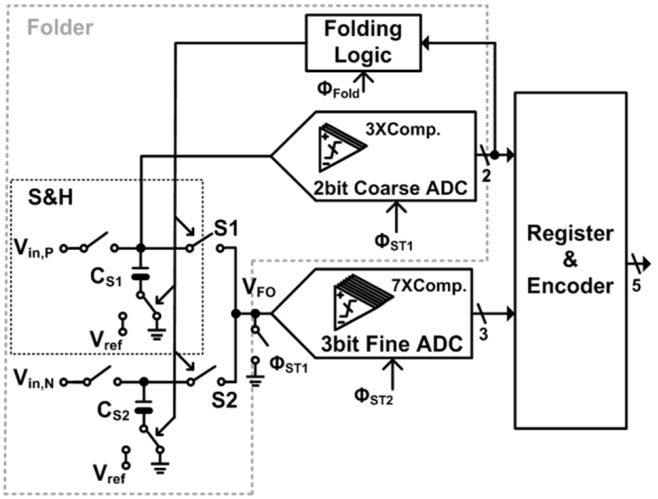
Conventional folding ADC demands a steep trade-off amount of power and bandwidth in the folder. The proposed work adopts simple switched-capacitor operation to relax this constraint.

Threshold voltages of comparators are embedded thus saving a power hungry reference ladder.

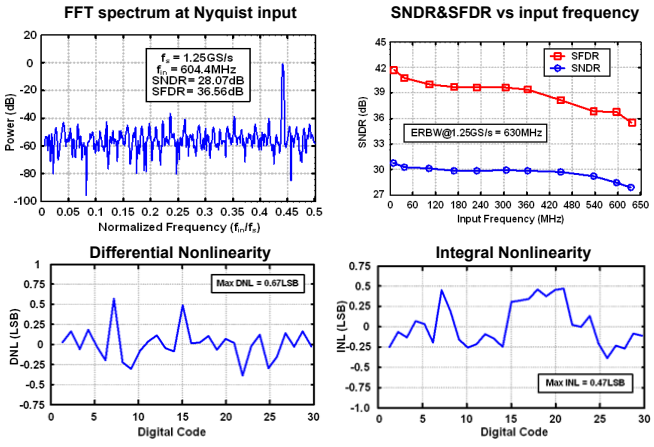
Non-linearity in the folding operation is calibrated on-chip through various proposed schemes.

Best energy efficient gigahertz sampling rate ADC when compared with state-of-the-art.

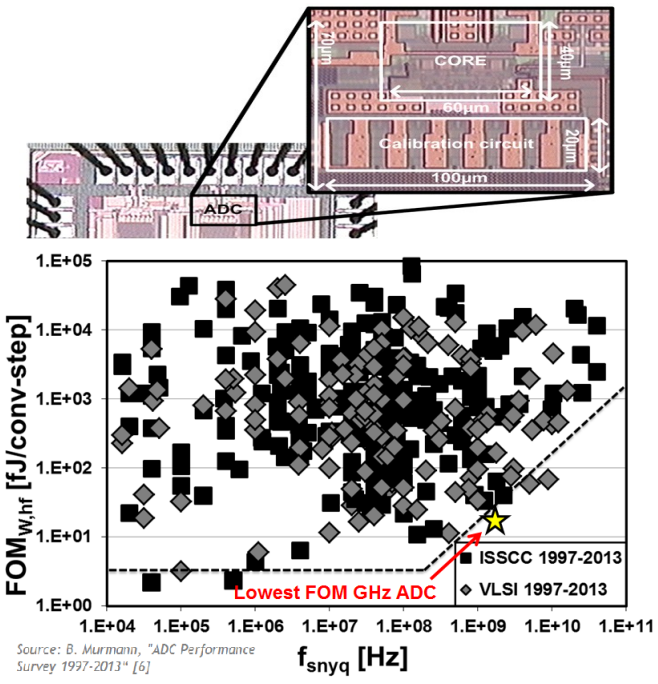
Architecture



Verification I



Verification II



in ISSCC 2013 and JSSC 2014

A 1.7mW 0.22mm^2 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65nm CMOS

Zhicheng Lin, Pui-In Mak and Rui P. Martins

Motivation

An extensive-current-reuse 2.4GHz ZigBee RX vertically unifies a passive-/active-gain-boosted Balun-LNA-I/Q-Mixer (Blixer) with a hybrid filter in one cell.

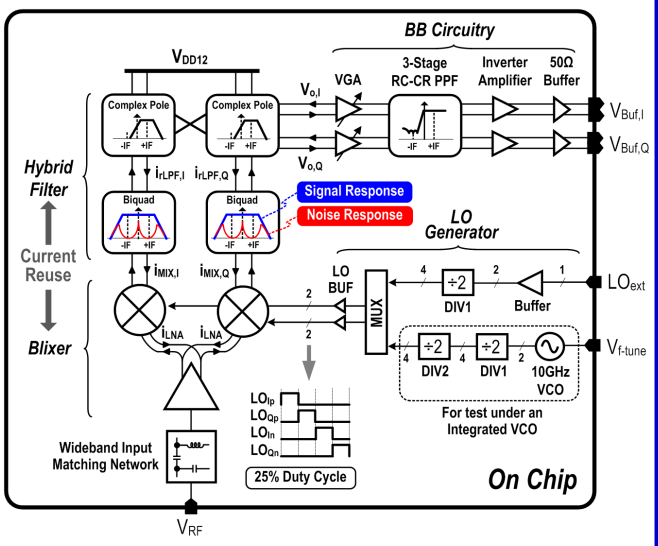
The Blixer matches a wideband S_{11} with no external components.

The hybrid filter merges an IF-noise-shaping Biquad with a complex-pole load, offering 3rd-order channel selection and 1st-order image rejection directly atop the Blixer.

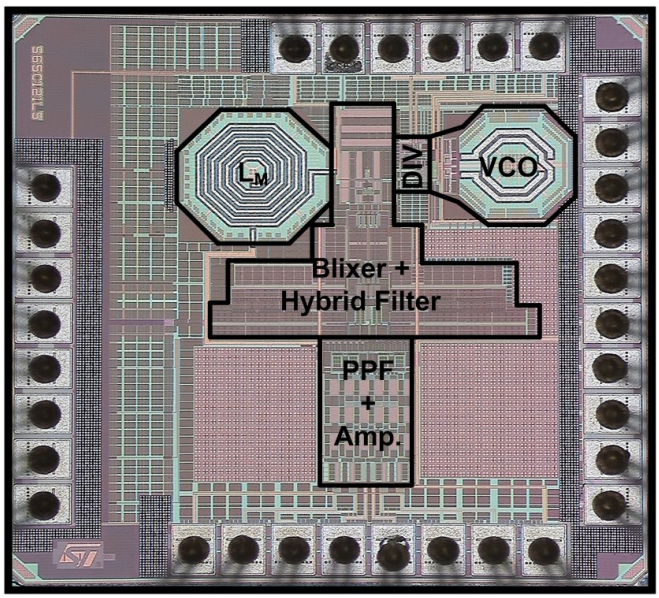
The RX measures 8.5dB NF, 57dB gain, 36dB IRR and –6dBm IIP3.

The die consumes 1.7mW and 0.22mm^2 in 65nm CMOS.

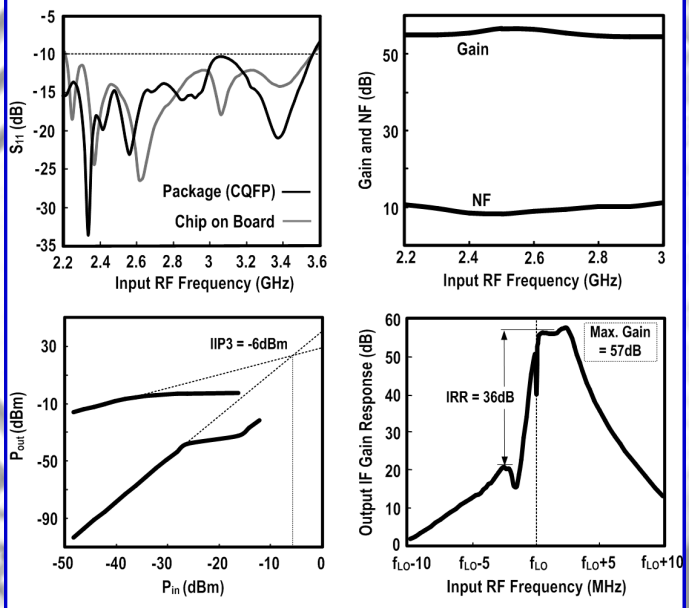
Architecture



System Implementation



Verification



in TBioCAS 2013

15-nW Biopotential LPFs in 0.35-μm CMOS Using Subthreshold-Source-Follower Biquads with and without Gain Compensation

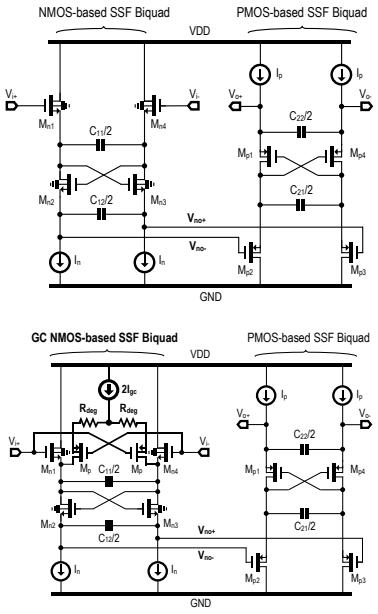
Tan-Tan Zhang, Pui-In Mak, Mang-I Vai, Peng-Un Mak, Man-Kay Law, Sio-Hang Pun, Feng Wan and Rui P. Martins

Motivation

Most biopotential readout front-ends rely on the g_m-C lowpass filter (LPF) for forefront signal conditioning. A small g_m realizes a large time constant ($\tau = C/g_m$) suitable for ultra-low-cutoff filtering, saving both power and area. Yet, the noise and linearity can be compromised, given that each g_m cell can involve one or several noisy and nonlinear V-I conversions originated from the active devices. This work proposes the subthreshold-source-follower (SSF) Biquad as a prospective alternative. It features: 1) a very small number of active devices reducing the noise and nonlinearity footsteps; 2) no explicit feedback in differential implementation, and 3) extension of filter order by cascading.

A gain-compensation (GC) scheme addressing the gain-loss problem of NMOS-based SSF Biquad due to the body effect is also proposed. Two 100-Hz 4th-order Butterworth LPFs using the SSF Biquads with and without GC were fabricated in 0.35-μm CMOS.

Architecture



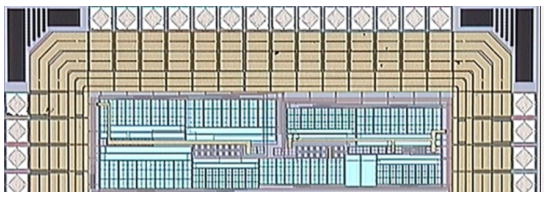
Non-GC LPF

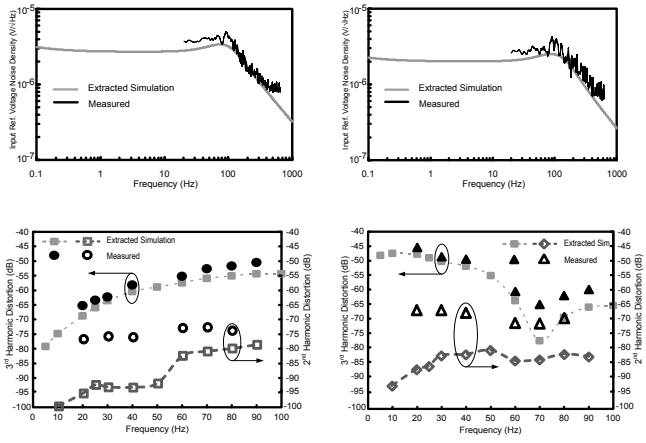
- Biased in sub-threshold region to achieve ultra low power consumption
- Inherent feedback in source follower to maintain high linearity

GC LPF

- Enhance the DC gain.
- Optimize the linearity with harmonic distortion cancellation
- Improve the noise performance.

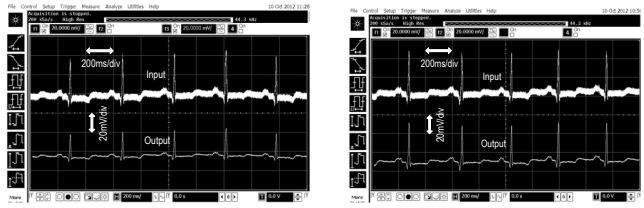
Experimental Result





Measured and simulated performances for non-GC LPF (left) and GC LPF (right).

Verification



Arrhythmic ECG signals before and after filtering with non-GC LPF (left) and GC LPF (right).

Summary and Benchmark with Prior Arts.

	TBIOCAS'09 [15]	EL'10 [25]	TBIOCAS'10 [26]	This Work	
				Non-GC LPF	GC LPF
VDD	1 V	1 V	1.8 V	**3 V**	**3 V**
CMOS Technology	0.18 μm	0.18 μm	0.18 μm	**0.35 μm**	**0.35 μm**
Filter Order (Topology [a])	5 (D)	4 (D)	9(S)	**4 (D)**	**4 (D)**
BW	250 Hz	732 Hz[b]	3 KHz	**100 Hz**	**100 Hz**
Integrated IRN voltage	<340 μV_{rms}	50 μV_{rms}	~564 μV_{rms}[c]	**36 μV_{rms} (0.1 to 100 Hz)**	**29 μV_{rms} (0.1 to 100 Hz)**
HD3	-49 dB @ f_{in}=50 Hz, V_{out}=9.43 mV_{p-p}	<-40 dB @ f_{in}=700 Hz, V_{out}= N/A	<-38.4 dB @ f_{in}= 1 KHz, V_{out}=40 mV_{p-p}	**-55.2 dB** @ f_{in}=60 Hz, V_{out}=50 mV_{p-p}	**-60.7 dB** @ f_{in}=60 Hz, V_{out}=50 mV_{p-p}
DR	50 dB	55 dB	34 dB	**66.7 dB**	**64.8 dB**
Power	0.453 μW	14.4 nW	360 nW	**15 nW**	**15 nW**
DC Gain	-10.5 dB	-6 dB	~0 dB	**-3.7 dB**	**0 dB**
Active Area	0.13 mm^2	0.13 mm^2	0.03 mm^2	**0.11 mm^2**	**0.08 mm^2**
FoM	7.25 x 10^{-12}	0.89 x 10^{-13}	3.9 x 10^{-13}	**5.62 x 10^{-13}**	**5.79 x 10^{-13}**

a (S): Single-ended, (D): Differential. b Center frequency of bandpass filter. c Calculated by given input range and DR.

in Lab on a Chip 2013

An Intelligent Digital Microfluidic System with Fuzzy-Enhanced Feedback for Multi-Droplet Manipulation

Jie Gao, Xianming Liu, Tianlan Chen, Pui-In Mak, Yuguang Du, Mang-I Vai, Bingcheng Lin and R. P. Martins

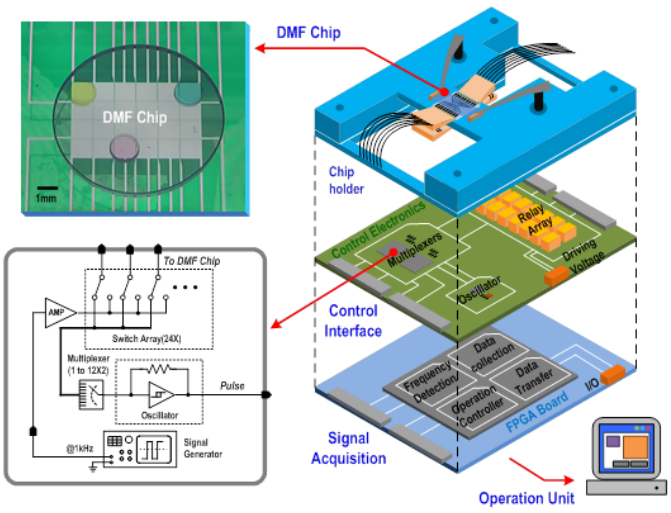
Motivation

This project developed an intelligent digital microfluidic (DMF) technology unifying engineering physics, material science, biochemistry, mixed-signal circuits and systems, as well as advanced control theory to address the intricacy of large-scale microreactors, which could underpin a wide variety of chemical/biological applications in extremely small volumes. The first milestone of this technology is a successful validation of a wide variety of control-engaged droplet manageability such as:

1. Profiling of different droplet's hydrodynamics under real-time trajectory track of droplet-derived capacitance, permitting autonomous multi-droplet positioning without visual setup and heavy image signal processing;
2. Fuzzy-based adaptability of electrode's charging time, enhancing the throughput, fidelity and lifetime of the DMF chip, while identifying and renouncing those weakened electrodes that are deteriorated over time;
3. Expert controllability of multi-droplet routings under counter-measure decisions, preventing droplet-to-droplet or task-to-task interference in real time.

System Implementation

Taken together this work signifies the state-of-the-art most-autonomous DMF module with well-built intelligence, getting one step closer to being manufacturable for a wide multiplicity of life science analyses and combinatorial chemical screening applications.



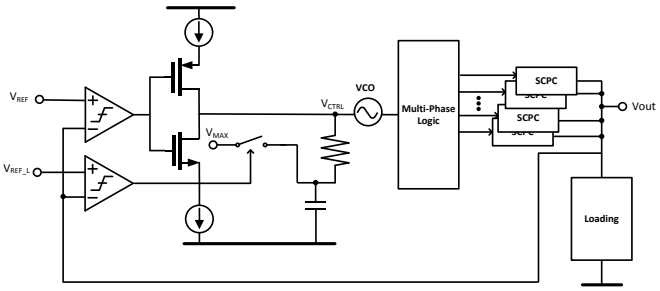
designed in 2013

Fully Integrated Switched Capacitor DC-DC Converter with Fast Transient Frequency Compensation

Guo-Zhi Wen, U-Fat Chio, Sai-Weng Sin, Seng-Pan U and R. P. Martins

Motivation & Architecture

When compared with single boundary multiphase control, the use of voltage-controlled oscillator (VCO) control loop to attain output regulation can provide a more stable operation, thus achieving the smaller output-voltage ripple at steady-state. Cautious frequency compensation is essential for VCO based control loop to ensure that the closed loop is stable, but it will restrain the performance of the load transient, due to the limited loop bandwidth. A switched capacitor DC-DC converter using the proposed frequency compensation technique was fabricated in 65nm CMOS.

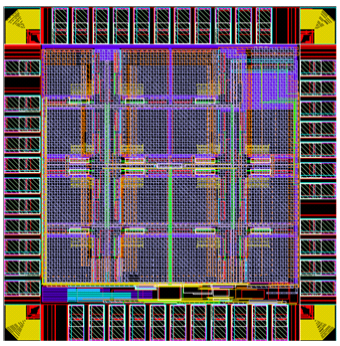


Verification

Performance Summary

Technology	65nm buck
Type	1/2 SC
VIN/VOUT	2.35 V / 1 V
Max Power Density	0.25 W/mm^2
Power Efficiency	76 %
Chip Area	1 mm^2

Chip Layout



Events and Visits

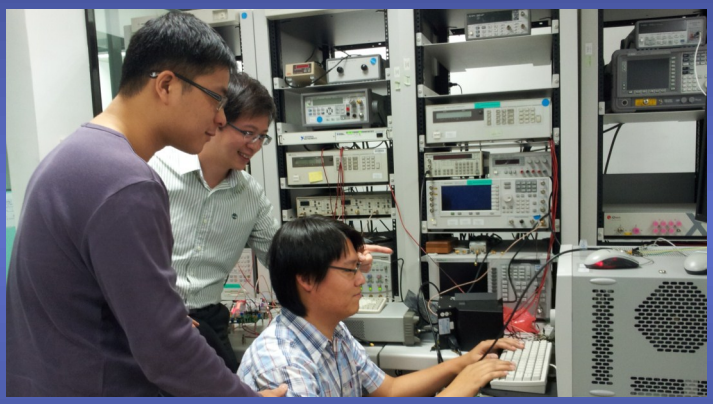
Visit by Dr. Wang Weizhong, Vice-Minister, Ministry of Science & Technology, China

Distinguished Lectures on Microelectronics

SKL Workshop on Fabless Semiconductor by Dr. Rakesh Kumar, President of IEEE Solid-State Circuits Society and Prof. Seng-Pan U

Introduction to Flexray Transceivers for Car Electronics by Prof. Chua-Chin Wang, National Sun Yat-Sen University, Taiwan

Testing and Measurement Environment in SKL AMS – VLSI



Two New Academics Joined SKL AMS-VLSI

We are most delighted with the recruitment of 2 new Assistant Professors to the SKL, original from China and Macao, which will further enhance SKL's competitiveness.

Dr. Yan Zhu received the B.Sc. degree in electrical engineering and automation from the Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau Macao, China, in 2009 and 2011, respectively.

Research interests: Low-power and Wideband Nyquist A/D Converters, ADC's Interface, Ultrasound Image Systems, Digitally Assisted System

Dr. Chi-Seng Lam received the B.Sc., M.Sc. and Ph.D. degrees in Electrical and Electronics Engineering from the University of Macau, Macao, China, in 2003, 2006 and 2012 respectively. In 2013, he was a Postdoctoral Fellow in The Hong Kong Polytechnic University, Hong Kong, China.

Research interests: Integrated Power Electronics Controller, Power Management and Energy Saving Techniques, Power Conversion and Storage, Power Quality Compensations

SCI Journals – 21 Papers

- "Systematic Analysis and Cancellation of Kickback Noise in a Dynamic Latched Comparator", ***Analog Integrated Circuits and Signal Processing, Springer***, **Nov. 2013**
- "A Single-Branch Third-Order Pole-Zero Lowpass Filter with 0.014-mm^2 Die Size and 0.8 kHz (1.25 nW) to 0.94 GHz (3.99 mW) Bandwidth-Power Scalability", ***IEEE Transactions on Circuits and Systems – II***, **Nov. 2013**
- "A 0.013mm^2, kHz-to-GHz-Bandwidth, 3rd-Order All-Pole Lowpass Filter with a 0.52-to-1.11pW/Pole/Hz Efficiency", ***IET Electronics Letters***, **Oct. 2013**
- "15-nW Biopotential LPFs in 0.35-µm CMOS Using Subthreshold-Source-Follower Biquads with and without Gain Compensation", ***IEEE Transactions on Biomedical Circuits and Systems***, **Oct. 2013**
- "Construction of a microfluidic chip, using dried-down reagents, for LATE-PCR amplification and detection of single-stranded DNA", ***Lab on a Chip***, **Sep. 2013**
- "Opportunistic Routing in Intermittently Connected Mobile P2P Networks", ***IEEE Journal on Selected Areas in Communications***, **Sep. 2013**
- "A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS", ***IEEE Journal of Solid-State Circuits***, **Sep. 2013**
- "Design and Performance of an adaptive low dc voltage controlled LC-hybrid active power filter with a neutral inductor in three-phase four-wire power systems", ***IEEE Transactions on Industrial Electronics***, **Aug. 2013**
- "A 53-to-75 mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS", ***IEEE Journal of Solid-State Circuits***, **Aug. 2013**
- "A Non-Recursive Digital Calibration Technique for Joint-Elimination of Transmitter and Receiver I/Q Imbalances with Minimized Add-on Hardware", ***IEEE Transactions on Circuits and Systems – II***, **Aug. 2013**
- "A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC", ***IEEE Journal of Solid-State Circuits***, **Aug. 2013**
- "A 3.6mW 6GHz Current-Reuse VCO-Buffer with Improved Load Drivability in 65nm CMOS", ***Wiley International Journal of Circuit Theory and Applications***, **Jul. 2013**
- "Excess-loop-delay compensation technique for CT ΔΣ modulator with hybrid active-passive loop-filters", ***Analog Integrated Circuits and Signal Processing***, Sprjnger, **Jul. 2013**
- "Pre-emphasis transmitter (0.007 mm^2, 8 Gbit/s, 0–14 dB) with improved data zero-crossing accuracy in 65 nm CMOS", ***IET Electronics Letters***, **Jul. 2013**
- "Analysis of DC-link Voltage Controls in Three-Phase Four-Wire Hybrid Active Power Filters", ***IEEE Transactions on Power Electronics***, **May 2013**
- "A 0.0012mm^2, 8mW, Single-to-Differential Converter with <1.1% Data Cross Error and <3.4ps RMS Jitter up to 14Gb/s Data Rate", ***IET Electronics Letters***, **May 2013**
- "A 3.6-mW 6-GHz current-reuse VCO-buffer with improved load drivability in 65-nm CMOS", ***International Journal of Circuit Theory and Applications, Wiley Online Library***, **May 2013**
- "Hybrid power quality compensator with minimum dc operation voltage design for high-speed traction power systems", ***IEEE Transactions on Power Electronics***, **Apr. 2013**
- "A 0.016-mm^2 144-µW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load with >0.95-MHz GBW", ***IEEE Journal of Solid-State Circuits***, **Feb. 2013**
- "An Intelligent Digital Microfluidic System with Fuzzy-Enhanced Feedback for Multi-Droplet Manipulation", ***Lab on a Chip***, **Jan. 2013**
- "A 5th-Order 20-MHz Transistorized-LC-Ladder LPF with 58.2-dB SFDR, 68-µW/Pole/MHz Efficiency and 0.13-mm^2 Die Size in 90-nm CMOS", ***IEEE Transactions on Circuits and Systems – II***, **Jan. 2013**

Conferences – 25 Papers

Major solid-state circuits conferences

A-SSCC 2013, Singapore, **Nov. 2013**
- "A 0.127-mm^2, 5.6-mW, 5th-Order SC LPF with +23.5-dBm IIP3 and 1.5-to-15-MHz Clock-Defined Bandwidth in 65-nm CMOS"
- "A 13-bit 60M Split Pipelined ADC with Background Gain and Mismatch Error Calibration"
- "A 10.4-ENOB 120MS/s SAR ADC with DAC Linearity Calibration in 90nm CMOS"

ISSCC 2013, San Francisco, CA, USA, **Feb. 2013**
- "A 1.7mW 0.22mm^2 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65nm CMOS" **[Regular Paper]**
- "An Extremely Power-and-Area-Efficient Three-Stage Amplifier for LCD Display Drivers" **[Ph.D. Student Research Preview]**

Other conferences:

Lab-On-A-Chip Asia 2013, Singapore, **Nov. 2013**
- "An Intelligent Digital Microfluidics with Autonomous Positioning and Fuzzy-Enhanced Feedback Control"
- "Dried-down Reagents on a Microfluidic Chip for LATE-PCR Amplification and Detection of Single-stranded DNA"

IFEEC 2013, Tainan, Taiwan, **Nov. 2013**
- "Three-level hybrid active power filter with quasi-resonant dc-link technique in three-phase four-wire system"
- "Design of LCL filter for harmonic suppression in co-phase railway power quality conditioner"
- "Review of current quality compensators for high power unidirectional electric vehicle battery charger"

MWSCAS 2013, Columbus, Ohio, USA, **Aug. 2013**
- "A Background Gain-Calibration Technique for Low Voltage Pipelined ADCs Based on Nonlinear Interpolation"

ASQED 2013, Malaysia, **Aug. 2013**
- "A 2.93µW 8-Bit Capacitance-to-RF Converter for Movable Laboratory Mice Blood Pressure Monitoring"
- "A Wideband Multi-Stage Inverter-Based Driver Amplifier for IEEE 802.22 WRAN Transmitters"

ISNN 2013, Dalian, China, **Jul. 2013**
- "Canonical Correlation Analysis Neural Network for Steady-State Visual Evoked Potentials Based Brain-Computer Interfaces"

EMBC 2013, Osaka, Japan, **Jul. 2013**
- "Sub-threshold Standard Cell Library Design for Ultra-Low Power Biomedical Applications"
- "Canonical Correlation Analysis Neural Network for Steady-State Visual Evoked Potentials Based Brain-Computer Interfaces"
- "Bit Error Rate Estimation for Galvanic-Type Intra-Body Communication Using Experimental Eye-Diagram and Jitter Characteristics"

EDSSC 2013, Hong Kong, China, **Jun. 2013**
- "Optimization of Microwatt On-Chip Charge Pump for Single-Chip Solar Energy Harvesting"
- "An Ultra-Low Power CMOS Smart Temperature Sensor for Clinical Temperature Monitoring"
- "Standard Cell Library Design with Voltage Scaling and Transistor Sizing for Ultra-Low-Power Biomedical Applications"

ISCAS 2013, Beijing, China, **Apr. 2013**
- "A Continuous-Time VCO-Assisted Sigma Delta Modulator with 76.6dB SNDR and 10MHz BW"
- "A 0.6V 8B 100MS/s SAR ADC with Minimized DAC Capacitance and Switching Energy in 65nm CMOS"
- "A 0.5V 10GHz 8-Phase LC-VCO Combining Current-Reuse and Back-Gate-Coupling Techniques Consuming 2mW"
- "A 1.83µW, 0.78µVrms Input Referred Noise Neural Recording Front End"

APEC 2013, Long Beach, CA, USA, **Mar. 2013**
- "A hybrid railway power conditioner for traction power supply system"