澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

模拟与混合信号
超大规模集成电路
国家重点实验室
（澳门大学伙伴实验室）
State Key Laboratory of Analog and Mixed - Signal VLSI
(Partner Laboratory in University of Macau)
中华人民共和国科学技术部

State Key Laboratory of
Analog and Mixed-Signal VLSI

State Key Lab of Analog and Mixed-Signal VLSI (SKL AMS-VLSI) Newsletter

Motto: "Locally, from (World) Quality towards (National) Quantity"

座右銘:立足本土、人才培養，以世界級質量創建國家級規模

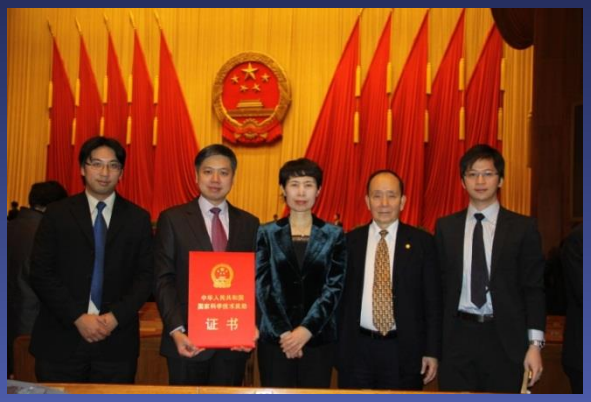
Year 2
No. 2

December 2012

2012 Milestones

Outstanding Recognition

Local (Macao), National (China) & International (USA)



2nd-Class State Scientific & Technological Progress Award "The Design & Development of High-Performance Analog & Mixed-Signal IC Technology" - China

[(left to right) Dr. Sai-Weng Sin, Prof. Seng-Pan U, Deputy Director of Liaison Office of China in Macao SAR Ms. Gao Yan, President of Administrative Committee FDCT Dr. Tong Chi Kin, & Prof. Pui-In Mak]

Macao Science & Technology Award, Technology Invention, 2nd-Prize, "Analog and Mixed- Signal Interface for a Ubiquitous Electronic World"

[(left to right) Prof. Pui-In Mak, Dr. Sai-Weng Sin, Ms. Gao Yan (Liaison Office of China in Macao SAR), Prof. Rui Martins, & Prof. Seng-Pan U, receive the award]

Recipients of the China S&T Progress Award (above), and Prof. Rui Martins, share research experience with Macao secondary school students

Macao Science & Technology Award – Special Award, "The Design & Development of High-Performance Analog & Mixed- Signal IC Technology"

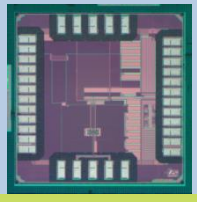
[Award Recipients with CE of Macao SAR Dr. Chui Sai On]

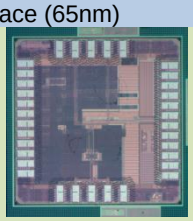
IEEE Macao SSCS (Solid-State Circuits Society) Chapter 2012 Best Chapter Award @ Diamond Jubilee (60 Years) of ISSCC, to be awarded in ISSCC 2013, February 18, San Francisco, USA

State-of-the-Art Chips - Designed and Tested in 2012 (10 chips)

Analog to Digital Converters (ADCs) chips

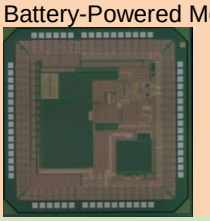
High Speed ADC for Optical Communication Interface (65nm)

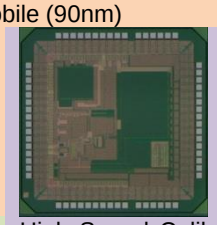




Compact and low power ADC in Ultra Wide Band portable system (65nm)

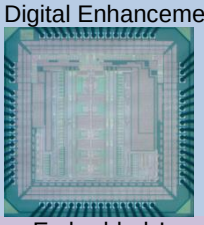
High Speed and Power Efficient ADC for Battery-Powered Mobile (90nm)





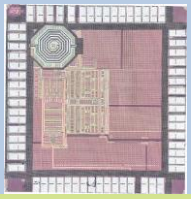
High Speed Calibration Embedded Low Power ADC for Mobile Communications (90nm)

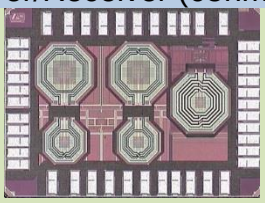
High Performance Pipelined ADC with Digital Enhancement Technique (90nm)



Wireless and Biomedical Engineering (BME) chips

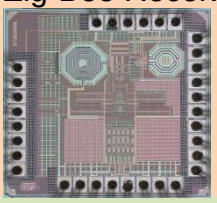
WIFI Transceiver/Receiver (65nm)

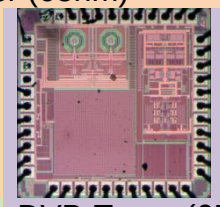




Quadrature VCO (65nm)

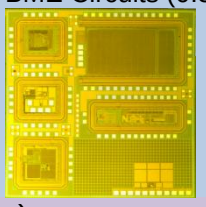
Zig-Bee Receiver (65nm)





DVB-Tuner (65nm)

Energy Harvesting Sensors & BME Circuits (0.35µm)



Important Events

PhD Oral Defense on Microelectronics
26-April 2012

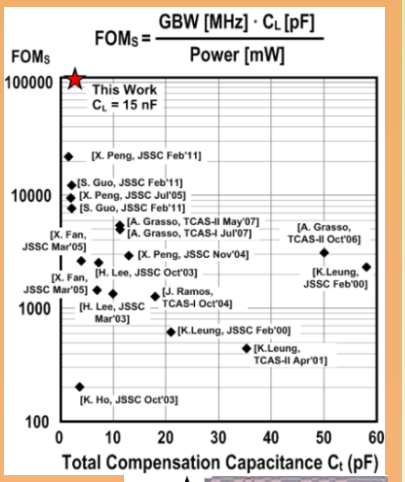
Title: Design Techniques for Low-Power High-Speed Analog-to-Digital Converters using Binary-Search and Subranging Schemes

Candidate: U-Fat Chio (Alpha)

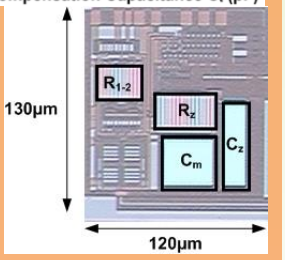
PhD Oral Defense – Candidate with Examiners (external from Tsinghua U., China & U. of Seville, Spain)

"Chip Olympics" – 59th International Solid-State Circuits Conference - ISSCC 2012

The 59th IEEE International Solid-State Circuits Conference – **ISSCC 2012** held between February 19 & 23, in San Francisco, USA, is the flagship conference of the Solid-State Circuits Society (SSCS), one of the largest of the 40 societies of IEEE (Institute of Electrical and Electronics Engineers), and at the forefront of the current Information Age Revolution.



Zushu Yan, Pui-In Mak, Man-Kay Law, R. Martins, "A 0.016mm^2 144µW three-stage amplifier capable of driving 1-to-15nF capacitive load with >0.95MHz GBW," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012, vol., no., pp.368-370, 19-23 Feb. 2012



News:

State Key Laboratory of Analog and Mixed-Signal VLSI is established as Independent Academic Unit in the University of Macau, November 2012.

US Patents granted in 2012/2013

1. **Pui-In Mak, Seng-Pan U, R.P.Martins,** "Switched Current-Resistor Programmable Gain Array for Low-Voltage Wireless LAN System and Method Using the Same," *US Patent,* Serial No. 12/355,649, **June 25, 2012**.
2. **Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins, Franco Maloberti,** "N-Bits Successive Approximation Register Analog-to-Digital Converting System," *US Patent Pending* - No. 13/150,508, **March 2013**.
3. **Sai-Weng Sin, He-Gong Wei, Li Ding, Yan Zhu, Chi-Hang Chan, U-Fat Chio, Seng-Pan U, R. P. Martins, Franco Maloberti,** "Analog to Digital Converter Circuit," *US Patent Pending* - No. 13/232,442, **March 2013**.

1st Academic Committee Meeting of the SKL of Analog and Mixed-Signal VLSI:

The 1st meeting & the one day evaluation of the current research at SKL was held on 23 March 2012 by the Academic Committee Members *(International Board of Advisors).* After the opening ceremony the Academic Committee was given an overall presentation of the research including laboratory demonstrations and there were discussions with representatives and students of the various research lines.

Academic Committee Members (present):

Prof. Franco Maloberti, Chair, University of Pavia, (Italy)
Prof. Hoi-Jun Yoo, Korea Advanced Institute of Science and Technology - KAIST (South Korea)
Prof. Jacob Baker, Boise State University (USA)
Prof. Hong Zhiliang, Fudan University (China)
Prof. Wang Zhihua, Tsinghua University (China)
Prof. Akira Matsuzawa, Tokyo Institute of Technology - TIT (Japan)
Dr. Chris Mangelsdorf, Analog Device (Japan)
Prof. Ming-Dou Ker, National Chiao-Tung University (Taiwan)
Prof. Bram Nauta, University of Twente (Netherlands)
Prof. Howard Luong, Hong Kong University of Science and Technology - HKUST (Hong Kong)

State Key Lab. of AMS-VLSI Science Series

2nd Distinguished Lectures
22 & 24 March 2012

The World of Analog Micro-Power, **Prof. Franco Maloberti**
Wearable Healthcare (Bio-Medical CMOS IC System Design), **Prof. Hoi-Jun Yoo**
Low Power, High-BW & Ultra-Small Memory Module Design, **Prof. Jacob Baker**
Low cost, high efficiency Power Management IC Design, **Prof. Hong Zhiliang**
Medical Electronics-the Next Big Engine for Semi. Industry, **Prof. Wang Zhihua**
Low Energy and Low Voltage ADC Design Strategy & Proposing an Interpolated Pipeline ADC, **Prof. Akira Matsuzawa**
What you Don't Know about Miller Compensation, **Dr. Chris Mangelsdorf**
New Design Considerations on ESD Clamp Circuit in Nanoscale CMOS Technology, **Prof. Ming-Dou Ker**

2012 GSA-UM SKL Semiconductor Insight Roundtable

21 June 2012

Dr. Jeremy Wang Asia-Pacific Executive Director, Global Semiconductor Association
Prof. Jason Cong, Director, Center for Customizable Domain-Specific Computing, University of California, Los Angela, USA
Prof. Tim Cheng, Director, Learning-Based Multimedia Group & SoC Design and Test group, University of California, Santa Barbara, USA
Prof. Xiaolang Yan, Director, Strategic Expert Committee for VLSI Design of China 863 Program, Zhejiang University, China
Prof. Xu Cheng, Director, Microprocessor Development & Research Center, Peking University, China

Others:

Visit by Dr. Cao Jianlin, Vice-Minister, Ministry of Science & Technology, Beijing, China, 25, September, 2012

Visit & Distinguished Lecture by Dr. Rakesh Kumar, President IEEE SSCS, and Prof. Boris Murmann, Stanford University, 21 and 22 November, 2012

Visit & Distinguished Lecture by Prof. Thanos Stouraitis, President IEEE CASS, 7, December, 2012

Two New Academics Joined SKL AMS-VLSI

We are most delighted with the recruitment of 2 new Assistant Professors to the SKL, original from Hong Kong and Macao SARs, which will further enhance SKL's competitiveness.

Dr. Man-Kay Law received the B.Sc. in Computer Engineering and the Ph.D. degree in Electronic and Computer Engineering from the Hong Kong University of Science and Technology (HKUST), in 2006 and 2011, respectively. He was in HKUST as a Visiting Assistant Professor from February 2011 to August 2011.
Research interests: CMOS Smart Temperature Sensors, CMOS Image Sensors, Integrated Wireless Sensing and Biomedical Systems, Ultra-low Power Analog Design Techniques, Energy Harvesting Techniques

Dr. Sio-Hang Pun received the BSc degree in Electrical and Electronics Engineering (EEE) from University of Macau, in 1997, the MSc degree in Computer and Electrical Engineering from the University of Porto, Portugal, in 1999, and the Ph.D. in EEE from U. of Macau, in 2011.
Research interests: Bioelectronic circuits, Bio-electromagnetism, Intra-Body Communications

Book

1. "**High-/Mixed-Voltage Analog and RF Circuit Techniques for Nanoscale CMOS**", Series of *Analog Circuits and Signal Processing (ACSP)*, **Springer Press**, ISBN 978-1-4419-9538-4, **April 2012**.

SCI Journals – 14 Papers (13 in 2012)

1. "An intelligent digital microfluidic system with fuzzy-enhanced feedback for multi-droplet manipulation", ***Lab on a Chip, Royal Society Chemistry Publishing***, **January 2013**.
2. "A 0.83-μW QRS Detection Processor Using Quadratic Spline Wavelet Transform for Wireless ECG Acquisition in 0.35-μm CMOS", ***IEEE Transactions on Biomedical Circuits and Systems***, **December 2012**.
3. "Low-Complexity, Full-Resolution, Mirror-Switching Digital Pre-Distortion Scheme for Polar-Modulated Power Amplifiers", ***IET Electronics Letters***, **November 2012**.
4. "A 8-bit 400MS/s 2-bit per cycle SAR ADC with Resistive DAC", ***IEEE Journal of Solid-State Circuits***, **November 2012**.
5. "A 50fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation", ***IEEE Journal of Solid-State Circuits***, **November 2012**.
6. "Enhanced RFICs in Nanoscale CMOS", ***IEEE Microwave Magazine***, **September/October 2012**.
7. "A Frequency-Translation Technique for Low-Noise Ultra-Low-Cutoff Lowpass Filtering", ***Analog Integrated Circuits and Signal Processing***, Springer, **July 2012**.
8. "Ultra-Area-Efficient Three-Stage Amplifier Using Current Buffer Miller Compensation and Parallel Compensation", ***IET Electronics Letters***, **May 2012**.
9. "A 0.07mm^2, 2mW, 75MHz-IF, 4th-Order BPF Using a Source-Follower-Based Resonator in 90nm CMOS", ***IET Electronics Letters***, **May 2012**.
10. "Creating Multi-Stage Amplifiers with a Wide Range of Output-Current Drivability and Capacitive-Load Drivability is still very Challenging - Interview," ***IET Electronics Letters***, **May 2012**.
11. "Double Recycling Technique for Folded-Cascode OTA", ***Analog Integrated Circuits and Signal Processing***, Springer, **April 2012**.

[with Department of ECE / FST_UM]

12. "Individual Alpha Neurofeedback Training Effect on Short Term Memory," ***Elsevier International Journal of Psychophysiology***, **October 2012**.
13. "Robust Deterministic Annealing Based EM Algorithm," ***IET Electronics Letters***, **March 2012**.
14. "Trial Pruning Based on Genetic Algorithm for Single-Trial EEG Classification," ***Elsevier Journal of Computers and Electrical Engineering***, **January 2012**.

IEEE Conferences – 22 Papers (20 in 2012)

Major solid-state circuits conferences *[Unique in the World]*:

ISSCC 2013 , San Francisco, CA, USA ,**February 2013**

1. "A 1.7mW 0.22mm^2 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65nm CMOS" **[Regular Paper]**
2. "An Extremely Power-and-Area-Efficient Three-Stage Amplifier for LCD Display Drivers" **[Ph.D. Student Research Preview]**

A-SSCC 2012, Kobe, Japan, **November 2012**

3. "A 22.4μW 80dB SNDR ΣΔ Modulator with Passive Analog Adder and SAR Quantizer for EMG Application"
4. "Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470MS/s Pipelined-SAR ADC"

ESSCIRC 2012, Bordeaux, France, **September 2012**

5. "A 0.024mm^2 4.9 fJ 10-Bit 2MS/s SAR ADC in 65 nm CMOS"
6. "A 12-Bit 110MS/S 4-Stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique"

CICC 2012, San Jose, CA, **United States, September 2012**

7. "A 2.3mW 10-bit 170MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC"

VLSI 2012, Honolulu, USA, **June 2012**

8. "A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC"
9. "A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure"

ISSCC 2012 , San Francisco, CA, USA , **February 2012**

10. "A 0.016mm^2 144μW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load with >0.95MHz GBW"

Other conferences:

APCCAS 2012, Kaohsiung, Taiwan, **December 2012**

11. "A Dynamic-Range-Improved 2.4GHz WLAN Class-E PA Combining PWPM and Cascode Modulation"
12. "A Robust NTF Zero Optimization Technique for Both Low and High OSRs Sigma-Delta Modulators"
13. "A DT 0-2 MASH Modulator with VCO-Based Quantizer for Enhanced Linearity"
14. "A 10-bit SAR ADC With Two Redundant Decisions and Splitted-MSB-Cap DAC Array"

BIOCAS 2012, Hsinchu,Taiwan, **November 2012**

15. "A 0.8-μW 8-Bit 1.5~20-pF-Input-Range Capacitance-to-Digital Converter for Lab-on-Chip Digital Microfluidics Systems"

MWSCAS 2012, Boise, Idaho, USA , **August 2012**

16. "An ELD Tracking Compensation Technique for Active-RC CT ΣΔ Modulators"

ASQED 2012, Penang, Malaysia , **July 2012**

17. "A low-cost capacitive relative humidity sensor for food moisture monitoring application"

ISCAS 2012, Seoul, Korea, **May 2012**

18. "A 0.02-to-6GHz SDR Balun-LNA Using a Triple-Stage Inverter-Based Amplifier"
19. "A 10MHz BW 78dB DR CT ΣΔ Modulator with Novel Switched High Linearity VCO-Based Quantizer"
20. "A sub-1V BJT-based CMOS temperature sensor from -55 °C to 125 °C"

ICBEB 2012, Macau, **May 2012**

21. "A Wearable Wireless General Purpose Bio-signal Acquisition Prototype System for Home Healthcare"

IFMA 2012, Hangchow, China, **April 2012**

22. "A Digital Microfluidic System with Low Voltage Threshold and Control Module for Droplet Manipulation"