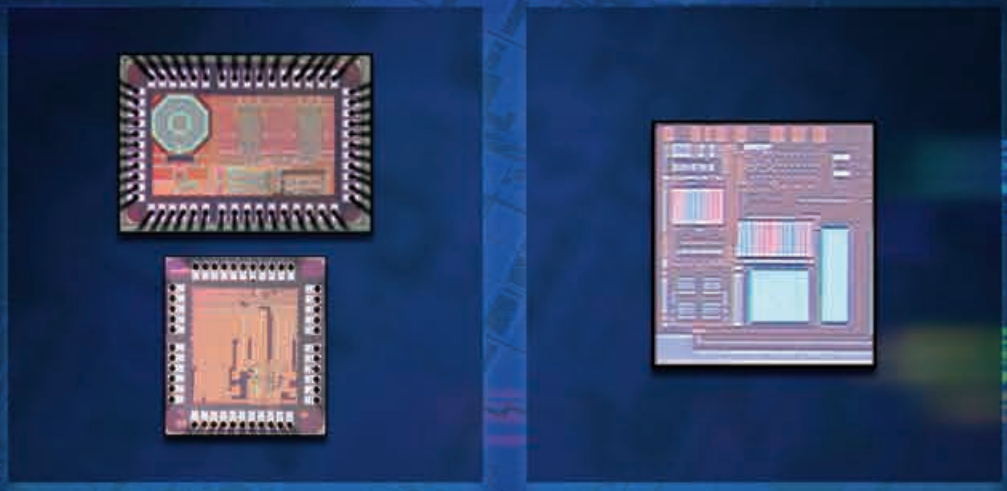
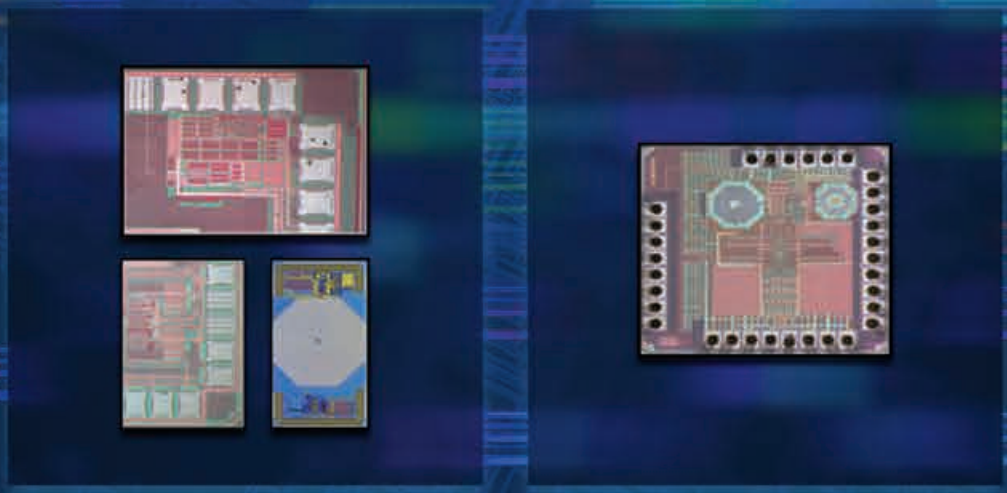
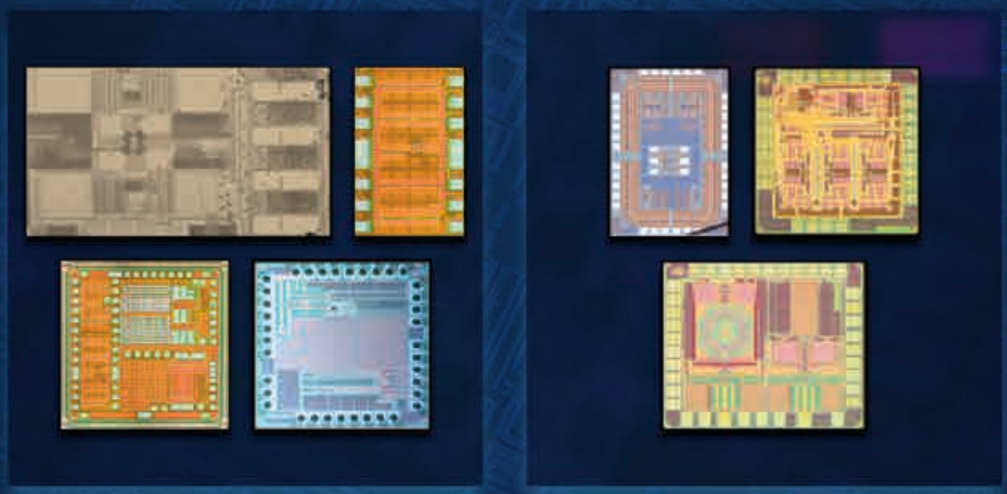


Research Report 2011-2016

State Key Laboratory of Analog and Mixed-Signal VLSI
University of Macau





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FOREWORD

It is with a great pleasure that I present to you the 2011-2016 Research Report of the State Key Laboratory of Analog and Mixed-Signal VLSI (SKL-AMSV). It features the results and achievements of the whole team of collaborators that include academics, staff, students, postdocs and visiting scholars associated with SKL-AMSV during the referred period.

The mission of the SKL-AMSV is to advance world-state-of-the-art research, education and innovation in Electronics by establishing an excellent R&D platform in the area of analog and mixed-signal integrated circuits and systems that should meet the State (China) and international standards. Following our Motto: ***Locally, from (World) Quality towards (National) Quantity***, we aimed at the importance of the close relationship between innovative IC research and the State's emerging growth of IT and technology development. Our original goals, in the initial period 2011-2013, were to setup the basic human and technical infrastructure to launch cutting-edge research projects important for the advance of various electronics systems in data conversion and signal processing, wireless communications, biomedical and integrated power electronics. Further, the original target of SKL-AMSV was to setup the State's most important silicon access center in advanced nanometer IC technologies, pointing at building-up a highly-qualified local technical (including software-design and hardware testing equipment platforms) and human infrastructure through training and cultivation at postgraduate level M.Sc. and Ph.D. candidates, as well as involving post-doctoral researchers in R&D projects with possible industrial applications, objectives that were clearly met.

In the second period from 2014-2016, we followed a consolidation and further integration of the research lines experiencing a fast and consistent growth placing SKL-AMSV at the frontier of state-of-the-art silicon chips in China, resulting into hundreds of papers in leading journals and conferences in the IEEE Solid-State Circuits Society (SSCS), Circuits and Systems Society, Microwave Theory and Techniques Society, plus the Royal Society of Chemistry, for the emerging area of Biochips. All of them are the topmost international societies that cover the field of integrated circuits and systems, and experimental results from real chips or microfluidic prototypes are essential for publication, thus ensuring its maturity and quality. Our most significant outcome has been the continuous contribution with 20 papers/chips to the IEEE International Solid State Circuits Conference (ISSCC) from 2011 to 2017, which is the flagship conference of the IEEE SSCS that serves as a premier forum, and the real world-benchmark conference, for presenting advances in solid-state circuits. Almost all chip-design breakthroughs from top companies like Intel, Analog Devices, Qualcomm, Broadcom, Texas Instruments, and top universities like MIT, Stanford, UCLA, UC Berkeley were firstly reported there for the first time.

Since its inception SKL-AMSV trained 6 Post-Doc Fellows, 18 Ph.Ds, 50+ M.Sc. and 60+ B.Sc students, published 7 Books, 130+ SCI Journal Papers, 180+ Conference Papers and holds now 25+ US Patents. Plus, 86 chips were designed, fabricated, and measured, with highly competitive state-of-the-art results, including the advanced 28nm CMOS process. Also, numerous awards were received locally (Macao), regionally (China) with the first S&T national award ever attributed to a local Macao research team, and internationally (USA). Furthermore, SKL-AMSV recruited 9 Assistant Professors, 2 UM Macao Fellows (with PhDs obtained @UM), 7 staff for administrative and technical support, including 1 for technology transfer. The development of SKL-AMSV will not only promise technological advances for Macao through state-of-the-art R&D, but also the devotion in the future to technology transfer in terms of application and commercialization of R&D results/Patents to industry. The developing of technical human resources and world-class innovative technologies will contemplate the forthcoming conversion into an Institute of Microelectronics - IME as well as the eventual emergence of spin-off companies to bring real industrial impact to cope with China's strategic development towards full-autonomy in IC design capability. In the future, we are confident that we can maintain our world-level state-of-the-art electronics status while expanding the commercialization activity. High-end measurement equipment and IT facilities were purchased to meet the needs of current and future developments, with the setup of a cleanroom to support R&D of Biochips and multidisciplinary research. On-going cooperation projects with advanced Chinese IC Design companies allows us to envisage the future with good perspectives following the trends defined in SKL-AMSV development plans.

Prof. Rui Martins
SKL-AMSV, Director
Macao, April 2017

RESEARCH ABSTRACTS
WIRELESS TRANSCEIVERS

A 0.46-mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS

Pui-In Mak and Rui P. Martins

06

FEATURES

Full-band mobile TV (170 to 1700 MHz)
Low power consumption, 43 to 55 mW
Gain-boosting current-balancing Balun-LNA
Direct-injection-locked 4-/8-phase LO generator
Current-reuse mixer-lowpass filter
Silicon verified in ST 65 nm CMOS

DESCRIPTION

It is a unified receiver front-end (RFE) for full-band mobile TV covering the VHF-III (174 to 248 MHz), UHF (470 to 862 MHz) and L (1.4 to 1.7 GHz) bands, where standards like T-DMB, ISDB-T, DVB-H and DMB-T are resided. The performance, power and area efficiencies are advanced in threefold: 1) a gain-boosting current-balancing balun-LNA exhibits high linearity, wideband output balancing and adequate against gain control; 2) a current-reuse mixer-low-pass-filter merges quadrature-/harmonic-rejection mixing and 3rd-order current-mode post-filtering in one block, enhancing linearity and noise just where both are demanding, while saving power and area for its simplicity; 3) a direct injection-locked 4-/8-phase local oscillator (LO) generator relaxes the master LO frequency by avoiding frequency division.

Fabricated in 65-nm CMOS, the RFE measures 4-dB noise figure, 17-to-35-dB gain range, and 32/3.4-dBm IIP2/IIP3 with no tuning. The power consumption ranges from 43 mW (170 MHz) to 55 mW (1.7 GHz). The active area is 0.46 mm2 excluding the VCO. Dual 1.2/2.5-V supplies allow more functions to be realized in the current domain. Device reliability is ensured via a hybrid use of thin-oxide and thick-oxide MOSFETs and voltage-conscious biasing.

Benchmarking with the prior art, this work succeeds in extending the operating bandwidth and baseband selectivity with comparable power, while reducing the external parts, chip area and frequency of the LO that can ease the design of the PLL and VCO.

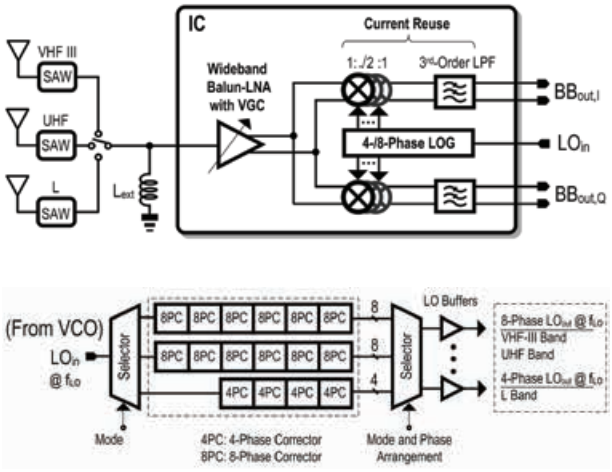

Fig. 1. (a) Receiver front-end (RFE) architecture and (b) detail of the LO generator.

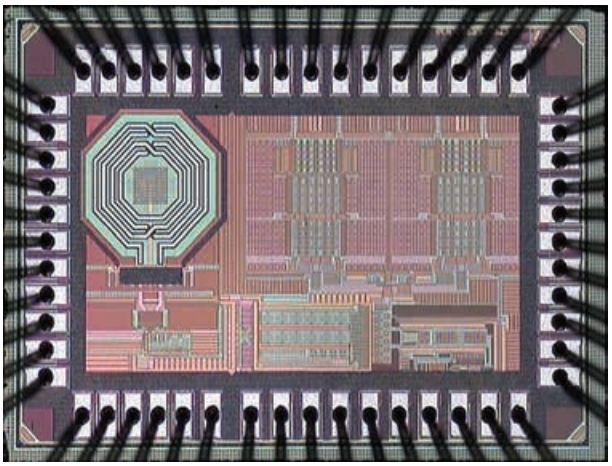

Fig. 2. Chip micrograph.

Publication(s):

[1] P.-I. Mak and R. P. Martins, "A 0.46-mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS," IEEE Journal of Solid-State Circuits, pp. 1970-1984, vol. 46, Sept. 2011.

[2] P.-I. Mak and R. P. Martins, "A 0.46mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), pp. 172-173, Feb. 2011.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 53-to-75-mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS

Ka-Fai Un, Pui-In Mak, and Rui P. Martins

FEATURES

Two-stage 6-/14-path harmonic-rejection mixers
Low power consumption, 53 to 75 mW
Large bandwidth, 54 to 862 MHz
High harmonic rejection ratio, 59.3 dB
Low LO reference frequency, 432 to 864 MHz
Silicon verified in ST 65nm bulk CMOS

DESCRIPTION

A TV-band white-space transmitter covering a 16x-wide spectrum from 54 to 864 MHz is described.

It features a systematic co-design between the architecture and circuits to address the harmonic-mixing problem.

It incorporates two-stage 6-/14-path harmonic-rejection mixers and low-Q passive-RC/-CLC filters to manage the unwanted harmonic emission fully on chip.

It achieves an uncalibrated harmonic rejection ratio (HRR) of minimally 59.3 dB (16 samples) for all in-/out-band harmonics.

The employed 8-/16-phase LO generator is based on injection-locked 4-/8-phase correctors and even-ratio-only frequency dividers to save the LO-path power (2.5 to 14.2 mW) while lowering the required reference LO frequency (432 to 864 MHz).

Without any pre-distortion, the EVM tested under a 64-QAM OFDM digital-TV signal is 2.9% at 96 MHz, 3.3% at 384 MHz, and 4.0% at 600 MHz.

The first (second) adjacent channel leakage ratio is -46 dBc (-43 dBc) at 6 MHz (12 MHz) offset.

The power consumption is 53.1 to 75.2 mW and active area is 0.93 mm in 65-nm CMOS.

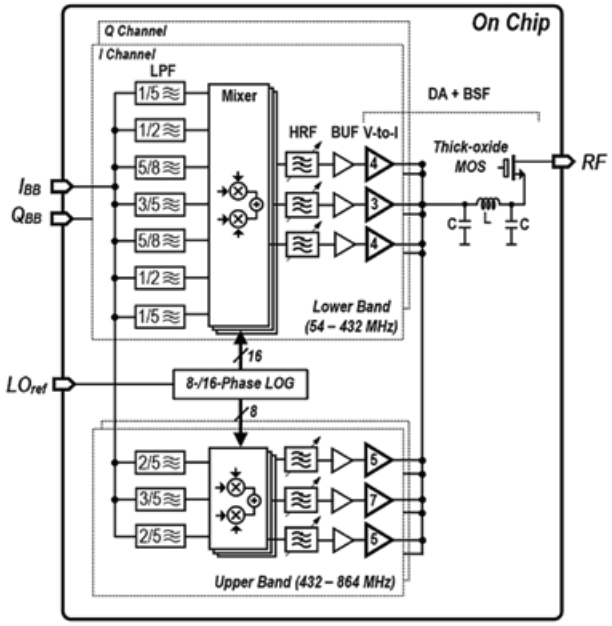

Fig. 1. Proposed TX with two-stage 6-/14-path harmonic rejection mixer.

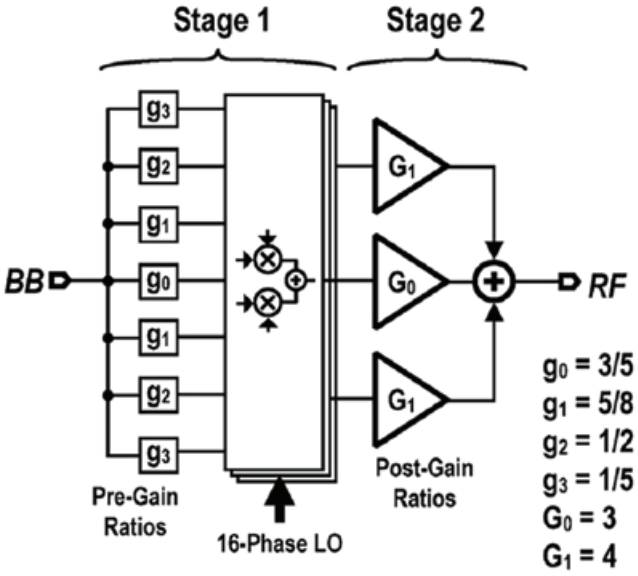

Fig. 2. Single-ended diagram two-stage 14P-HRM.

Publication(s):

[1] K.-F. Un, P.-I. Mak, and R. P. Martins, "A 53-to75-mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS," IEEE J. Solid-State Circ., vol. 48, no. 9, pp. 2078-2089, Sep. 2013.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Nonrecursive Digital Calibration Technique for Joint Elimination of Transceiver I/Q Imbalances With Minimized Add-On Hardware

Wei-Han Yu, Chak-Fong Cheang, Pui-In Mak, Weng-Fai Cheng, Ka-Fai Un, U-Wai Lok, and Rui P. Martins

FEATURES

A non-recursive local oscillator switching technique
Coordinate rotation digital computer algorithm
Improved TX's image rejection, from 27.8 to 37.2 dB
Improved RX's image rejection, from 31.2 to 42.0 dB
Algorithm verified on an FPGA

DESCRIPTION

A non-recursive digital calibration technique, namely, local oscillator (LO) switching, is proposed for jointly eliminating transmitter (TX) and receiver (RX) I/Q imbalances in one combined process.

The add-on analog parts are limited to a set of source followers (0.00228 mm^2) and metal–oxide–semiconductor (MOS) switches (0.00017 mm^2) for reusing the 90◦ phase shift property of the reference LO, avoiding the sinusoidal test tone, loop-back detector, high-speed analog-to-digital converter, and 2-D iterative search algorithm, mostly required in the prior art.

A 65-nm complementary MOS transceiver, which is co-designed with a field-programmable-gate-array-based coordinate rotation digital computer algorithm, measures a 10-dB improvement in the image rejection ratio of both the TX (27.8 → 37.2 dB) and the RX (31.2 → 42 dB).

The required digital circuitry for the algorithm is also assessed and simulated.

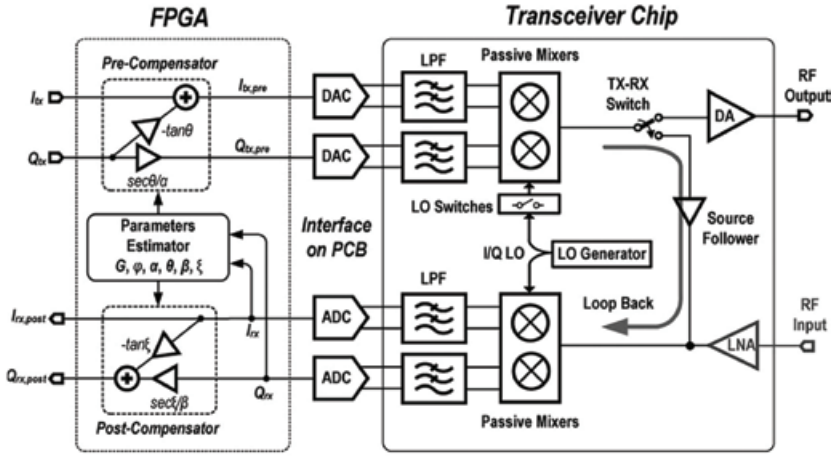

Fig. 1. CMOS TRX chip co-designed with an FPGA implementing the proposed calibration algorithm.

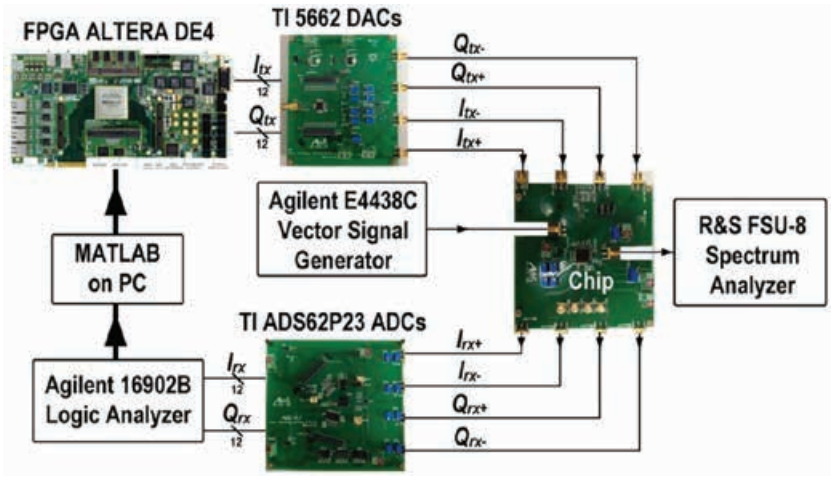

Fig. 2. Measurement setup.

Publication(s):

[1] W.-H. Yu, C.-F. Cheang, P.-I. Mak, W.-F. Cheng, K.-F. Un, U-W. Lok, and R. P. Martins, "A Nonrecursive Digital Calibration Technique for Joint Elimination of Transmitter and Receiver I/Q Imbalances with Minimized Add-On Hardware," IEEE Trans. Circuits Syst. II, Express Briefs, vol. 60, no. 8, pp. 462-466, Aug. 2013.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 2.4-GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65-nm CMOS

Zhicheng Lin, Pui-In Mak, and Rui P. Martins

FEATURES

On-chip input matching network + balun-LNA
Low power consumption, 1.7 mW
Wide S_{11} matching bandwidth, >1 GHz
Compact chip area, 0.24 mm^2
Silicon verified in ST 65 nm CMOS

DESCRIPTION

Ultra-low-power radios have essentially underpinned the development of short-range wireless technologies such as personal/body-area networks and Internet of Things. The main challenges faced by them are the stringent power and area budgets, and the pressure of minimum external components to save cost and system volume.

Ultra-low-voltage ultra-low-power radios are the most widespread design trend for ZigBee, Bluetooth and energy-harvesting applications. Yet, the lack of voltage head-room will limit the signal swing and transistor's f_T, imposing the need of bulky inductors/ transformers to facilitate the biasing and tune out the parasitics. Thus, the die area is easily penalized.

This work is a 2.4-GHz ZigBee receiver, unifying a balun-LNA-I/Q-mixer (Blixer) and a baseband (BB) hybrid filter in one cell, is fabricated in 65-nm CMOS. Without any external components, wideband input matching and passive pre-gain are concurrently achieved via co-optimizing an integrated low-Q network with a balun-LNA. The latter also features active-gain boosting and partial-noise canceling to enhance the gain and noise figure (NF). Above the balun-LNA are I/Q double-balanced mixers driven by a 4-phase 25% LO for downconversion and gain-phase balancing. The generated BB currents are immediately filtered by an IF-noise-shaping current-mode Biquad and a complex-pole load, offering 1st-order image rejection and 3rd-order channel selection directly atop the Blixer. Together with other BB and LO circuitries, the receiver measures 8.5-dB NF, 57-dB gain and –6-dBm $IIP3_{out\text{-}band}$ at 1.7-mW power and 0.24-mm^2 die size. The S_{11}-bandwidth (<–10 dB) covers 2.25 to 3.55 GHz being robust to packaging variations. Most performance metrics compare favorably with the state-of-the-art.

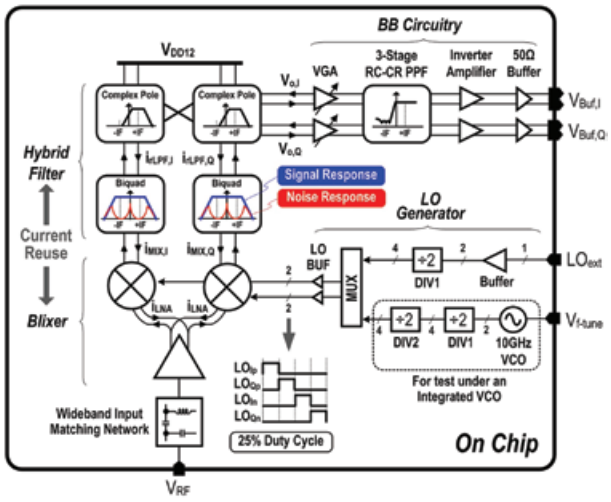

Fig. 1. Proposed 2.4-GHz RF-to-BB-current-reuse ultra-low-power receiver.

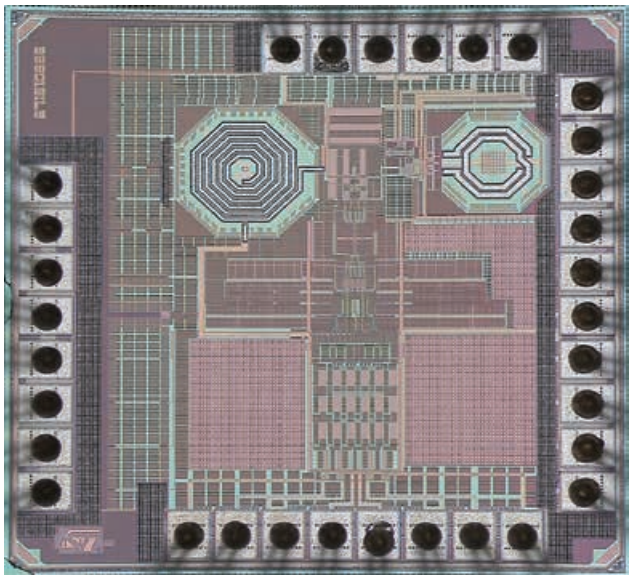

Fig. 2. Chip micrograph.

Publication(s):

[1] Z. Lin, P.-I. Mak and R. P. Martins, "A 2.4-GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65-nm CMOS," IEEE Journal of Solid-State Circuits, vol. 49, pp. 1333-1344, Jun. 2014.

[2] Z. Lin, P.-I. Mak and R. P. Martins, "A 1.7mW 0.22mm^2 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), pp. 448-449, Feb. 2013.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/ Passive Mixers and a Single-MOS Pole-Zero LPF

Fujian Lin, Pui-In Mak, and Rui P. Martins

FEATURES

Clock-rate-defined on-chip N-path bandpass filtering
Low power consumption, 16.2 mW at 0.85 GHz
High out-of-band linearity, IIP2=61 dBm, IIP3=17.4 dBm
Compact chip area, 0.55 mm^2
Silicon verified in ST 65 nm CMOS

DESCRIPTION

Frequency-flexible radios are low-cost platforms for multi-band multi-standard wireless communications. To minimize the number of SAW filters, wideband receivers mostly favor the N-path passive mixer for down-conversion, due to its high linearity and bidirec-tional response-translational property. Depending on the first baseband (BB) node of the receiver that can be a virtual ground or a lowpass-RC, the N-path passive mixer can be classified into current or voltage mode, respectively. For the former, the BB virtual ground is frequency-translated to RF, absorbing both the in-band signal and out-of-band interferers. As such, the signal amplification and channel selection can be delayed to BB. For the latter, the lowpass-RC at BB is shifted to RF, offering a tunable bandpass response to suppress the out-of-band interferers.

This work is an extensively-current-reuse wideband receiver exploiting parallel N-path active/passive mixers. The key features are: 1) a stacked RF-to-BB front-end with an 8-path active mixer realizing RF amplification, harmonic-recombination (HR) down-conversion and BB filtering in the current domain for better linearity and power efficiency; 2) a feedforward 8-path passive mixer enabling LO-defined input S_{11} matching without external components, while offering frequency-translated bandpass filtering and noise cancelling; 3) a single-MOS pole-zero lowpass filter (LPF) permitting both RF and BB filtering at low voltage headroom, while easing the tradeoff between the in-/out-of-band linearity, and 4) a BB-only two-stage HR amplifier boosting the harmonic rejection ratios ($HRR_{3,5}$). Measurements over 0.15 to 0.85 GHz manifest favorable NF (4.6 ± 0.9 dB) and out-of-band IIP2/IIP3 (+61/+17.4 dBm) at small power (10.6 to 16.2 mW) and area (0.55 mm^2). The HRR_{2-6} are >51 dB without any calibration or tuning. The out-of-band P_{-1dB} is >+2.5 dBm. The BB stopband rejection is >86 dB at 150-MHz offset.

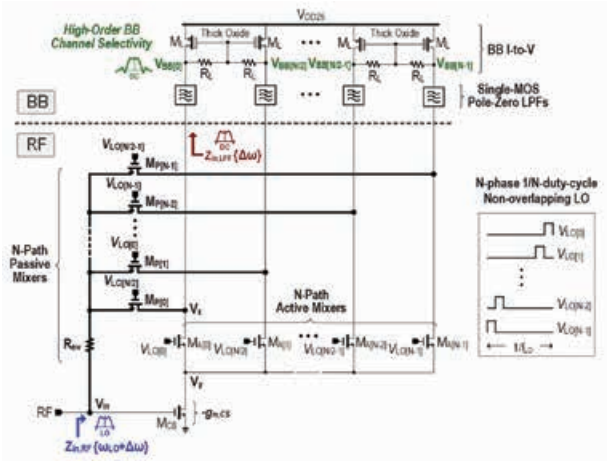

Fig. 1. Proposed RF-to-BB-current-reuse wideband receiver with the N-path filtering technique.

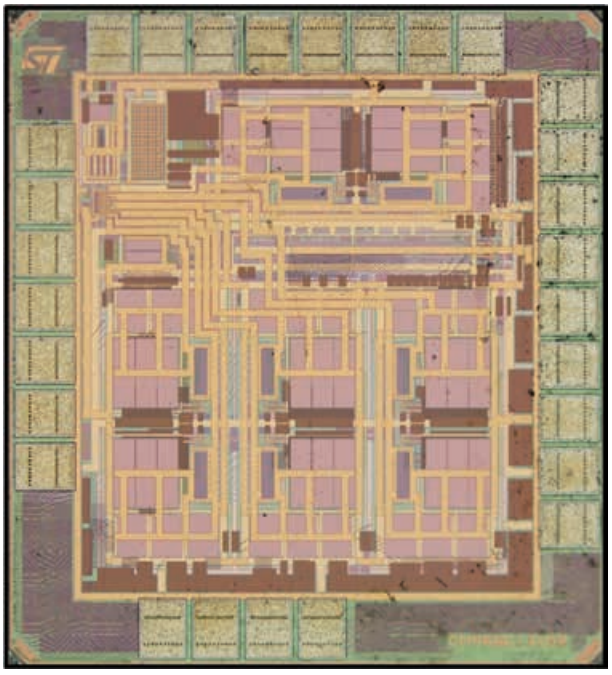

Fig. 2. Chip micrograph.

Publication(s):

[1] F. Lin, P.-I. Mak and R. P. Martins, "An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/ Passive Mixers and a Single-MOS Pole-Zero LPF," IEEE Journal of Solid-State Circuits, vol. 49, pp. 2547-2559, Nov. 2014.

[2] F. Lin, P.-I. Mak and R. P. Martins, "An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF," IEEE International Solid-State Circuits Conference (ISSCC), pp. 74-75, Feb. 2014.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications

Zhicheng Lin, Pui-In Mak, and Rui P. Martins

FEATURES

On-chip area-efficient N-path bandpass filtering
Ultra-Low power consumption, 1.15 mW
Multiple ISM bands (433/860/915/960 MHz)
Compact chip area, 0.2 mm^2
Silicon verified in ST 65 nm CMOS

DESCRIPTION

With the concept of Internet of Things (IoT), sub-GHz ULP wireless nodes compliant with the existing wireless standard such as the IEEE 802.15.4c/d (ZigBee) will be of great demand, especially for those that can cover all regional ISM bands [e.g., China (433 MHz), Europe (860 MHz), North America (915 MHz) and Japan (960 MHz)]. Together with the obvious goals of small chip area, minimum external components and ultra-low-voltage (ULV) supply (for possible energy harvesting), the design of such a receiver is quite challenging.

This work is a sub-GHz multi-ISM-band (433/860/915/960 MHz) ZigBee receiver. It features a gain-boosted N-path switched-capacitor (SC) network embedded into a function-reuse RF front-end, offering concurrent RF (common-mode) and BB (differential-mode) amplification, LO-defined RF filtering, and input impedance matching with zero external components. Interestingly, not only the BB power and area are nullified, but also the loading effect between the RF and BB blocks is averted, resulting in better noise figure (NF). Unlike the existing N-path filtering, the described gain-boosted topology offers: 1) double RF filtering at both input and output of the RF front-end; 2) size reduction of the physical capacitors thanks to the Miller multi-plication effect, and 3) LO-power saving by decoupling the mixer's on-resistance to the ultimate stopband rejection. Together with a low-voltage LC-VCO with extensively-distributed negative-gain cells for current-reuse with the BB filters, the receiver achieves 8.1 ± 0.6 dB NF, 50 ± 2 dB gain and –20.5 ± 1.5 dBm out-of-band IIP3 at 1.15 ± 0.05 mW power at 0.5 V over the four ISM bands.

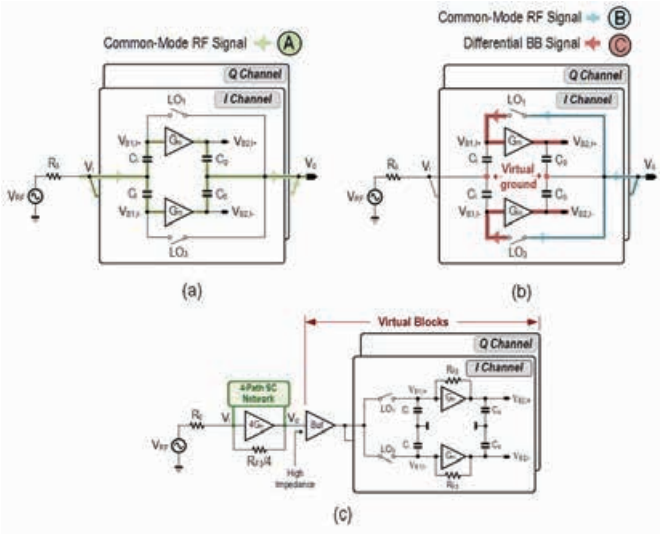

Fig. 1a-c Key idea of the proposed sub-GHz multi-ISM-band ZigBee receiver gain-boosted N-path filtering.

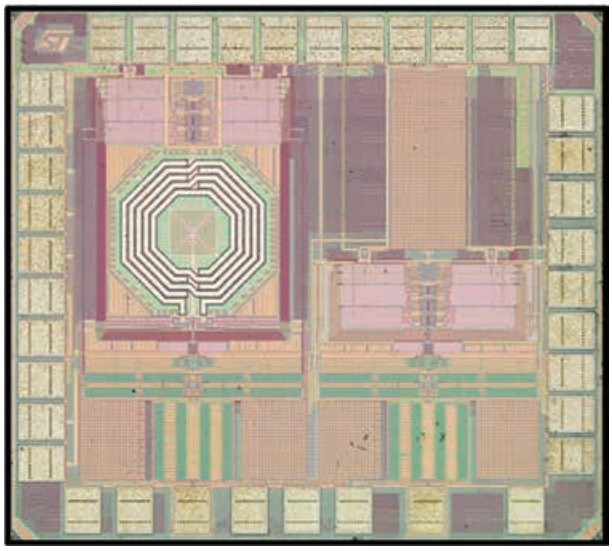

Fig. 2. Chip micrograph.

Publication(s):

[1] Z. Lin, P.-I. Mak and R. P. Martins, "A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications," IEEE Journal of Solid-State Circuits, vol. 49, pp. 2990-3004, Dec. 2014.

[2] Z. Lin, P.-I. Mak and R. P. Martins, "A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components," IEEE International Solid-State Circuits Conference (ISSCC), pp. 164-165, Feb. 2014.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.02-mm² 59.2-dB SFDR 4th-Order SC LPF with 0.5-to-10 MHz Bandwidth Scalability Exploiting a Recycling SC-Buffer Biquad

Yaohua Zhao, Pui-In Mak, Rui P. Martins, and Franco Maloberti

FEATURES

High in-band IIP3, +17.6 dBm
High SFDR, 59.2 dB
Ultra-compact chip area, 0.02 mm²
Silicon verified in ST 65 nm CMOS

DESCRIPTION

In response to the ever-increasing demand for higher data rates, Long-Term Evolution (LTE) and Wireless Local-Area Network (WLAN) radios have introduced the carrier aggregation (CA) and multiple-input multiple-output (MIMO) techniques to enhance their throughput. The numerous channel-selection low-pass filters (LPFs) will occupy a significant chip area. For common LPF topologies like active-RC and gm-C that hinge on passives to define the time constant, the area can be relatively large because of bandwidth (BW) tuning and kT/C requirement. Also, to resist the process variations and allow BW scaling, spare capacitor banks are unavoidable. Although the recent ring-oscillator-based LPF has improved area and power efficiencies, the BW could only be tuned by the supply voltage. This undertaking couples the BW scalability with other performance metrics, while entailing a precision voltage regulator to avoid drifting of BW against PVT.

This work is a switched-capacitor (SC)-buffer Biquad that can be recycled efficiently as an ultra-compact LPF. It incorporates only passive-SC networks and open-loop unity-gain buffers; both are friendlier to technology downscaling than most conventional Biquads that use high-gain amplifiers and closed-loop negative feedback. Complex-pole pairs with independent Q factors are recursively realized in one clock period, while ensuring low crosstalk effect between the formations of each pole. Nonlinearity and parasitic effects are inherently low due to no internal gain.

The fabricated 65-nm CMOS 1x-recycling SC-buffer Biquad is equivalent to a 4th-order Butterworth LPF with 75% buffer utilization. It occupies a die size of only 0.02 mm² and exhibits 20x BW tunability (0.5 to 10 MHz), linear with the clock rate. At 10-MHz bandwidth, the in-band IIP3 is +17.6 dBm and input-referred noise is 19.5 nV/√Hz; they correspond to 59.2-dB SFDR and 0.013-fJ FoM that is favorably comparable with the recent art. The P_{1dB} conforms to the out-of-band blocker profile of the LTE standard at a 20-dB front-end gain.

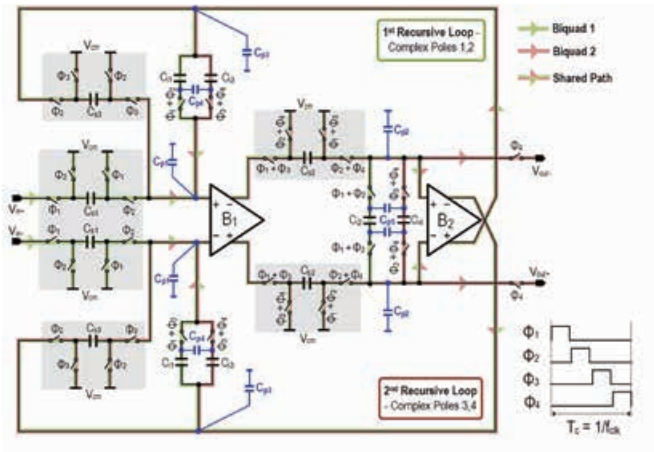

Fig. 1. 1x-recycling SC-buffer Biquad that is equivalent to a 4th-order Butterworth LPF.

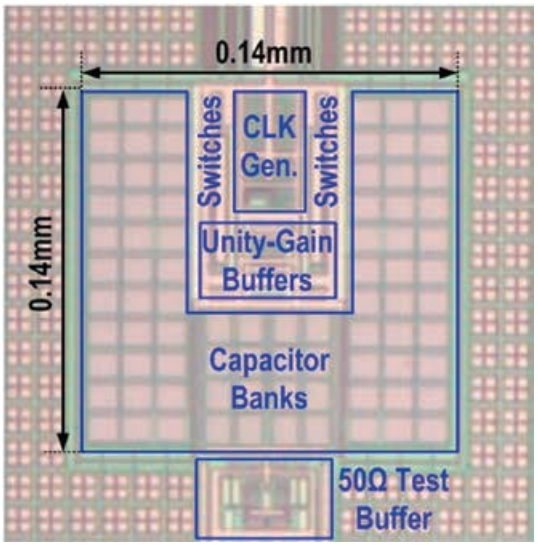

Fig. 2. Chip micrograph.

Publication(s):

[1] Y. Zhao, P.-I. Mak and R. P. Martins, and F. Maloberti, "A 0.02-mm² 59.2-dB SFDR 4th-Order SC LPF with 0.5-to-10 MHz Bandwidth Scalability Exploiting a Recycling SC-Buffer Biquad," IEEE Journal of Solid-State Circuits, vol. 50, pp. 1988-2001, Sep. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S_{11} Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF

Zhicheng Lin, Pui-In Mak, and Rui P. Martins

FEATURES

Low 0 dBm-blocker Noise Figure, 13.5 dB
Low power consumption, 11 mW
Wide RF coverage (0.1 to 1.5 GHz)
Ultra-compact chip area, 0.028 mm²
Silicon verified in ST 65 nm CMOS

DESCRIPTION

An RF-tunable blocker-tolerant receiver (RX) is desired to enhance the flexibility of multi-band multi-standard radios at low cost. The mixer-first RX delays the signal amplification to baseband (BB) by frequency-translating the BB lowpass response to RF as bandpass. This aim raises the out-of-band (OB) IIP3 at the expense of NF and power due to no RF gain. The noise-cancellation RX breaks such a tradeoff via paralleling a voltage-sensing RX with the mixer-first. This undertaking confers a better pair of NF and OB-IIP3, but sacrificing more die size and power to accommodate the doubled RF and BB circuitries. Although there is N-path RF filtering that can be combined with noise cancellation to save the die area and power consumption while offering a high OB-IIP3, a high supply voltage is required to widen the voltage headroom.

This work is a single-mixing blocker-tolerant RX using a gain-boosted-mixer-first topology. Two unexplored features: indirect BB amplification and double-RF N-path filtering improve the NF (1.5 to 2.9 dB) and OB-IIP3 (13 dBm) over a wide range of RF (0.1 to 1.5 GHz), while squeezing the power (11 mW) and area (0.028 mm²) with zero external components. The RX also originates partial-inductive input impedance to self-cancel the frequency shift of S_{11} bandwidth, which is a typical inadequacy of mixer-first RX demanding input-impedance tuning.

Thanks to the double-RF N-path filtering with narrow –3-dB bandwidth, the OB-IIP3 rapidly reaches 10 dBm at 30 MHz offset. The RF-to-IF gain is 38 dB, and drops by 1 dB with a –6 dBm blocker power at 80MHz offset, consistent with the 5.8 dB BB gain measured at that frequency offset. With a 0 dBm blocker, the 10 dB gain compression is due to the saturation of the BB amplifiers. The –3-dB BW at BB is ~2 MHz. With a single-tone blocker injected at 80MHz offset, the 0 dBm-blocker NF is 13.5 dB. Benchmarking with the recent art, this work succeeds in squeezing the power and area without penalizing the NF and OB-IIP3.

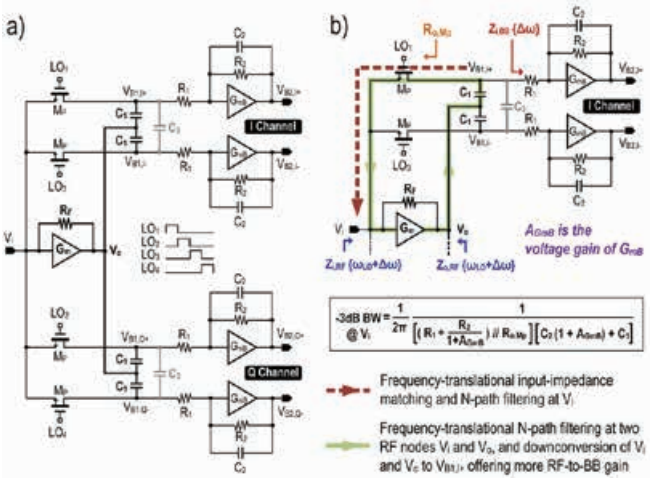

Fig. 1. Key idea of the proposed single-mixing blocker-tolerant receiver.

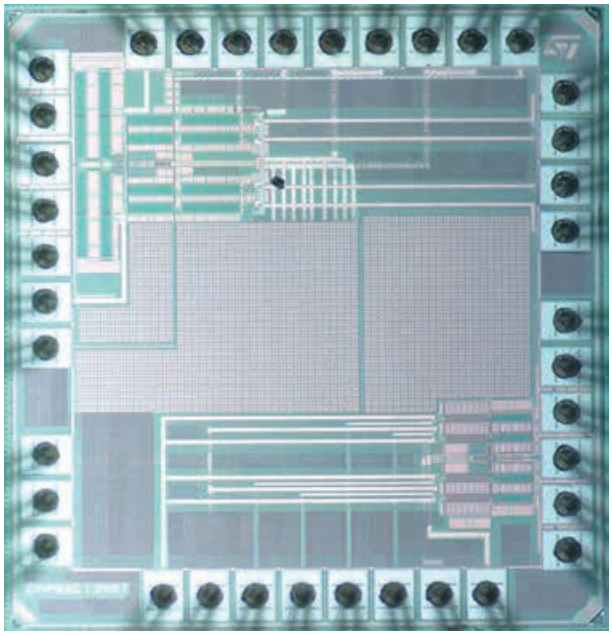

Fig. 2. Chip micrograph.

Publication(s):

[1] Z. Lin, P.-I. Mak and R. P. Martins, "A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S11 Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF," IEEE International Solid-State Circuits Conference (ISSCC), pp. 36-37, Feb. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.07 mm² 2.2 mW 10 GHz Current-Reuse Class-B/C Hybrid VCO Achieving 196-dBc/Hz FoM_A

Md. Tawfiq Amin, Jun Yin, Pui-In Mak, and Rui P. Martins

FEATURES

Low power, 2.2mW
Small area, 0.77 mm²

DESCRIPTION

This work is a current-reuse class-B/C hybrid voltage-controlled oscillator (VCO) with robust startup, enhanced phase noise and differential balancing at small area and power. Specifically, an asymmetrical CMOS class-C core is aided by a symmetrical NMOS-only class-B core that effectively shares the bias current for deeper class-C operation of the former; wider margin of startup against PVT variations, and lower amplitude imbalance against oscillation frequencies. Moreover, this topology adds the freedom of adjustable peak dynamic current and boosts the oscillation swing at low power. The spiral inductors with patterned ground shields shrink the die size. Fabricated in 65 nm CMOS, the 0.07 mm² VCO prototype exhibits 10.15-to-11.17 GHz tunability, and -107.7dBc/Hz phase noise at 1 MHz offset, while dissipating merely 2.2 mW at 1.2 V. The achieved area-included figure-of-merit (FoM_A = 196 dBc/Hz) favorably compares with the state-of-the-art.

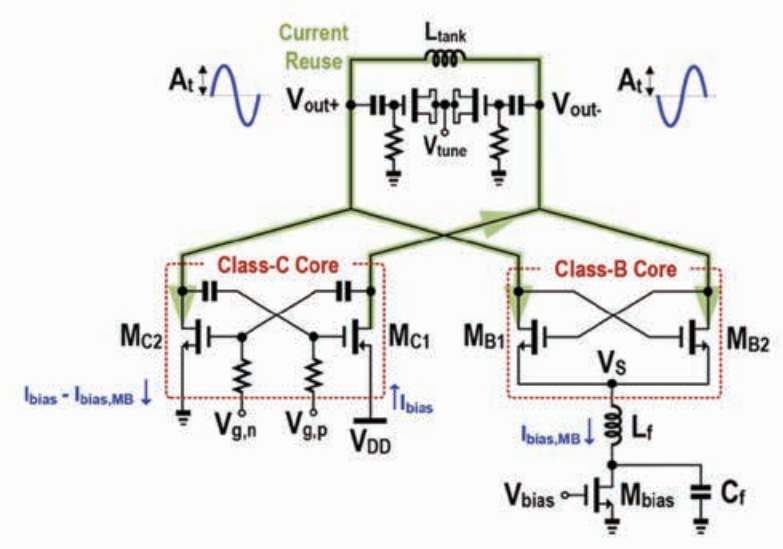

Fig. 1. Schematic of the proposed current-reuse class-B/C hybrid VCO.

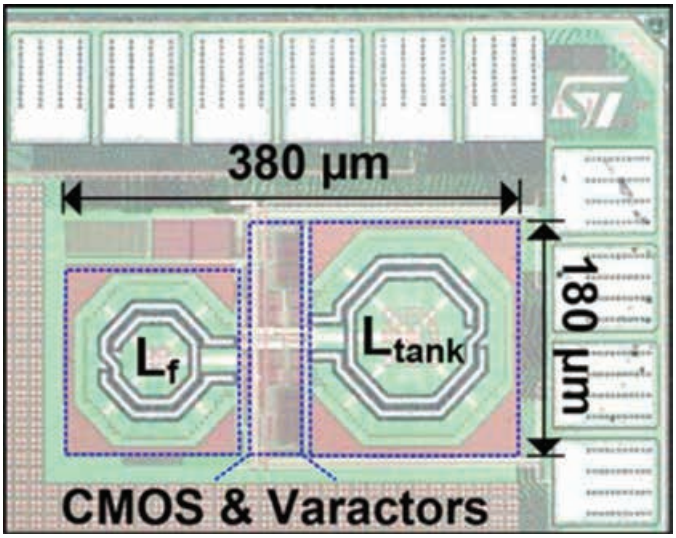

Fig. 2. Chip photo of the proposed VCO fabricated in 65 nm CMOS.

Publication(s):

[1] M. T. Amin, J. Yin, P.-I. Mak, and R. P. Martins, "A 0.07 mm² 2.2 mW 10 GHz Current-Reuse Class-B/C Hybrid VCO Achieving 196-dBc/Hz FoM_A," IEEE Microwave and Wireless Components Letters (MWCL), vol. 25, no. 7, pp. 457-459, Jul. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Sub-GHz Wireless Transmitter Utilizing a Multi-Class-Linearized PA and Wideband-Auto I/Q-LOFT Calibration for IEEE 802.11af WLAN

Ka-Fai Un, Wei-Han Yu, Chak-Fong Cheang, Gengzhen Qi, Pui-In Mak, Rui P. Martins

FEATURES

Multi-class-linearized PA
Time-domain auto I/Q-LOFT calibration
Large bandwidth, 54 to 600 MHz
High harmonic rejection ratio, 59.8 dB
High system efficiency, 7.4 to 18.5%
Low harmonics, -41 dBc
Silicon verified in ST 65nm bulk CMOS

DESCRIPTION

This work describes a sub-GHz wireless transmitter (TX) with an integrated multi-class-linearized power amplifier (PA) compliant with the IEEE 802.11af wireless local-area network.

It features a wideband in-phase/quadrature (I/Q) modulator exploiting two-stage 6-/14-path harmonic-rejection mixers plus G_m-C low-pass filters to manage the spurs emission induced by hard-switched mixing.

The entailed 8/16-phase local oscillator (LO) is generated by injection-locked phase correctors plus frequency dividers to relax the frequency and tuning range of the reference LO.

The linearized PA features overdriven-class-A/B/C cells to balance the power efficiency and linearity.

A dual-gate input pair enlarges the linear gain range.

A wideband low-impedance ground at the second harmonic suppresses the harmonic distortion and ground bounces.

The wideband I/Q imbalance and LO feedthrough are resolved by automatic digital calibration, which incorporates time-domain parameter estimation for better computational efficiency.

Benchmarking with the recent art, this solution fabricated in 65-nm CMOS exhibits higher system power efficiency (from 7.4% to 18.5%) and 1-dB compression point (from 12.5 to 16.3 dBm).

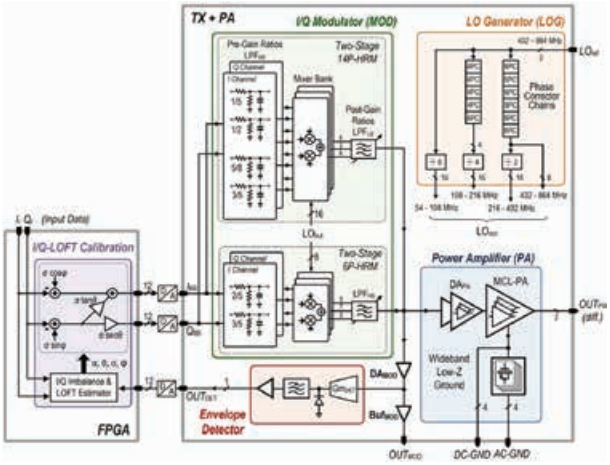

Fig. 1. Proposed wideband TX+PA with automatic I/Q-LOFT calibration in a closed-loop form.

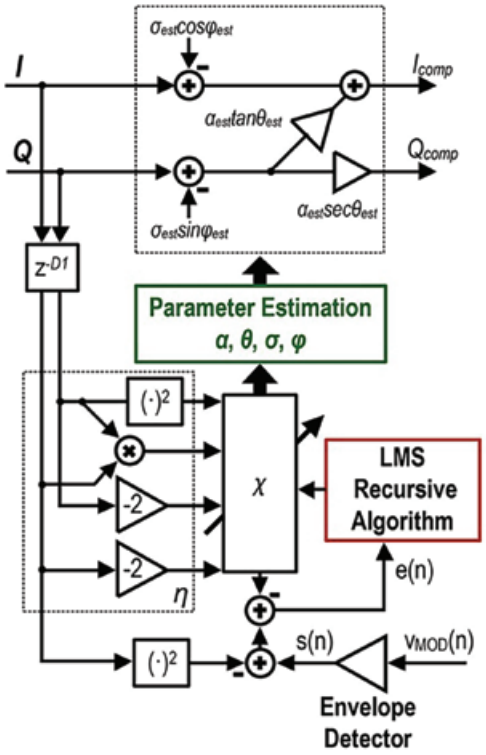

Fig. 2. Block diagram of the digital I/Q-LOFT calibration.

Publication(s):

[1] K.-F. Un, W.-H. Yu, C.-F. Cheang, G.Qi, P.-I. Mak, and R.P. Martins, "A Sub-GHz Wireless Transmitter Utilizing a Multi-Class-Linearized PA and Time-Domain Wideband-Auto I/Q-LOFT Calibration for IEEE 802.11af WLAN," IEEE Trans. Microw. Theory Techn., vol. 63, no. 10, pp. 3228-3241, Oct. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Combinatorial Impairment-Compensation Digital Predistorter for a IEEE 802.11af-WLAN CMOS Transmitter Covering a 10x-Wide Bandwidth

Chak-Fong Cheang, Ka-Fai Un, Wei-Han Yu, Pui-In Mak, and Rui P. Martins

FEATURES

A modified dynamic deviation reduction-based Volterra series digital predistorter
Fulfill the IEEE 802.11af standard
Large bandwidth, 54 to 600 MHz
Improved EVM, from 8.1% to 2.8%
Improved ACLR, 10 dB
Algorithm verified on a ST 65-nm CMOS TX prototype

DESCRIPTION

A new combinatorial impairment-compensation digital predistorter (DPD) for a sub-GHz IEEE 802.11af-WLAN CMOS transmitter (TX) is proposed.

For the TX to cover a 10x-wide bandwidth, the DPD implements a modified dynamic deviation reduction (DDR)-based Volterra series to jointly nullify the frequency-dependent I/Q imbalance, counter-inter-modulation (CIM) of mixers, and nonlinearities of power amplifier (PA) with memory effect.

The interactions of those impairments are firstly analyzed using two Volterra series. After applying the tandem properties of Volterra series, interactions of all impairments can be described in one Volterra series by bonding those impairments in parallel.

Coefficients of the DPD are extracted with the Least-Square (LS) estimator, achieving lower running complexity than the existing DPDs, which were developed to handle the PA nonlinearities only.

Verifications are based on both system-level simulations and silicon measurements of a 65-nm CMOS TX prototype. When the TX delivers a 6-MHz bandwidth, 2048-point, 64-QAM OFDM signal at 10 dBm output power, the measured EVM is <3.7% and adjacent channel leakage ratio (ACLR) is <-40.2 dBc under individual DPD applied at each RF.

A novel one-shot calibration for reuse in the entire TV-band is demonstrated also, showing EVM <4.2% and ACLR <-39.8 dBc.

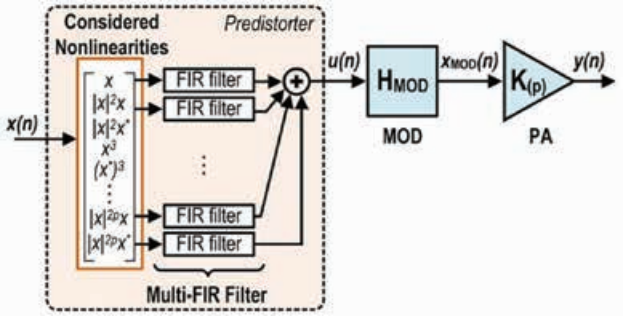

Fig. 1. Block schematic of the DPD addressing both CIM, I/Q imbalance, and RF nonlinearities.

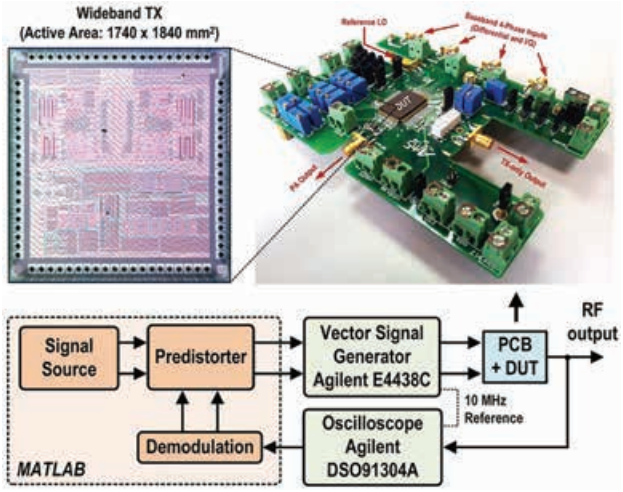

Fig. 2. Measurement setup. The DUT is a wideband TX fabricated in a 65-nm CMOS technology.

Publication(s):

[1] C.-F. Cheang, K.-F. Un, W.-H. Yu, P.-I. Mak, and R. P. Martins, "A Combinatorial Impairment-Compensation Digital Predistorter for a Sub-GHz IEEE 802.11af- WLAN CMOS Transmitter Covering a 10x-Wide RF Bandwidth," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 4, pp. 1025-1032, Apr. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Time-Interleaved Ring-VCO with Reduced 1/f³ Phase Noise Corner, Extended Tuning Range and Inherent Divided Output

Jun Yin, Pui-In Mak, Franco Maloberti, and Rui P. Martins

FEATURES

Reduced 1/f³ Phase Noise Corner, 90kHz to 150kHz
Extended Frequency Tuning Range
Inherent divided-by-5/7 output
Small area, 0.003mm²
Silicon verified in 65nm bulk CMOS

DESCRIPTION

This work is a time-interleaved (TI) ring-VCO (RVCO) exhibiting an improved phase noise over a wide range of frequency offsets, an extended tuning range and an inherent divided output. Such features are achieved by substantially increasing the number of delay stages in a RVCO, such that the rich multi-phase sub-outputs can be combined through a time-interleaved method, generating a high-frequency output with a significantly lowered 1/f³ phase noise corner (). The critical block is the phase combiner, which features a timing window to minimize the delay offset and mismatch. A reconfigurable TI factor extends the tuning range over the same range of supply voltage (V_{DD}). The prototype is a 35-stage dual-mode TI-RVCO occupying 0.003 mm² in 65-nm CMOS, and has a selectable TI factor of 5 and 7. The measured is 150 kHz at 3.47 GHz, which is 6.2x less than that of a typical 5-stage RVCO. The tuning range covers 1.7 to 3.5 GHz (68.5%) over V_{DD} = 0.7 to 1 V. The multi-phase sub-outputs are the inherent divided output (÷ 5 or ÷ 7) that can be directly utilized in a PLL to save area and power.

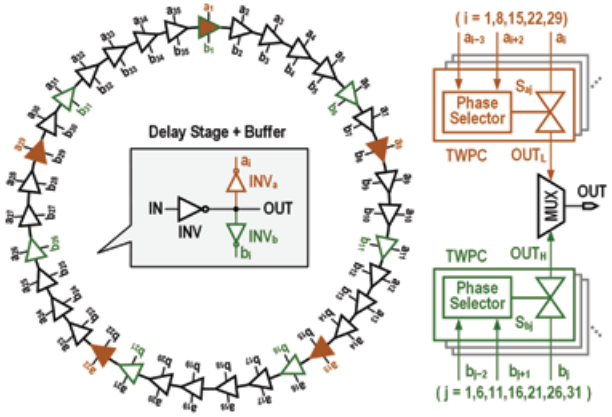

Fig. 1. Schematic of the proposed 35-stage dual-mode TI-RVCO.

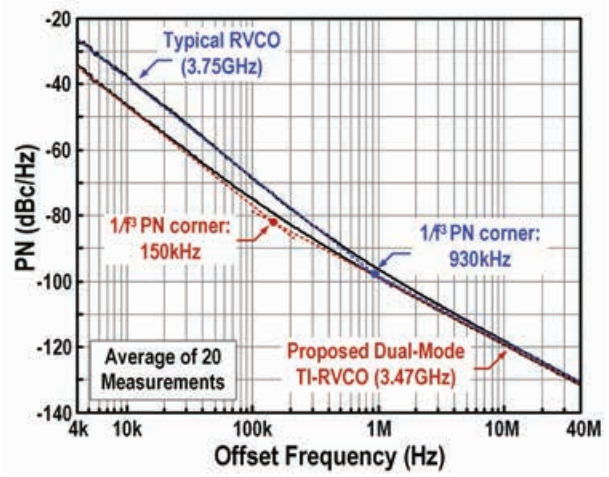

Fig. 2. Measured PN of the 35-stage dual-mode TI-RVCO and typical 5-stage RVCO at V_{DD} = 1V.

Publication(s):

[1] J.Yin*, P.-I. Mak*, F. Maloberti, and R. P. Martins*, "A Time-Interleaved Ring-VCO with Reduced 1/f³ Phase Noise Corner, Extended Tuning Range and Inherent Divided Output," IEEE Journal of Solid-State Circuits (JSSC), vol. 51, no. 12, pp. 2979-2991, Dec. 2016.

[2] J.Yin*, P.-I. Mak*, F. Maloberti, and R. P. Martins*, "A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f³ Phase-Noise Corner," IEEE International Solid- State Circuit Conference (ISSCC), Feb. 2016, pp. 48-49.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.038-mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop

Gengzhen Qi, Pui-In Mak, and Rui P. Martins

FEATURES

LO-defined Frequency (e.g., LTE Bands 5, 21, 2)
Low power consumption, 38.4 mW in transmit
20 mW in receive
Ultra-compact chip area, 0.038 mm²
Silicon verified in ST 65 nm CMOS

DESCRIPTION

In order to develop multiband cellular radios at low cost, on-chip N-path switched-capacitor (SC) filters are rekindled as a promising replacement of the off-chip SAW filters. The improved speed and parasitic effects of ultra-scaled CMOS technologies enable the N-path SC filters to provide tunable high-Q filtering over a wide range of frequencies.

This work is an N-path SC gain loop that can operate as an area-efficient SAW-less wireless transceiver (TXR) for multiband TDD communications. Unlike the typical direct-conversion transmitter (TX: BB Filter → I/Q modulation → PA driver) and receiver (RX: LNA → I/Q demodulation → BB Filter) that the functions are arranged in an open-loop style, here the signal amplification, bandpass filtering and I/Q (de)mod-ulation are unified in a closed-loop formation, being reconfigurable as a TX or RX with an LO-defined center frequency. The key advantages are low out-of-band (OB) noise in the TX mode, and high resilience to OB blockers in the RX mode.

Fabricated in 65-nm CMOS, the TXR prototype consumes up to 38.4 mW (20 mW) in the TX (RX) mode at the 1.88-GHz LTE-band2. The LO-defined center frequency covers >80% of the TDD-LTE bands with neither on-chip inductors nor external input-matching components. By properly injecting (extracting) the signals into (from) the N-path SC gain loop, the TX mode achieves an -1-dBm output power, a -40-dBc ACLREUTRA1 and a 2.0% EVM at 1.88 GHz, while showing a -154.5-dBc/Hz OB noise at 80-MHz offset. In the RX mode, a 3.2-dB NF and a +8-dBm OB-IIP3 are measured. The active area (0.038 mm2) of the TXR is 24x smaller than the state-of-the-art LTE solutions.

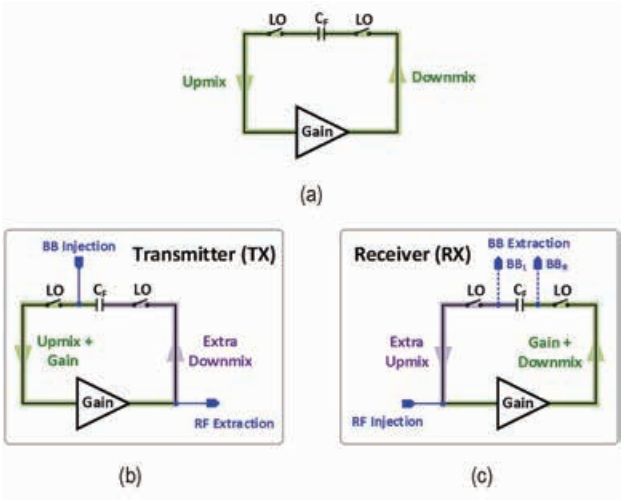

Fig. 1. An N-path SC gain loop operates as an area-efficient SAW-less wireless transceiver.

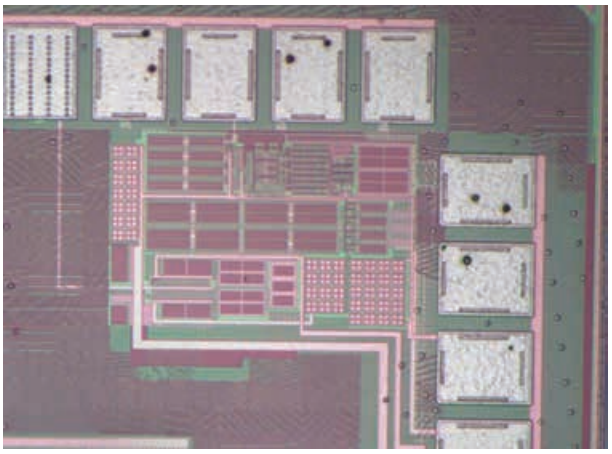

Fig. 2. Chip micrograph.

Publication(s):

[1] G. Qi, P.-I. Mak, R. P. Martins, "A 0.038-mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop," IEEE Journal of Solid-State Circuits, to appear, 2017.

[2] G. Qi, P.-I. Mak, R. P. Martins, "A 0.038mm² SAW-less Multi-Band Transceiver Using an N-Path SC Gain Loop," IEEE International Solid-State Circuits Conference (ISSCC), pp. 452-453, Feb. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS
HIGH RESOLUTION ADCs

A 12-Bit 110MS/s 4-Stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique

Rui Wang, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Zhihua Wang, and Rui P. Martins

FEATURES

Background Calibrated Multi-Stage Pipelined-SAR ADC
Ratio-Based Gain Error Calibration Technique
Only one PN Injection to Calibrate Multiple Gain Stages
Low Power consumption 12mW
High Sampling Rate, 120MHz
High Resolution, SNDR=63dB
Excellent Power efficiency, FoM_W=85fJ/step
Active Area, 0.12mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 12-bit 120MS/s multi-stage pipelined SAR ADC integrated through a single low-gain op-amp. A ratio-based GEC (Gain Error Calibration) technique is proposed to reduce the complexity of digital calibration circuit. A timing-derived technique is employed to share a single op-amp for residue amplification between pipelined SAR stages, where three non-overlap phases are allocated to maximize both usable bits and op-amp amplification time in each sampling period. Only one PN (Pseudo-random Number) signal is employed to perform the dither injection but calibrate multiple gain errors, and thus accelerates the convergence speed and minimizes the analog modification due to the background calibration. The effectiveness of the architecture is verified in a 65-nm CMOS chip whose active core area is 0.12 mm^2 only. The ADC obtains a peak SNDR of 63.2 dB and SFDR of 75.2 dB at 120MS/s consuming 12mW from a 1.2-V supply. Only 40 thousand points are needed to achieve desirable SNDR with the proposed calibration technique.

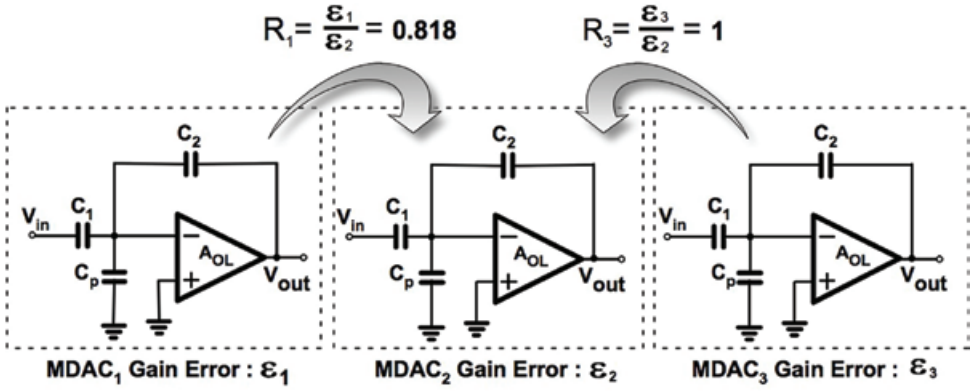

Fig. 1. Gain error ratios tracking between each MDAC.

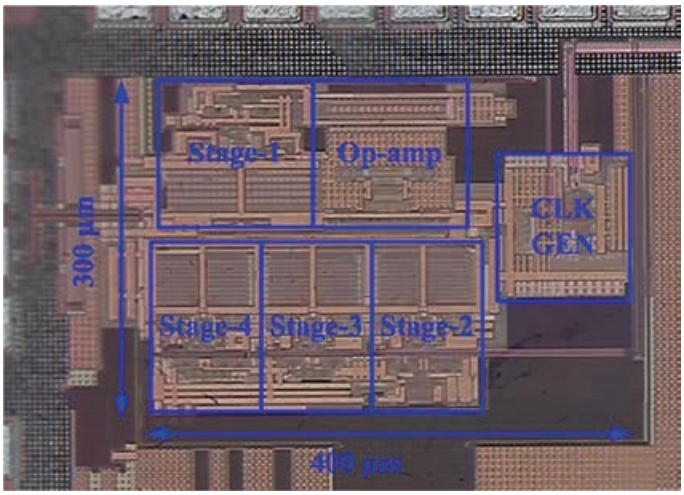

Fig. 2. Chip Photograph.

Publication(s):

[1] R. Wang*, U-Ft Chio*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*, "A 12-Bit 110MS/S 4-Stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique", in Proc. IEEE European Solid-State Circuits Conference – ESSCIRC 2012, Sept 2012.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 22.4μW 80dB SNDR ΣΔ modulator with passive analog adder and SAR Quantizer for EMG Application

Zhijie Chen, Yang Jiang, Chenyan Cai, He-Gong Wei, Sai-Wen Sin, Seng-Peng U, Zhihua Wang, and Rui P. Martins

FEATURES

Multi-bit Sigma-Delta ADC using SAR Quantizer
Passive Analog Summation in SAR DAC Array
Very Low Power consumption 22.4μW
Sampling Rate 1MS/s
High Resolution, SNDR=80dB
Good Power efficiency, FoM_W=130fJ/step
Active Area, 0.13mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

A Feed-Forward (FF) multi-bit ΣΔ modulator with passive analog adder and 4-bit Successive Approximation (SA) quantizer is presented. The scheme is composed by two SC integrators and a 4-bit SAR quantizer with feedback Data-Weighted Averaging (DWA). The modulator covers the 10KHz bandwidth according to electromyography application. The design utilizes the same DAC array of the SAR quantizer to realize analog summation for the FF signal, which significantly reduces the power dissipation and the silicon area. The modulator operates at 1MS/s with 1V supply. The prototype chip implemented in 65nm CMOS achieves 80dB SNDR and 81dB DR with 22.4μW power consumption. The Figure of Merit (FoM) is 0.13 pJ/conv.-step.

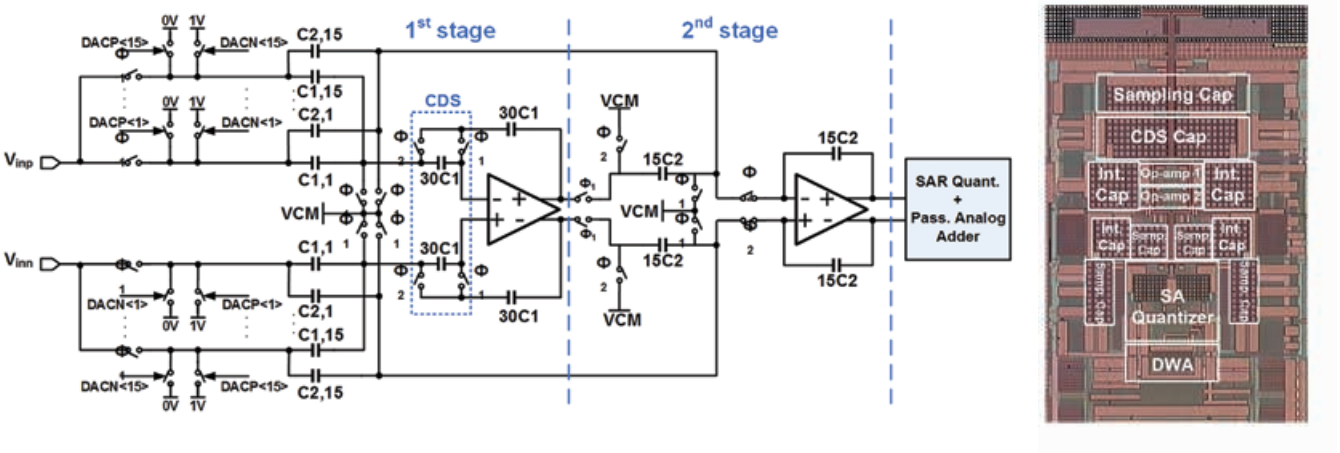

Fig. 1. Circuit Diagram of the Proposed Sigma-Delta ADC and Chip Photograph.

Publication(s):

[1] Z. Chen*, Y. Jiang*, C. Cai*, H.-G. Wei*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*, "A 22.4μW 80dB SNDR ΣΔ Modulator with Passive Analog Adder and SAR Quantizer for EMG Application", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 257-260, Nov 2012.

* Contributors with University of Macau

Sponsorship:

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A 13-bit 60MS/s Split Pipelined ADC with Background Gain and Mismatch Error Calibration

Li Ding, Wenlan Wu, Sai-Weng Sin, Seng-Pan, U, and Rui P. Martins

FEATURES

Split Pipelined ADC
Gain and Mismatch Calibration
Background Calibration
Power consumption 63.8mW
High Sampling Rate, 60MHz
High Resolution, SNDR=69dB
Good Power efficiency, FoM_W=452fJ/step
Active Area, 0.93mm^2
Silicon verified in UMC 90nm CMOS

DESCRIPTION

A comprehensive background gain and mismatch error calibration technique is proposed for split ADC, without injecting any test signal. By employing comparator threshold random selection method, the input/output transfer characteristics of each split ADC channel is differed, which allow their residue transfer curves are uncoupled and hence the calibration can be extended to any pipeline stages. Based on Least Mean Square (LMS) adaptation the interstage gain error and capacitor mismatch error are corrected. All the estimations and corrections are performed in digital domain, resulting in little analog circuit modification. The proposed calibration technique is applied on a 13-bit 60MS/s pipelined ADC. Fabricated in a 90nm CMOS process, the ADC achieves 70.8dB SNDR at a power consumption of 63.8mW. The FoM is 377fJ/ step at DC and 452 fJ/ step at Nyquist.

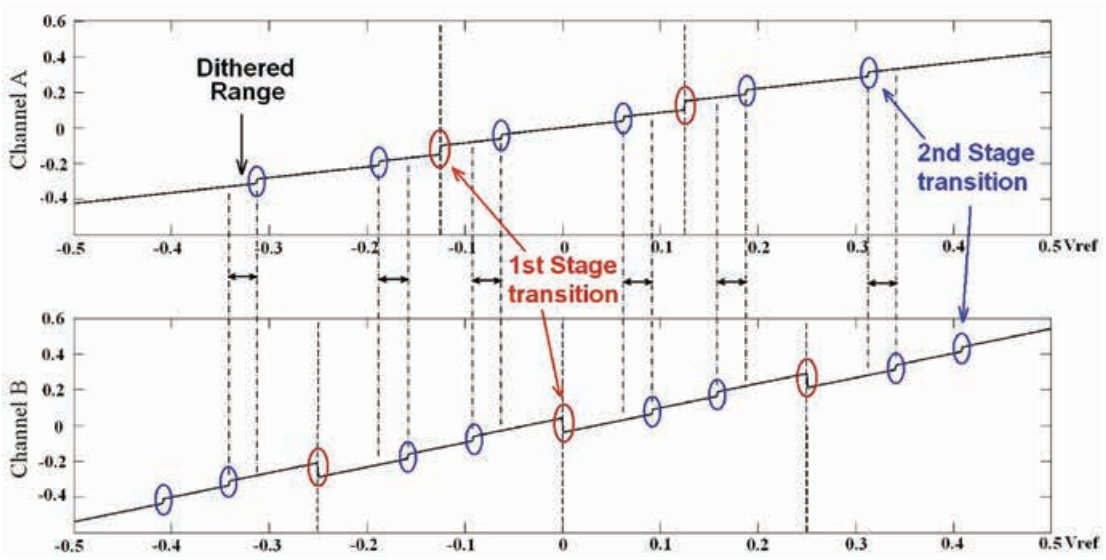

Fig. 1. Proposed Dithered ADC Transfer Characteristics.

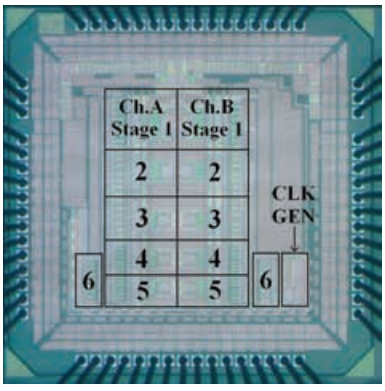

Fig. 2. Chip Photograph.

Publication(s):

[1] L. D., W. Wu, S.-W. Sin, S.-P., U, R .P. Martins, " A 13-bit 60MS/s split pipelined ADC with background gain and mismatch error calibration ", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 77-80, Nov 2013.

* Contributors with University of Macau

Sponsorship:

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Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters

Da Feng, Franco Maloberti, Sai-Weng Sin, and Rui P. Martins

FEATURES

Theoretical Analysis of the Polyphase Decomposition Technique to the NTF of Band-Pass ΣΔ modulators
Generalized and Tunable Band-Pass Implementation
Mismatch Spurs Out-of-band
Applicable to MASH structures

DESCRIPTION

The use of the polyphase decomposition technique applied to the noise transfer function (NTF) of band-pass sigma-delta (BPΣΔ) modulators is introduced and theoretically analyzed. Schemes for a second order and fourth order bandpass noise shaping are discussed in detail. The class of architectures studied here does not use resonators and avoids spur tones in the signal band. Those architectures are based on the polyphase decomposition applied only to the NTF of band-pass modulators (or to any other NTF responses). The signal transfer function (STF) remains unchanged with respect to the originating single path. The method is usable for any order but the analog inaccuracy limits its application. It is shown that an extension to MASH configurations is possible. The method allows tunability of the center frequency over a wide frequency range. Moreover, MASH schemes allow a rough-fine tuning with the rough tuning in the analog section followed by a fine digital adjustment. Simulation results verify the benefits and outline possible limits.

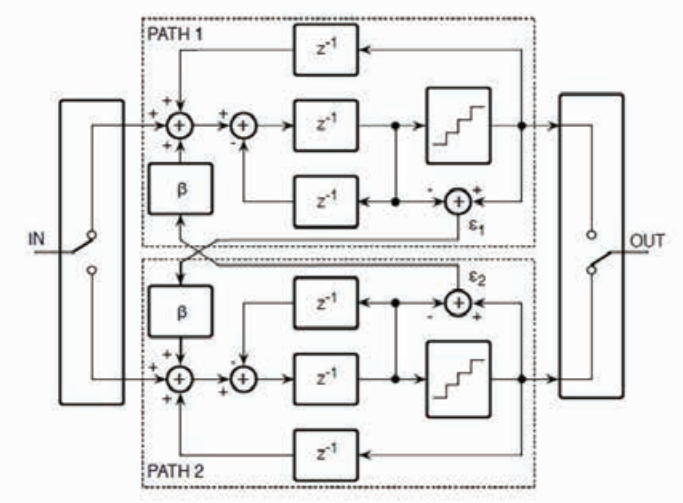


Fig. 1. A 2nd order band-pass polyphase sigma-delta ADC.

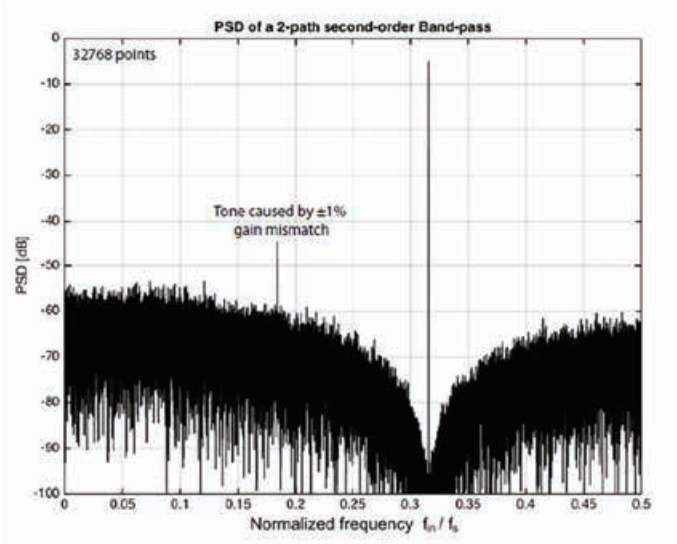


Fig. 2. FFT Spectrum.

Publication(s):

[1] D. Feng, F. Maloberti, S.-W. Sin, R. P. Martins, "Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 5, Issue 4, pp. 537-547, Dec. 2015.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A High DR Multi-Channel Stage-Shared Hybrid Sigma-Delta Analog Interface for Integrated Power Electronics Controller Front-End

Yuan Ren, Sai-Weng Sin, Chi-Seng Lam, Man-Chung Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Hybrid CT-DT ΔΣ Modulator with PGA Front-End
Opamp Shared in Discrete Stage
Low power consumption,68μW/Channel
High Dynamic Range, 98dB
Excellent Power efficiency, FoM_S = 179dB
Very Small Active Area, 0.03mm²/channel
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 4-channel power electronics (PE) controller front-end interface with input signal conditioning and analog-to-digital (A/D) conversion functions for different power electronics system applications. The proposed front-end is composed of a 4-channel continuous-time (CT) and discrete-time (DT) hybrid sigma-delta modulator (H-ΣΔM) embedding an input programmable-gain (PGA) in the first CT stage in order to enhance the dynamic range (DR). The second shared DT stage is designed to utilize multiple-sampling technique with a shared single Op-Amp for low power consumption. This PE controller front-end chip is fabricated with 65 nm CMOS technology. Measurement results show a high dynamic range of 98.3 dB and 84.2 dB SNDR, while achieving a power consumption of 68 μW per channel and a FoMS of 172-179 dB due to the dynamic range boost.

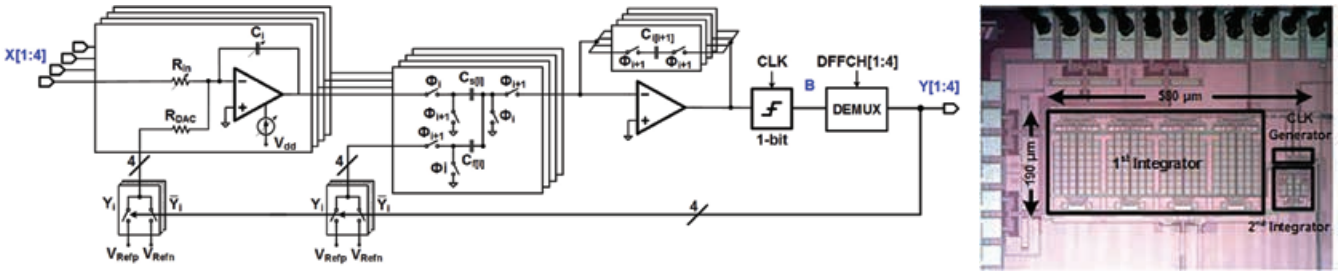


Fig. 1. The Multi-Channel Front-End Architecture and Chip Photograph.

Publication(s):

[1] Y. Ren, S.-W. Sin, C.-S. Lam, M.-C. Wong, S.-P. U, R. P. Martins, " A High DR Multi-Channel Stage-Shared Hybrid Front-End for Integrated Power Electronics Controller", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 1-4, Nov 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing

Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, and Rui P. Martins

FEATURES

Cascaded MASH DT-ΔΣ Modulator
Proposed Multirate Opamp Sharing Scheme
Low power consumption, 4.2mW
Wide bandwidth, 5MHz
High Resolution, SNDR=77.1dB
Excellent Power efficiency, FoM_S=168dB
Very Small Active Area, 0.066mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a discrete time (DT) 2-1 MASH Delta-Sigma (ΔΣ) modulator with multirate opamp sharing for Analog-to-Digital Converters (ADC), targeting the optimization of power efficiency in active blocks, like opamps and quantizers. Through the allocation of different settling times to the opamps and by adopting the multirate technique, the power of the shared opamps is utilized more efficiently, and the 4-bit SAR quantizer and the Data Weighted Averaging (DWA) in the first stage enjoy additional operation time. Moreover, a detailed analysis and related simulations are presented to validate the enhanced opamp power efficiency in the proposed sharing scheme. The 65nm CMOS experimental chip running at multirate 120/240MHz achieves a mean SNDR of 77.1dB for a 5MHz bandwidth, consuming 4.2mW from a 1.2V supply and occupying 0.066mm2 core area. It exhibits a Walden FoM of 69.7fJ/conv-step and a Schreier FoM of 167.9dB based on SNDR.

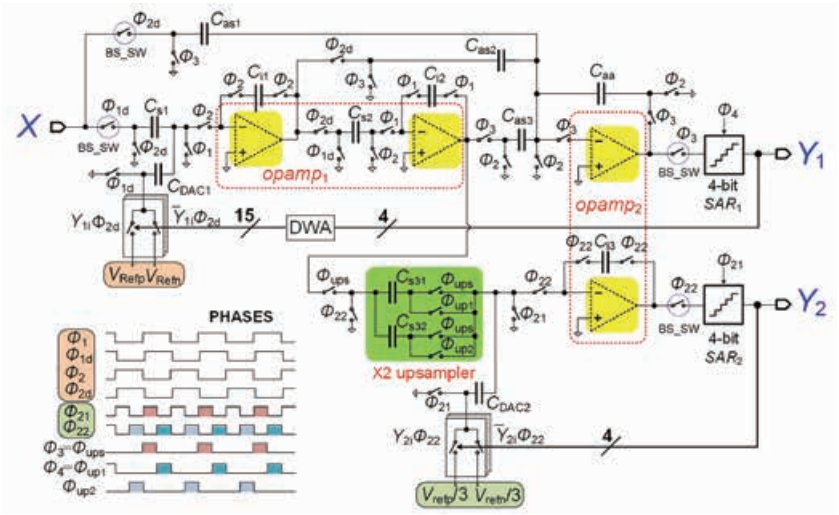


Fig. 1. ADC architecture.

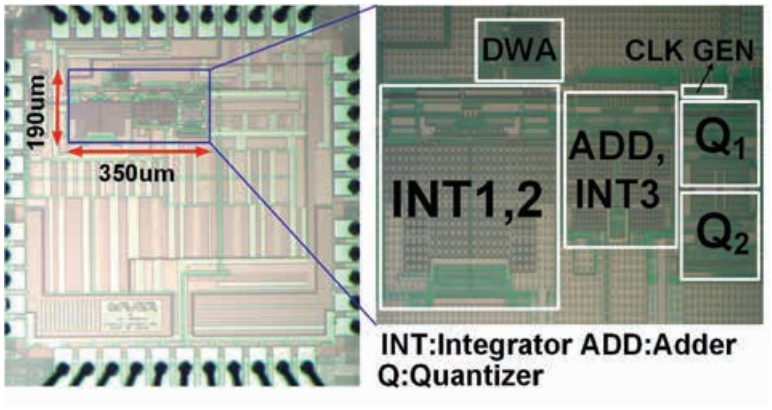


Fig. 2. Chip Photograph.

Publication(s):

[1] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, R. P. Martins, " A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing", IEEE Trans. of Circuits and Systems I – Regular Papers. in press, 2017.

[2] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, R. P. Martins, " A 12.5-ENOB 5MHz BW 4.2mW DT Multirate 2-1 Mash ΔΣ Modulator with Horizontal/Vertical Opamp Sharing in 65nm CMOS' in IEEE International Solid-State Circuits Conference, Student Research Preview, Jan 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Active-Passive ΔΣ Modulator for High Resolution and Low Power Applications

Arshad Hussain, Sai-Weng Sin, Chi-Hang Chan, Seng-Pan U, Franco Maloberti, and Rui P. Martins

FEATURES

Hybrid Active-Passive Integrator DT-ΔΣ Modulator
Proposed Positive Feedback NTF Zero Compensation
Very Low power consumption, 73.6μW
Audio bandwidth, 25kHz
High Resolution, SNDR=88.2dB
Excellent Power efficiency, FoM_S=176dB
Very Small Active Area, 0.1mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper discusses the use of a Low Gain Amplifier and a Passive Switched-capacitor (SC) network to enable the SC integrator function. The method is applied to a Delta-sigma Modulator to achieve high resolution as proven by the 65nm CMOS Technology Test Vehicle. Compared to the conventional operational amplifier (op-amp) based SC integrator, this solution utilizes a low gain open loop amplifier to drive a passive SC integrator with positive feedback. Since the open loop amplifier requires a low DC gain and implements an embedded current adder, the power consumption is very low. Power reduction is obtained by using passive feedforward with built-in adder to assist the first amplifier. The low swing obtained at the output of the active blocks relaxes the slew rate requirement and enhances the linearity. Implemented in 65-nm digital CMOS technology with an active area of 0.1-mm², the test chip achieves a dynamic range (DR) of 91dB, peak signal-to-noise ratio (SNR) of 88.4dB, peak signal-to-noise-plus-distortion ratio (SNDR) of 88.2dB, and a spurious free dynamic range (SFDR) of 106dB while consuming 73.6μW in a 25-kHz signal bandwidth at 1V supply, yielding a Walden FoM of 70fJ/Conversion-Step and Schreier FoM of 176dB.

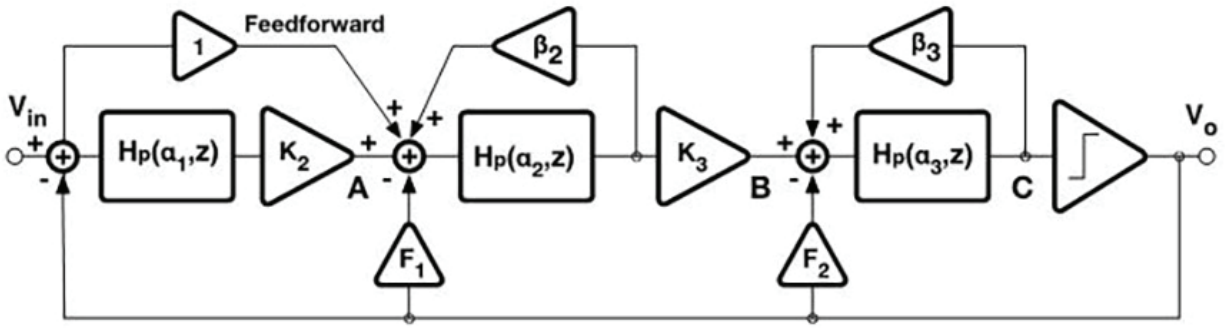


Fig. 1. ADC architecture.

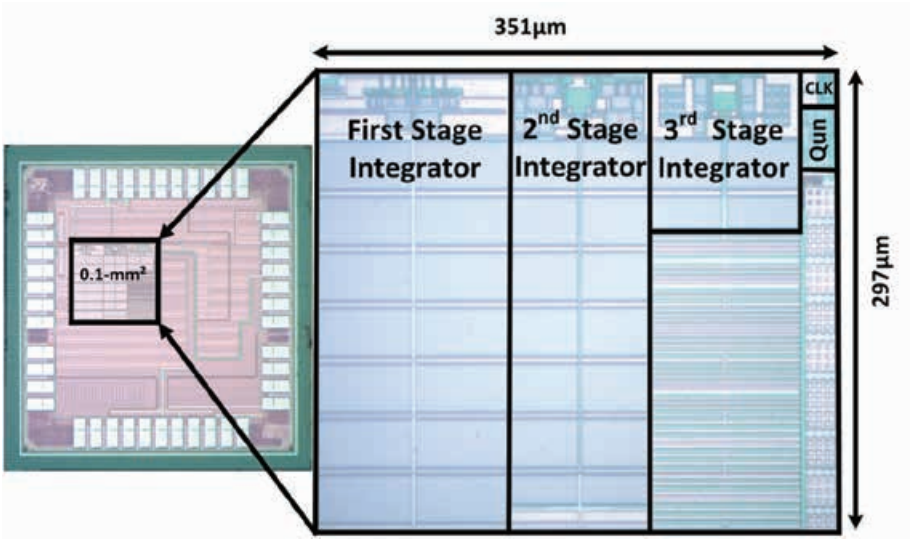


Fig. 2. Chip Photograph.

Publication(s):

[1] A. Hussain, S.-W. Sin, C.-H. Chan, S.-P. U, F. Maloberti, R. P. Martins, "Active-Passive ΔΣ Modulator for High-Resolution and Low-Power Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 1, pp. 364 – 374, Jan 2017.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS
HIGH SPEED ADCs

A 7-bit 300-MS/s Subranging ADC with Embedded Threshold & Gain-Loss Calibration

U-Fat Chio, Chi-Hang Chan, Hou-Lon Choi, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Low Power Subranging ADC with
Reference Voltages Embedded
Reference Errors and
Subranging Gain Loss Calibrated
Low Power consumption 2.7mW
High Sampling Rate 300MS/s
7b Resolution, SNDR=39dB
Good Power efficiency, FoM_W=88fJ/step
Small Active Area, 0.1mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work reports a 7-bit 300-MS/s subranging ADC fabricated in standard 65nm CMOS, which utilizes embedded reference and gain loss error calibration techniques. A shared passive capacitive DAC array performs the input sampling in quantization mode and reference generation in calibration mode, providing a linear, accurate and compact calibration implementation. The sign comparator with the threshold at mid-supply quantizes the B1 (MSB) which determines the connection of folding switches between the DAC and the 3-bit flash in the CADC. As a consequence of the developed calibration techniques, uniform-sized dynamic comparators are employed to reduce the process-mismatch variation and nonlinearity error, when compared with the conventional structures. The ADC achieves peak SNDR of 40.5dB at 300MS/s and 39dB at 400MS/s, with ERBW of 300MHz and 350MHz, respectively. The power consumption is 2.3mW only from 1.2-V supply at 300MS/s.

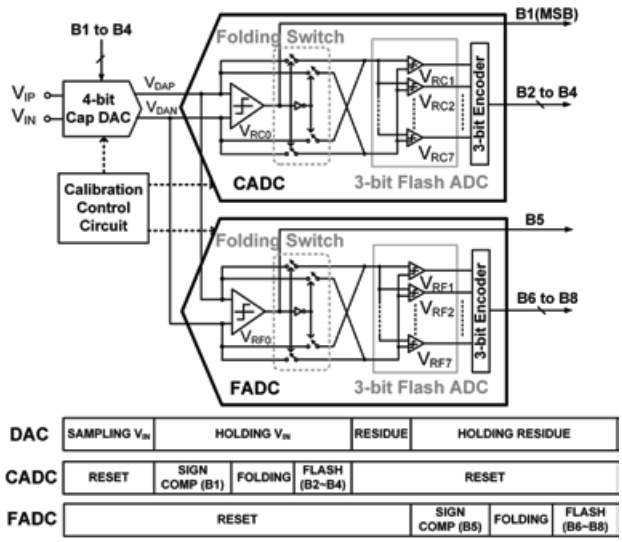


Fig. 1. Proposed ADC circuit diagram.

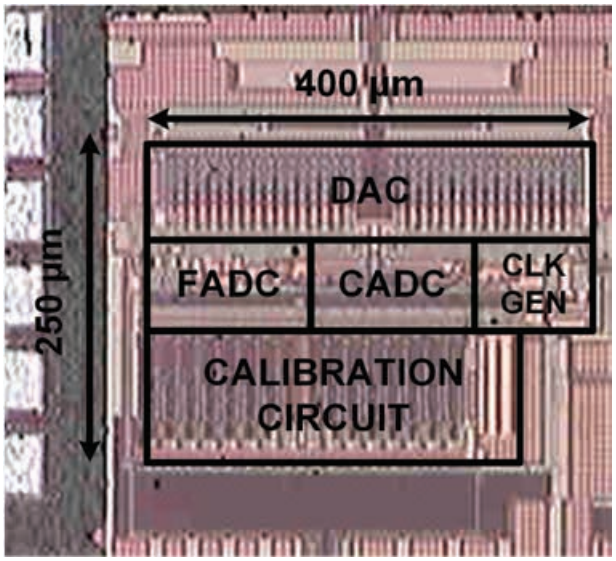


Fig. 2. Chip Photograph.

Publication(s):

[1] U-F. Chio, C.-H. Chan, H.-L. Choi, S.-W. Sin, S.-P. U, R. P. Martins, " A 7-bit 300-MS/s Subranging ADC with Embedded Threshold & Gain-Loss Calibration", in IEEE European Solid-State Circuits Conference – ESSCIRC, pp. 363-366, Sept 2011.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.024 mm² 4.9 fJ 10-bit 2 MS/s SAR ADC in 65 nm CMOS

Guohe Yin, He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Zhihua Wang, and Rui P. Martins

FEATURES

Extreme Low Power SAR ADC for Biomedical / Sensor Applications
Small Capacitor Array is utilized in MSB Conversion to Save Energy
Very Low Power consumption 6.6μW
Sampling Rate 2MS/s
Medium Resolution, SNDR=58.4dB
Excellent Power efficiency, FoM_W=4.9fJ/step
Very Small Active Area, 0.024mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a Successive Approximation Register Analog-to-Digital (SAR ADC) design for sensor applications. In this proposed ADC architecture, the conversion does not start from the largest capacitor. An energy-saving switching technique, by utilizing small capacitor Array in MSB conversion first, is proposed to achieve ultra low power consumption. This switching technique is simple with two advantages in saving switching energy. First, the first-step conversion completes in the smaller capacitor instead of the larger capacitor; Second, if the first bit code is zero, there is no need to charge the large capacitor. Both of these can save significant power consumption. The measured signal-to-noise-and-distortion ratios (SNDR) of the ADC is 58.4 dB at 2 MS/s sampling rate with an ultra-low power consumption of only 6.6 μW from a 0.8V supply voltage, resulting in a figure of merit (FOM) of 4.9 fJ/conversion-step. The prototype is fabricated in 65 nm CMOS technology with area of 0.024 mm².

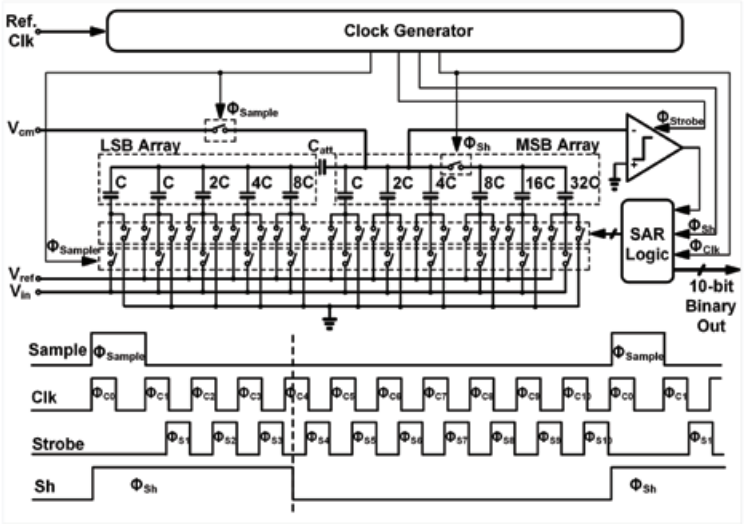


Fig. 1. Proposed ADC circuit diagram.

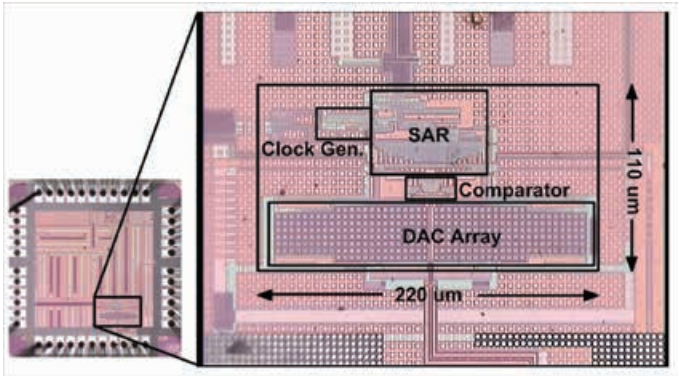


Fig. 2. Chip Photograph.

Publication(s):

[1] G.Yin*, H.-G. Wei*, U-F. Chio*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*,"A 0.024 mm2 4.9 fJ 10-bit 2 MS/s SAR ADC in 65 nm CMOS ", in IEEE European Solid-State Circuits Conference – ESSCIRC 2012, Sept. 2012.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 50-fJ 10-b 160-MS/s Pipelined-SAR ADC Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation

Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Shared Opamp in interleaved pipeline SAR ADC
Reused 1st Stage SAR DAC for flip around MDAC
Offset calibration onchip
~30 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a time-interleaved pipelined-SAR ADC with on-chip offset cancellation technique. The design reuses the SAR ADC to perform offset cancellation, thus saving calibration costs. The inter-stage gain of 8 is implemented in a 6-bit capacitive DAC with a flip-around operation. A capacitive attenuation used in both the first and second DACs significantly reduces the power dissipation and optimizes conversion speed. The detailed circuit implementation of the subthreshold op-amp is discussed, and the possible limits caused by nonidealities are analyzed for a proper correction in the design. These include the inter-stage-gain error and various channel mismatches of offset, gain, and timing. Measurements of a 65-nm CMOS prototype operating at 160 MS/s and 1.1-V supply show an SNDR of 55.4 dB and 2.72 mW total power consumption.

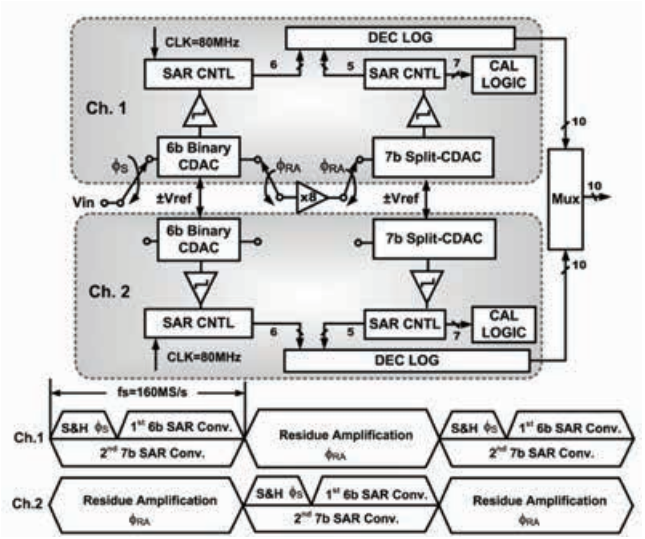


Fig. 1. Overall ADC architecture.

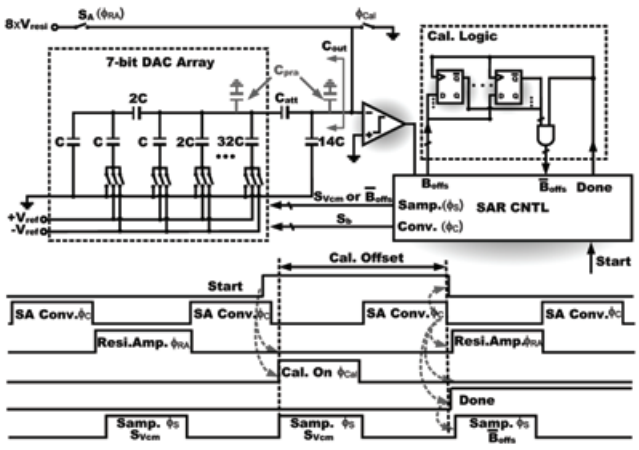


Fig. 2. Second-stage SAR ADC architecture and calibration timing diagram.

Publication(s):

[1] Y. Zhu*, C. H. Chan*, S. W. Sin*, S.-P. U*, R. P. Martins*, F. Maloberti, "A 50fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation", IEEE Journal of Solid-State Circuits, Dec. 2012.

[2] Y. Zhu*, C. H. Chan*, S. W. Sin*, S.-P. U*, R. P. Martins*, F. Maloberti, "A 35 fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation", in IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 61-64, Nov. 2011.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470Ms/s Pipelined-SAR ADC

Jianyu Zhong, Yan Zhu, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Inter-stage gain error calibration
Mapping table based calibration
Low completion time for calibration
~31 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper proposes an Inter-Stage Gain Error (ISGE) calibration method devoted to correct the residue gain errors induced by the parasitic effects, non-ideal op-amp gain and capacitor mismatch, and also the mismatched for supply-derived reference voltages between two stages for Pipelined-SAR ADC. The calibration reuses the SAR ADC to estimate the overall inter-stage gain error and compensates it in the 2nd-stage DAC in 2 cycles, and it is implemented in a Pipelined-SAR which achieves 10b 470MS/s in 65nm CMOS with the FoM of 31.5fJ/conv.-step by consuming only 6% of the total ADC area (0.049mm²).

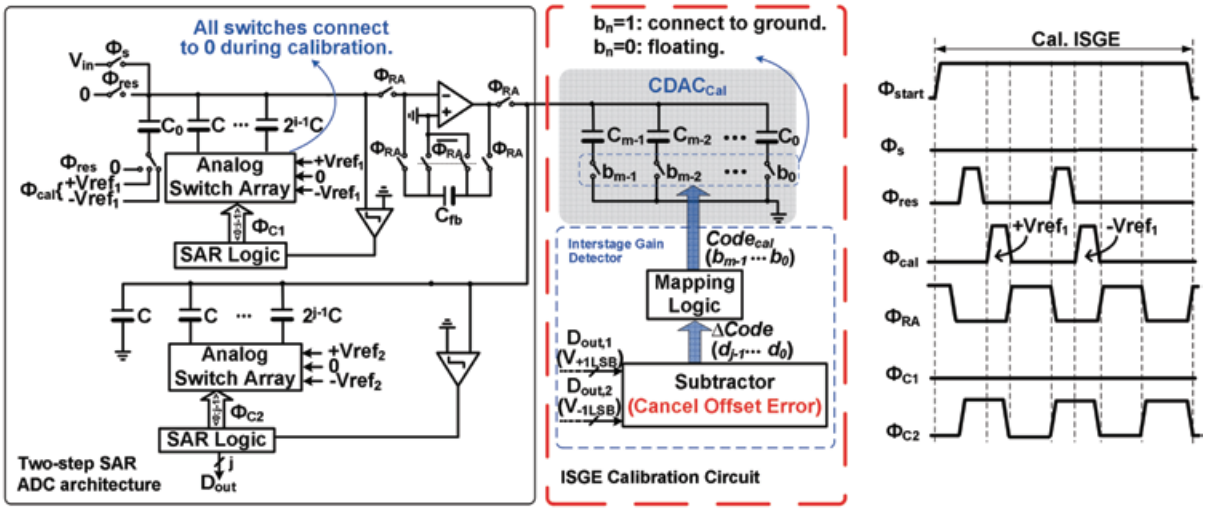


Fig. 1. Two-step SAR ADC with the ISGE calibration and timing diagram.

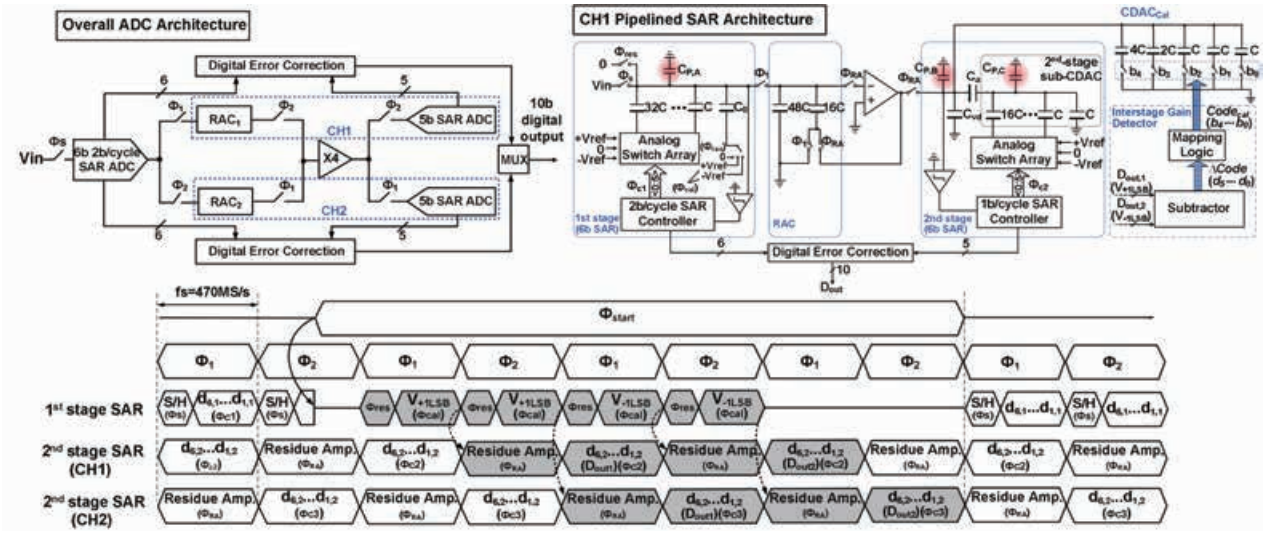


Fig. 2. PI Pipelined SAR ADC with the implementation of the ISGE calibration and timing diagram.

Publication(s):

[1] J. Zhong, Y. Zhu, S. W. Sin, S.-P. U, R. P. Martins, "Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470MS/s Pipelined-SAR ADC", IEEE Asian Solid-State Circuit Conference (A-SSCC), pp 153-156, Nov-2012.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC

Si-Seng Wong, U-Fat Chio, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Two-Step, Binary Search then Interleaved SAR
process insensitive asynchronous logic
Low power consumption, 2.3mW
Moderate Resolution, 10b
Excellent Power efficiency, 36.4fJ/step
Active Area, 0.1 mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents the architecture of a 10b 170 MS/s two-step binary-search assisted time-interleaved SAR ADC, which takes the advantages of speed, resolution, and power offered by the two types of ADCs. The front-end stage of this ADC is built with a 5b binary-search ADC, which is shared by two time-interleaved 6b SAR ADCs in the 2nd-stage. The design does not use any static component such as op-amp or pre-amplifier that causes large dissipation of static power. DAC settling speed and power are also relaxed thanks to this architecture. Besides, the process insensitive asynchronous logic further reduces the delay of SA loop rather than using worst case delay cells to compensate the process variation problem. The ADC was fabricated in 65 nm CMOS and achieves 54.6 dB SNDR at 170 MS/s with only 2.3 mW of power consumption, leading to a FoM of 30.8 fJ/conversion-step.

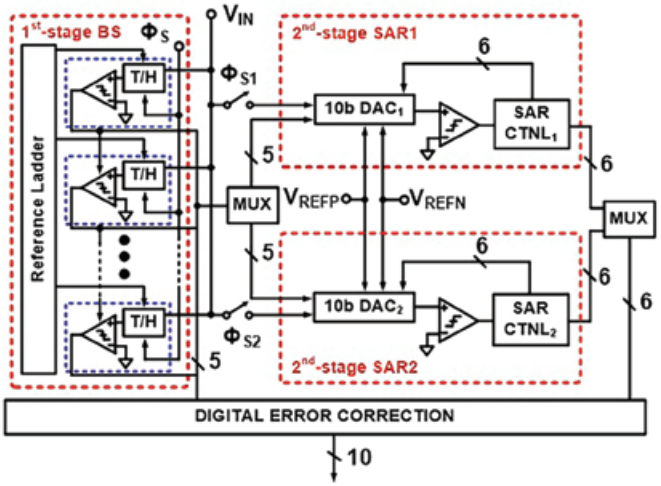


Fig. 1. ADC architecture.

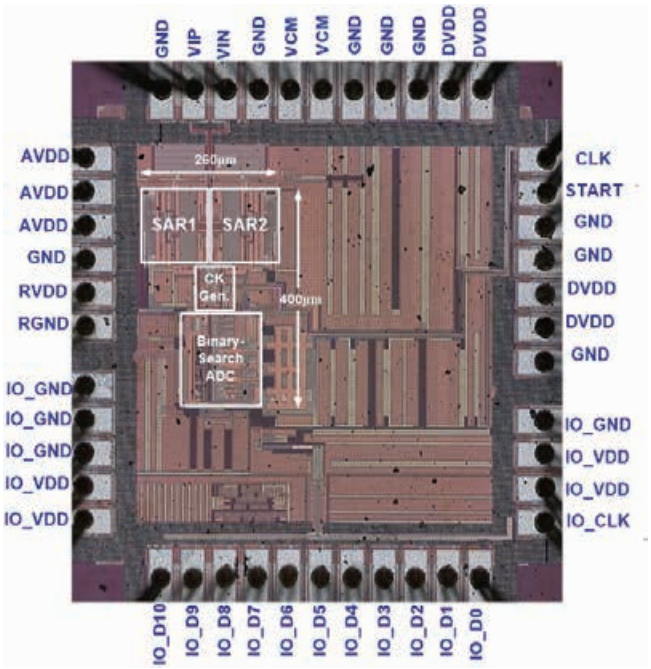


Fig. 2. Chip Photograph.

Publication(s):

[1] S.-S. Wong, U-F. Chio, Y. Zhu, S.-W. Sin, S.-P. U, R. P. Martins, "A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC", in IEEE Journal of Solid-State Circuits, vol. 48, Issue 8, pp. 1783-1794, Aug 2013.

[2] S.-S. Wong, U-F. Chio, Y. Zhu, S.-W. Sin, S.-P. U, R. P. Martins, "A 2.3mW 10-bit 170MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC," in Proc. of IEEE Custom Integrated Circuits Conference – CICC, Sept 2012.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Split-SAR ADCs: Improved Linearity With Power and Speed Optimization

Yan Zhu, Chi Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Switching techniques analysis
DNL and INL in SAR ADC
Switching energy in SAR ADC
Verified in UMC 90nm CMOS

DESCRIPTION

This paper presents the linearity analysis of a successive approximation registers (SAR) analog-to-digital converters (ADC) with split DAC structure based on two switching methods: conventional charge-redistribution and V_{cm}-based switching. The static linearity performance, namely the integral nonlinearity and differential nonlinearity, as well as the parasitic effects of the split DAC, are analyzed hereunder. In addition, a code-randomized calibration technique is proposed to correct the conversion nonlinearity in the conventional SAR ADC, which is verified by behavioral simulations, as well as measured results. Performances of both switching methods are demonstrated in 90 nm CMOS. Measurement results of power, speed, and linearity clearly show the benefits of using V_{cm}-based switching.

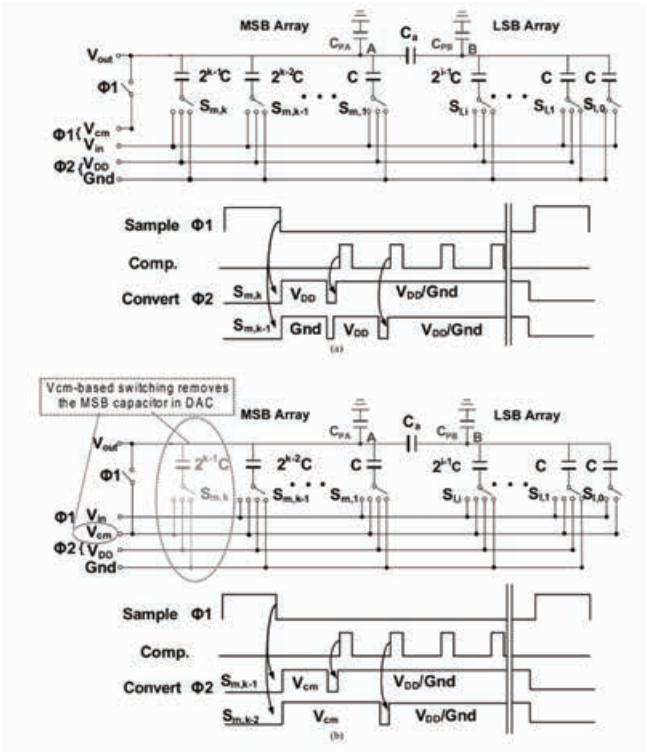


Fig. 1. Single-ended n-bit and (n – 1)-bit split capacitive DAC arrays with their switching timing diagrams (n = k + i). (a) Conventional switching. (b) V_{cm}-based switching.

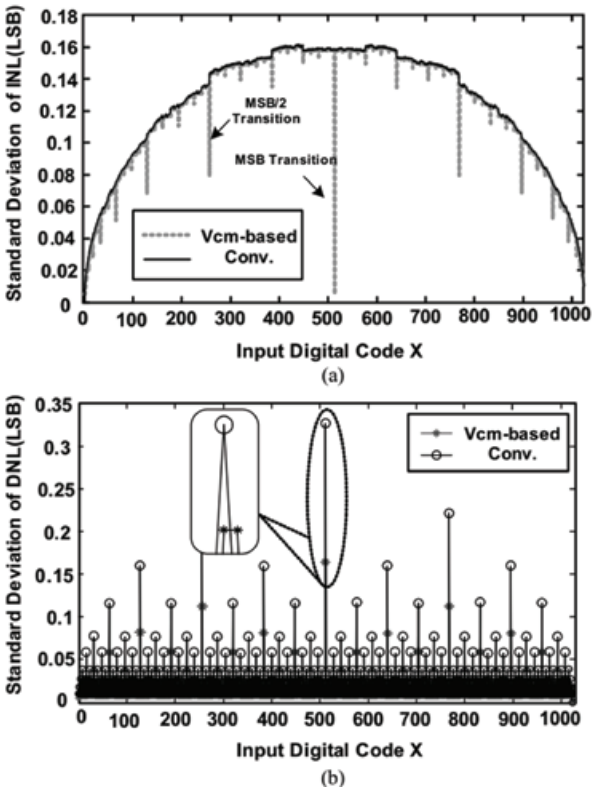


Fig. 2. Behavioral simulation comparing the DNL and INL of conventional and V_{cm}-based 10-b SAR ADCs.

Publication(s):

[1] Y. Zhu*, C. H. Chan*, U-F. Chio*, S. W. Sin*, S.-P. U*, R. P. Martins*, and F. Maloberti, "Split-SAR ADCs: Improved Linearity with Power and Speed Optimization," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Feb-2014.

* Contributors with University of Macau

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs

Jianyu Zhong, Yan Zhu, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Noise analysis in two architectures
Analyzed reference noise in SAR ADC
Provided design guideline for SAR and Pipeline SAR ADC
Simulation verified in ST 65nm CMOS

DESCRIPTION

This paper analyzes the thermal and reference noises of two types of successive-approximation-register (SAR) analog-to-digital converters (ADCs): the time-interleaving (TI) and the partial-interleaving (PI) Pipelined. The thermal noise is investigated with accurate estimation by deriving closed-form expressions according to the noise equivalent models on different phases. Additionally, the design trade-off between power and noise for two ADC architectures is discussed in detail. On the other hand, the reference noise due to the large switching transient, which significantly degrades the conversion accuracy, is analyzed and verified through behavioral and circuit level simulations of two ADC architectures operating at 500 MS/s for 10-bit resolution. The simulated results show the supremacy of the PI Pipelined-SAR (PS) architecture over the TI-SAR because it exhibits less reference noise sensitivity.

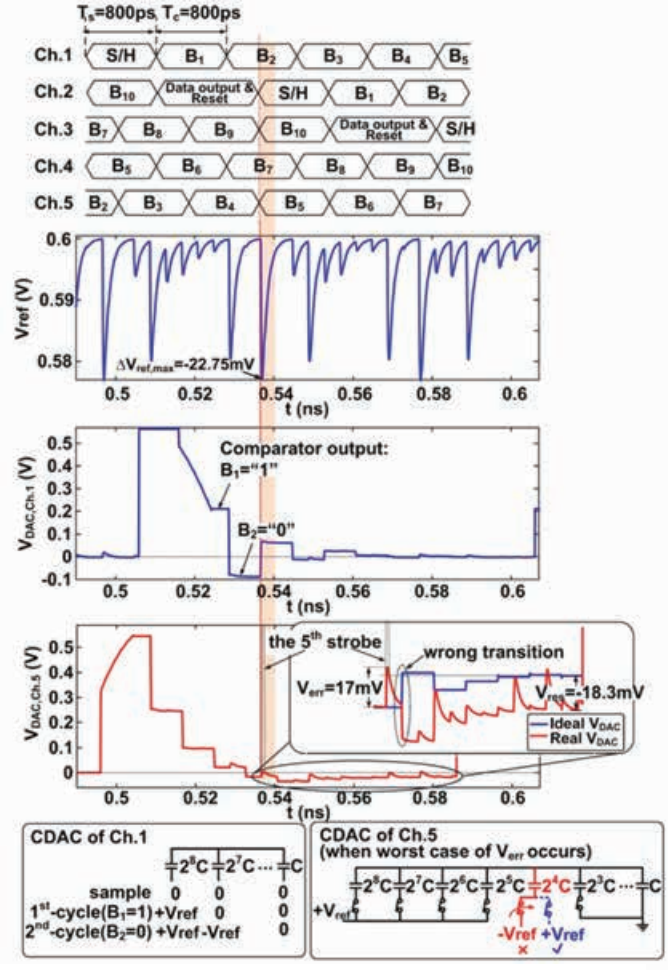


Fig. 1. The worst case of reference ripples in the TI-SAR ADC.

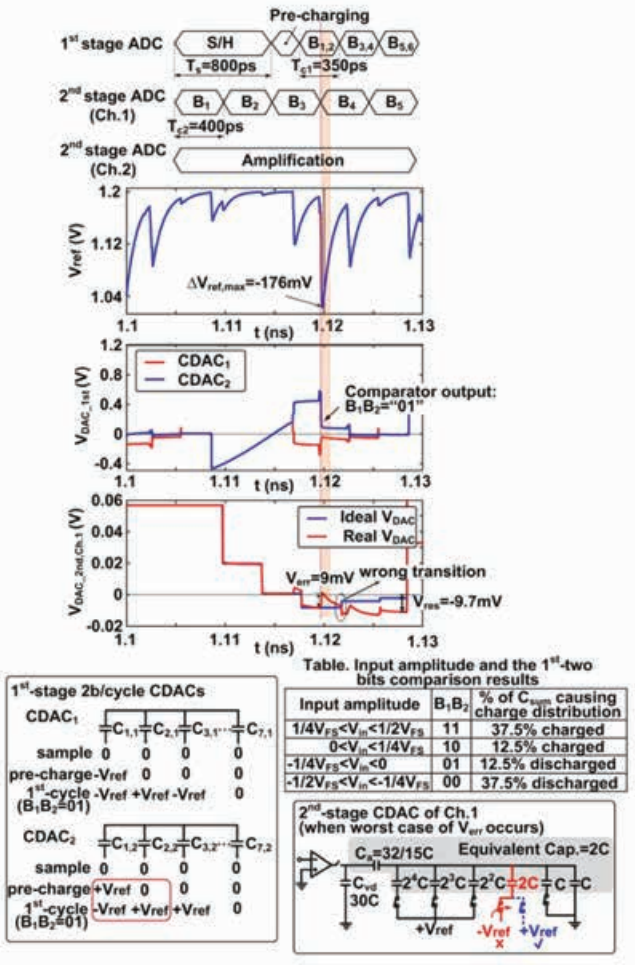


Table. Input amplitude and the 1st-two bits comparison results

Input amplitude	B_1B_2	% of C_{sum} causing charge distribution
$1/4V_{FS}<V_{in}<1/2V_{FS}$	11	37.5% charged
$0<V_{in}<1/4V_{FS}$	10	12.5% charged
$-1/4V_{FS}<V_{in}<0$	01	12.5% discharged
$-1/2V_{FS}<V_{in}<-1/4V_{FS}$	00	37.5% discharged

Fig. 2. The worst case of reference ripples in the PI PS ADC.

Publication(s):

[1] J. Zhong, Y. Zhu, S. W. Sin, S.-P. U, R. P. Martins, "Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs", IEEE Transactions on Circuits and Systems I: Regular Papers, Sep-2015.

Sponsorship:

Research Committee of the University of Macau, Macao Science and Technology Development Fund (FDCT)

Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC

Yan Zhu, Chi Hang Chan, S.-S. Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Gain error calibration
Histogram-based enhance accuracy
Verified with a SAR ADC design
~30 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This brief reports a 120 MS/s 12-bit successive approximation register analog-to-digital converter (ADC). The conversion nonlinearity in a bridge digital-to-analog converter is analyzed, and its corresponding histogram-based ratio mismatch (HBRM) calibration is presented in detail. Verified by behavioral simulations as well as measured results, the solution improves both the dynamic performance and the static performance of the ADC.

The measurement results demonstrate that the HBRM calibration effectively improves the signal-to-noise distortion ratio from 56.9 to 63.7 dB at dc input, with a sampling frequency of 120 MS/s.

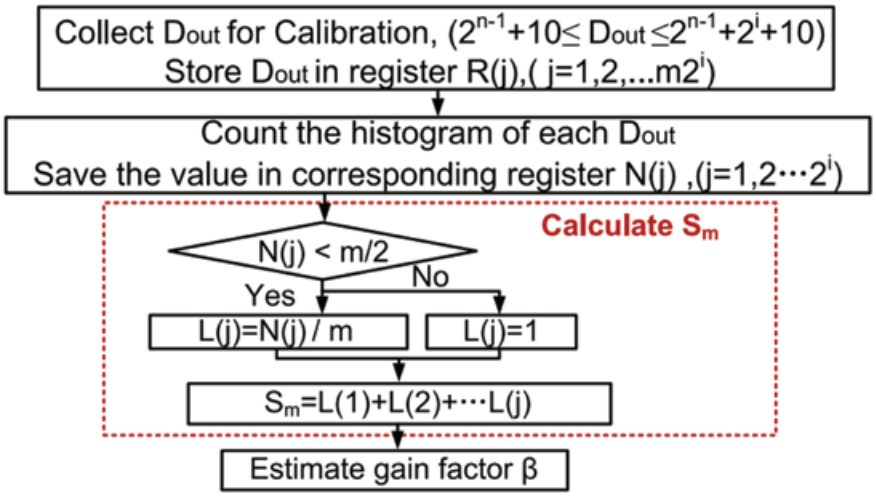


Fig. 1. Flowchart of the HBRM calibration.

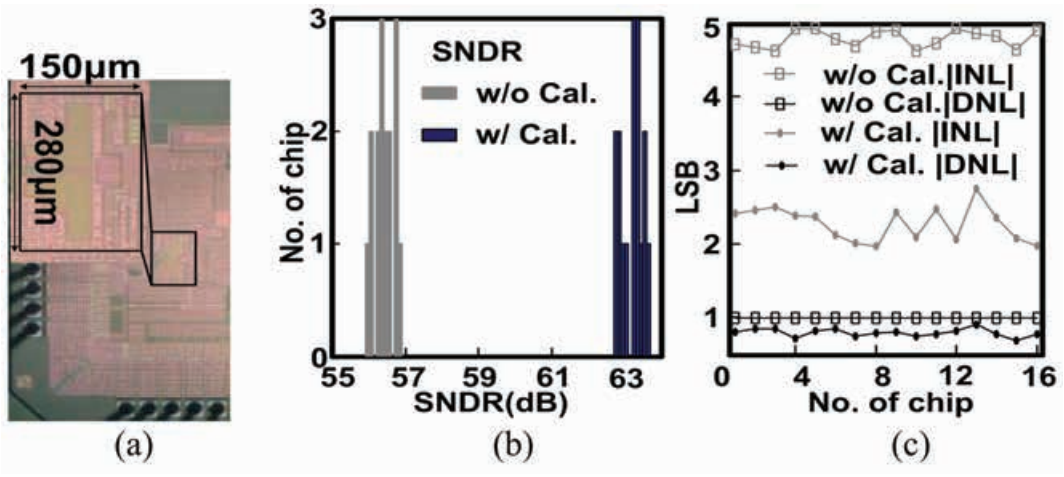


Fig. 2. (a) Chip photograph of SAR ADC. (b) Measured SNDR of total 16 chips. (c) Measured DNL and INL of total 16 chips.

Publication(s):

[1] Y. Zhu, C. H. Chan, S.-S. Wong, S.-P. U, R. P. Martins, "Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Jun-2015.

[2] Y. Zhu, C. H. Chan, S.-P. U, R. P. Martins, "A 10.4-ENOB 120MS/s SAR ADC with DAC Linearity Calibration in 90nm CMOS", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp 69-72, Nov-2013.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of the University of Macau

A 0.011mm² 60dB SNDR 100MS/s Reference Error Calibrated SAR ADC with 3pF Decoupling Capacitance for Reference Voltages

Chi-Hang Chan, Yan Zhu, Iok-Meng Ho, Wai-Hong Zhang, Chon-Lam Lio, Seng-Pan U, and Rui P. Martins

FEATURES

SAR reference error calibration
Low hardware overhead
~22 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a calibration scheme for reference error caused by signal dependent switching transient in a high speed SAR ADC. The scheme has a little hardware overhead, which is not dependent on the type of the input signal and is able to run in the background without interrupting the ADC's normal operation. The calibration along with the SAR ADC are implemented in a 65 nm CMOS and the measurement results show that the proposed scheme effectively improves the SNDR of an 11b SAR ADC by ~9 dB.

The calibration allows the placement of only 3 pF decoupling capacitance in the reference voltages. The prototype achieves 100 MS/s sampling rate with a total power consumption of 1.6 mW at a 1.2 V supply. Plus, it exhibits a 59.03 dB and 60.4 dB SNDR at Nyquist and low input frequency, respectively, yielding a Walden FoM@Nyquist of 21.9 fJ/conv.-step. The total core area is 0.011 mm2 which includes the decoupling capacitor.

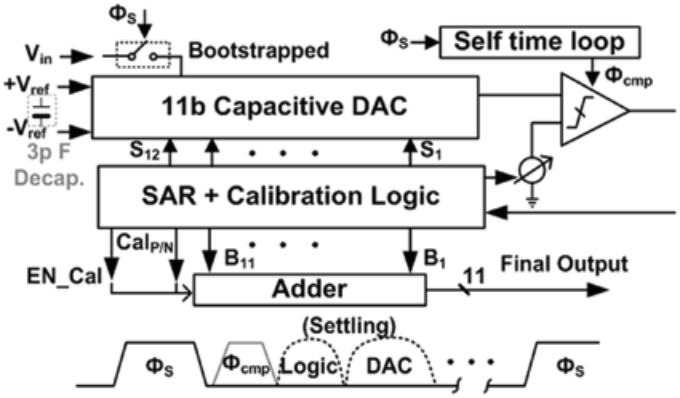


Fig. 1. ADC Architecture (actual implementation is in differential).

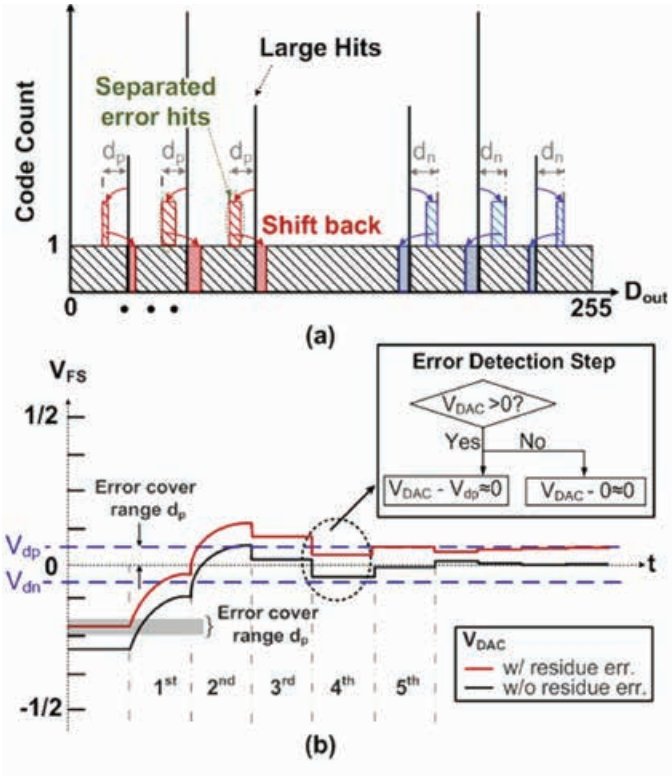


Fig. 2. (a) Code histogram of an 8b example with reference error. (b) Signal behavior of the DAC's output.

Publication(s):

[1] C.-H.g Chan, Y. Zhu, I.-M. Ho, W.i-H. Zhang, C.-L. Lio, S.-P. U, R. P. Martins, "0.011mm2 60dB SNDR 100MS/s Reference Error Calibrated SAR ADC with 3pF Decoupling Capacitance for Reference Voltages," in IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 145-148, Nov. 2016. Highlighted paper and invited to special issue of JSSC

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC

Jianwei Liu, Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Gain error calibration
Uniform Quantization based to simplified hardware
Calibration offchip
~30 fJ/conversion-step Walden FoM
Silicon verified in UMC 90nm CMOS

DESCRIPTION

This brief presents a uniform quantization theory (UQT)-based digital-to-analog converter (DAC) linearity calibration for a successive approximation register (SAR) analog-to-digital converter. According to the uniform quantization noise property, the nonlinearity due to the parasitics in an LSB array of the split-DAC structure is estimated and corrected in the digital domain. The calibration requires that the characteristic of the input signal must fulfill the prerogative of the quantization theory. The advantages lie in its low design complexity with no additional analog circuit modification. The proposed calibration is verified by both behavioral simulations and measured results in an SAR ADC. The measurements are based on a prototype implemented with large nonlinear split-DACs, which demonstrate that the UQT-base linearity calibration can effectively improve the Signal to Noise and Distortion (SNDR) from 56.9 to 63.3 dB at dc input with a sampling frequency of 120 MS/s.

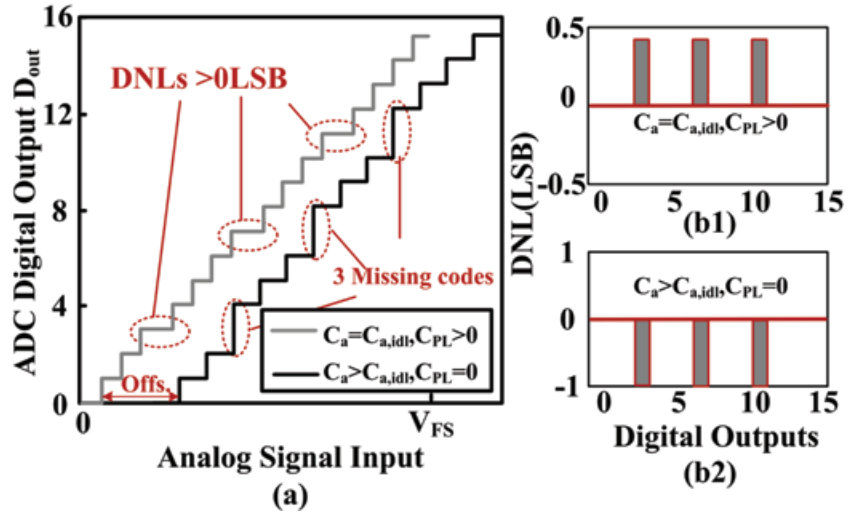


Fig. 1. (a) Output transfer characteristic of a 4-bit split-DAC. (b1) and (b2) Corresponding output code histogram of the 4-bit SAR ADC.

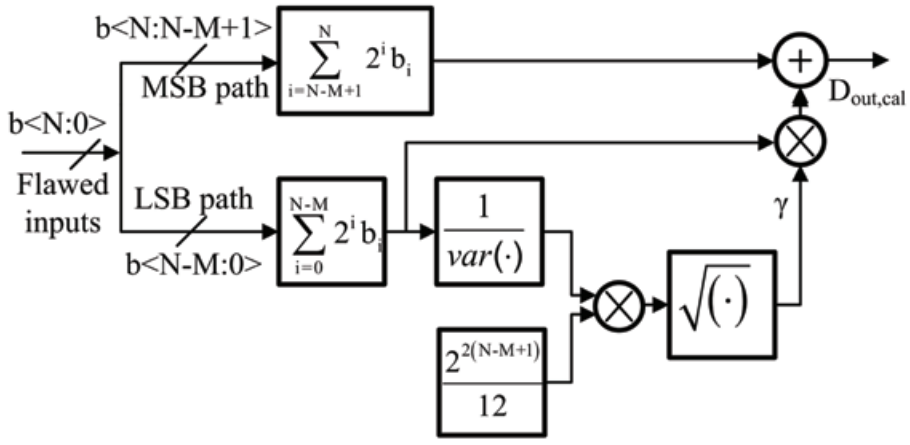


Fig. 2. Block diagram of the calibration based on UQT.

Publication(s):

[1] J. Liu, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Jan-2016.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 12b 180MS/s 0.068mm² With Full-Calibration-Integrated Pipelined-SAR ADC

Jianyu Zhong, Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Inter-stage gain calibration
Binary search calibration scheme to enhance completion time
Calibration on-cihp
Implement in a Pipeline SAR ADC
~37 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a 12b 180 MS/s 0.068 mm² 2× time-interleaved pipelined-SAR analog-to-digital converter (ADC) with gain and offset calibrations fully embedded on-chip. The proposed binary-search gain calibration (BSGC) technique corrects the inter-stage gain error caused by the open-loop residue amplifier. The BSGC, fully integrated into the second-stage SAR ADC, contributes to a compact area. We improve the noise performance by implementing a merged-residue-DAC operation in the first-stage ADC.

Also, we propose a dual-phase bootstrap technique to improve the sampling linearity in the partial interleaving architecture. The measurement results of the ADC prototype in 65 nm CMOS demonstrate the effectiveness of the proposed calibration through the enhancement of the signal to noise-and-distortion ratio from 51.5 to 60.9 dB at a Nyquist input, leading to a FoM@Nyq of 36.7 fJ/conversion-step.

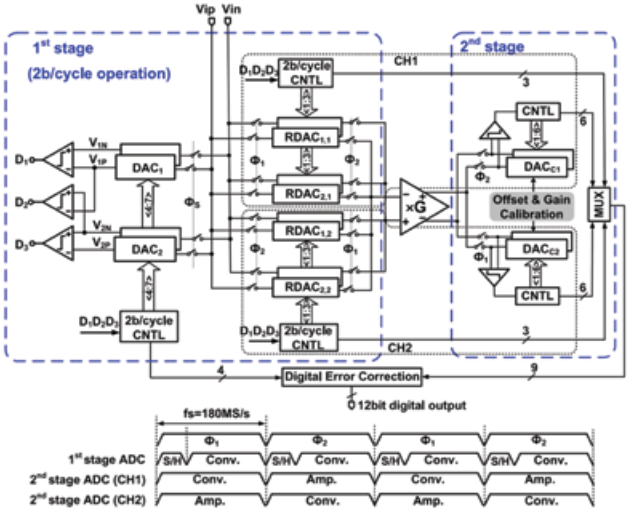


Fig. 1. PI Pipelined-SAR ADC architecture and timing diagram.

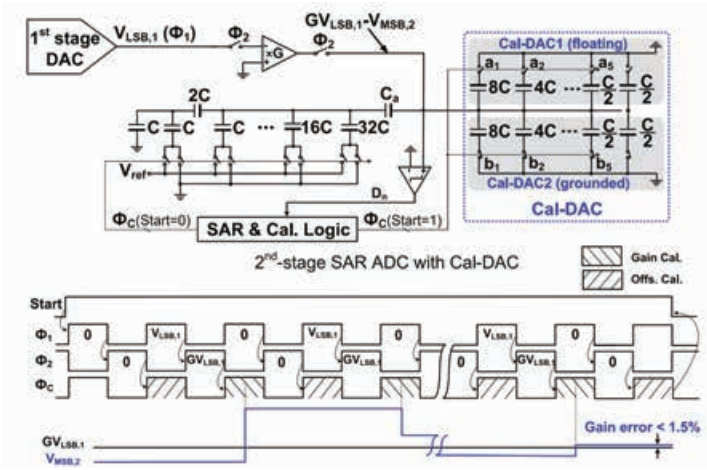


Fig. 2. Circuit implementation of the BSGC technique and its control timing diagram (Only Channel 1 shown).

Publication(s):

[1] J. Zhong, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 12b 180MS/s 0.068mm2 with Full-Calibration-Integrated Pipelined-SAR ADC", IEEE Transactions on Circuits and Systems I: Regular paper, Feb-2017

[2] J. Zhong, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 12b 180MS/s 0.068mm2 Pipelined-SAR ADC with Merged-residue DAC for Noise Reduction", IEEE European Solid-State Circuits Conference – ESSCIRC 2016, pp. 169-172, Sep-2016.

[3] J. Zhong, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 12b 180MS/s 0.068mm2 Full-Calibration Integrated Pipelined-SAR ADC", International Solid State Circuits Conference (ISSCC), Student Research Previews, Feb-2015

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of the University of Macau

RESEARCH ABSTRACTS
SUB-GHz to GHz ADCs

A 4.8-bit ENOB 5-bit 500MS/s Binary-Search ADC with Minimized Number of Comparators

Si-Seng Wong, U-Fat Chio, He-Gong Wei, Chi-Hang Chan, Hou-Lon Choi, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

High Speed Binary Search ADC
Reduced Comparators from 2N-1 to N
Low Power consumption 1.63mW
Very High Sampling Rate 500MS/s
5b Resolution, SNDR=30.7dB
Good Power efficiency, FoM_W=117fJ/step
Very Small Active Area, 0.015mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a topology to improve the system linearity and reduce the complexity of high-speed binary-search ADCs. The proposed topology, when compared with previous binary-search ADC architectures, further reduces the number of comparators from 2N-1 to N for N-bit precision, the comparator structure is simplified, and it can avoid both the signal dependent offsets and the kickback noise. The kickback noise injected to the current stage does not affect the output because the comparator has already quantized the output of the current stage during the kickback. The proposed binary-search ADC has been implemented in 65nm CMOS process and it consumes 1.63mW at an operation frequency of 500MS/s. The measurement results demonstrate that the binary-search ADC achieves 30.7dB SNDR (4.8-bit ENOB).

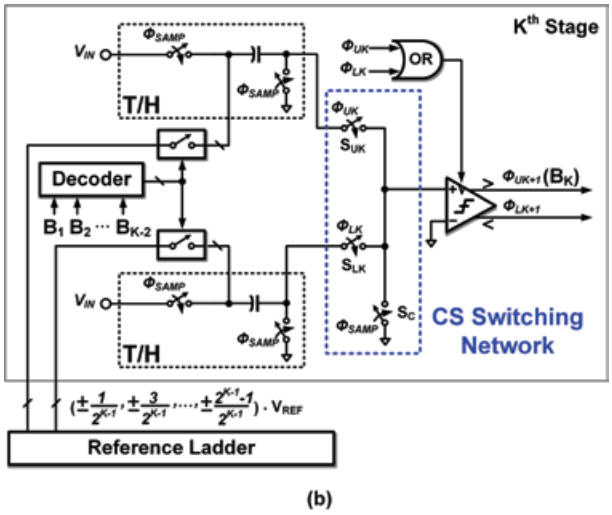


Fig. 1. Scheme of Kth stage of the proposed binary-search ADC.

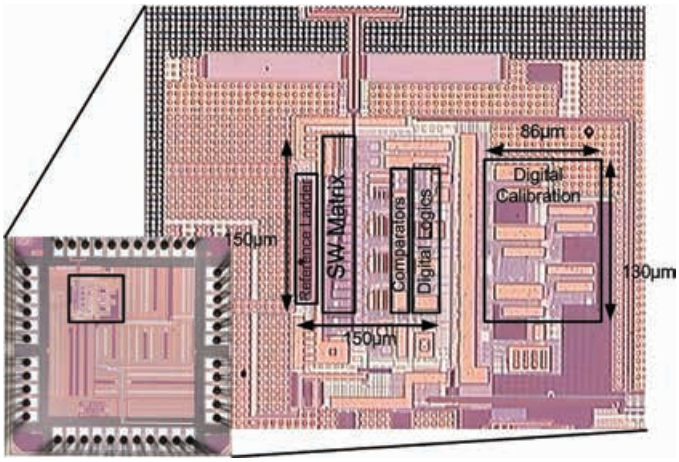


Fig. 2. Chip Photograph.

Publication(s):

[1] S.-S. Wong, U-F. Chio, C.-H. Chan, H.-L. Choi, S.-W. Sin, S.-P. U, R. P. Martins, "A 4.8-bit ENOB 5-bit 500MS/s Binary-Search ADC with Minimized Number of Comparators," in IEEE Asian Solid-State Circuit Conference – A-SSCC, pp. 73-76, Nov 2011.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

2b/cycle SAR ADC
VCM-based multi-bit switching
~34fJ/conversion-step walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

An 8b 1GS/s ADC is presented that interleaves two 2b/cycle SARs. To enhance speed and save power, the prototype utilizes segmentation switching and custom-designed DAC array with high density in a low parasitic layout structure. It operates at 1GS/s from 1V supply w/o interleaving calibration and consumes 3.8mW of power, exhibiting a FoM of 24fJ/conv. step. The ADC occupies an active area of 0.013mm2 in 65nm CMOS including on-chip offset calibration.

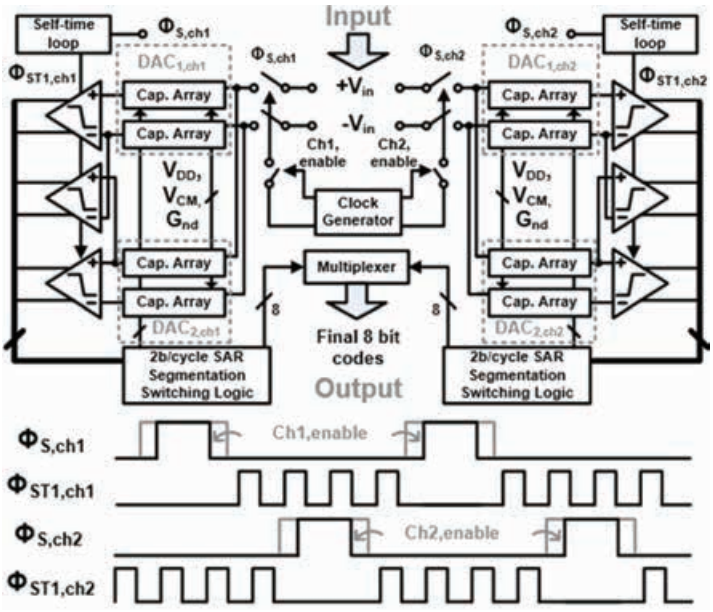


Fig. 1. Overall ADC architecture and its timing diagram.

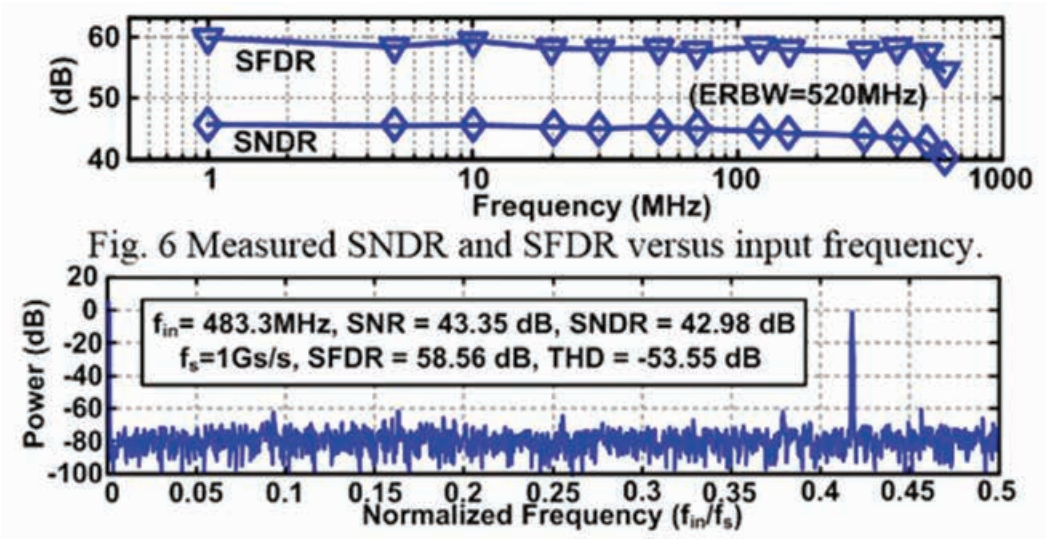


Fig. 2. Spectrum at 1GS/s and Nyquist input (decimated 125x).

Publication(s):

[1] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure," in IEEE Symposia on VLSI Technology and Circuit (VLSIC), pp. 86-87, Jun. 2012.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.024mm² 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65 nm CMOS

He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

2b/cycle SAR
On-Chip Digital Calibration
Low power consumption, 4mW
High Sampling Rate, 400MHz
Excellent Power efficiency, 73fJ/step
Very Small Active Area, 0.028mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This design is a power efficient ADC solution with up to 400MS/s conversion rate based on a (2b/Cycle) SAR topology that uses a resistive-based 2-bit DAC and several power/area reduction techniques, like interpolation in the sampling network, which reduces 33% of the hardware of the sampling circuit, DAC switches and digital decoder. Moreover, cascaded inverters in the decoder instead of the conventional AND/NAND gates saves by 2/3 the number of transistors leading to low-power performance and faster operation. Furthermore, a cross-coupled bootstrapping network alleviates the signal-dependent clock feed-through. The proposed SAR ADC achieves rapid conversion rate, low-power and compact area leading to SNDR of 44.5dB and SFDR of 54.0dB, at 400MS/s with 1.9MHz input. The measured FOM is 73fJ/conversion-step at 400MS/s from 1.2V supply and 42fJ/conversion-step at 250MS/s from 1V supply. The active area with the digital calibration is 0.028mm².

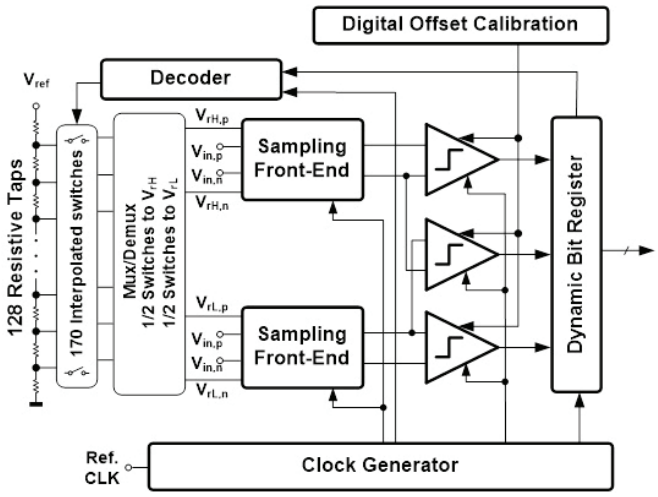


Fig. 1. ADC architecture.

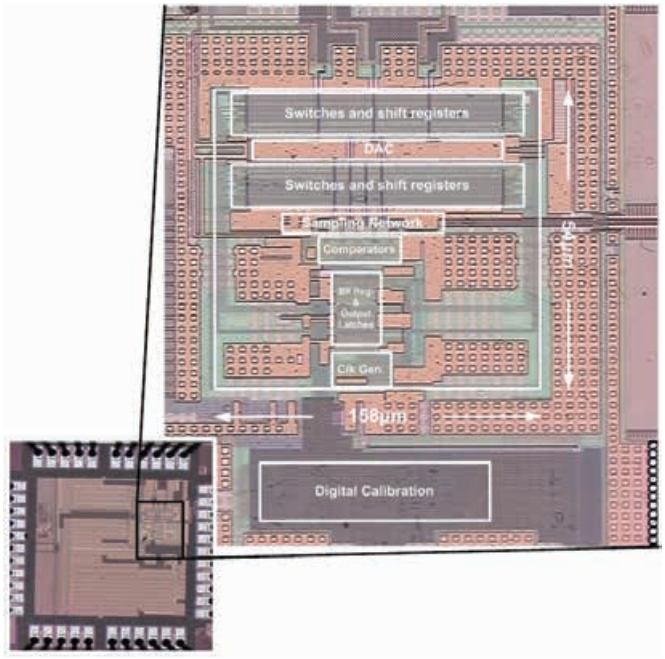


Fig. 2. Chip Photograph.

Publication(s):

[1] H.-G. Wei, C.-H. Chan, U-F. Chio, S.-W. Sin, S.-P. U, R. P. Martins, F. Maloberti, "A 8-bit 400MS/s 2-bit per cycle SAR ADC with Resistive DAC", IEEE Journal of Solid-State Circuits, vol. 47, Issue 11, pp. 2763-2772, Nov 2012.

[2] H.-G. Wei, C.-H. Chan, U-F. Chio, S.-W. Sin, S.-P. U, R. P. Martins, F. Maloberti,"A 0.024mm2 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65 nm CMOS," in IEEE International Solid-State Circuit Conference (ISSCC), vol. 54, pp.188-189, Feb 2011. (ISSCC Silk Road Award)

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC

Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Partial-Interleaving Architecture
Shared opamp in TI pipeline SAR
Offset calibration onchip
~30 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

A 10b 500MS/s ADC is presented that shares a full-speed SAR at front-end and interleaves the pipelined residue amplification with shared opamp and 2nd-stage SAR ADCs, which achieves high speed, low power and compact area.

The prototype ADC in 65nm CMOS achieves a mean SNDR of 55.4dB with 8.2mW power dissipation at 1.2V. The active die area including the offset calibrations is 0.046mm^2.

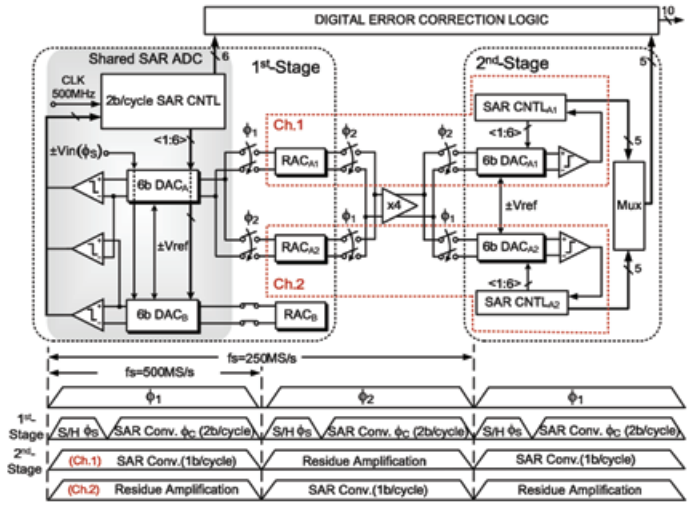


Fig. 1. Overall ADC architecture and its timing diagram.

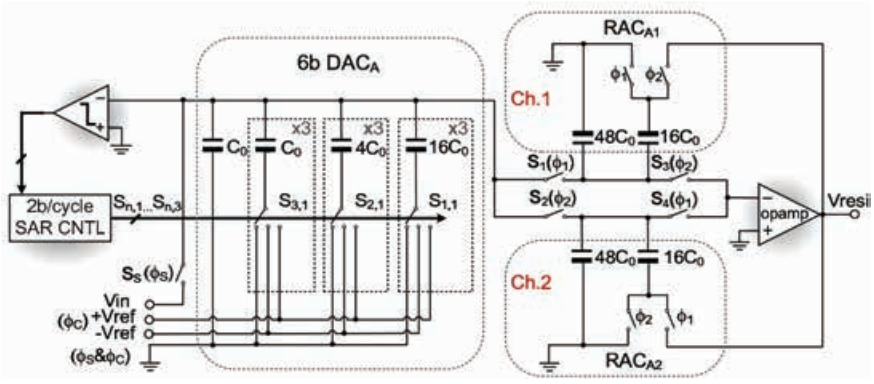


Fig. 2. 1st-stage 6b SAR ADC w/ Opamp-shared TI-Residue Amplification.

Publication(s):

[1] Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC", IEEE Symposium on VLSI Circuits, pp 90-91, Jun-2012.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Passive Folding
Embedded Reference
On-chip offset calibration
Gain calibration
~23 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a 5-bit 1.25-GS/s folding flash ADC. The prototype achieves a folding factor of four with a capacitive folding technique that only consumes dynamic power. Incorporated with various calibration schemes, folding errors and the comparator's threshold inaccuracies are corrected, thus allowing a low input capacitance of 80 fF. The design is fabricated using 65-nm digital CMOS technology and occupies 0.007 mm.

The maximum DNL and INL post calibration are 0.67 and 0.47 LSB, respectively. Measurement results show that the ADC can achieve 1.25 GS/s at 1-V supply with a total power consumption of 595 W. In addition, it exhibits a mean ENOB of 4.8b at dc among ten chips, which yields an FoM of 17 fJ/conversion-step.

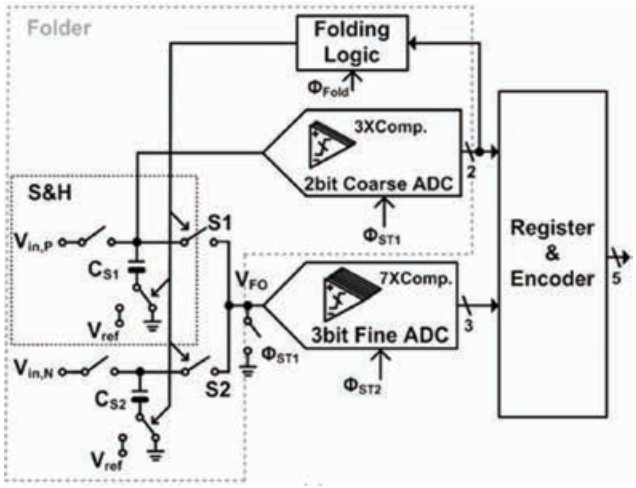


Fig. 1. ADC Architecture (actual implementation is in differential).

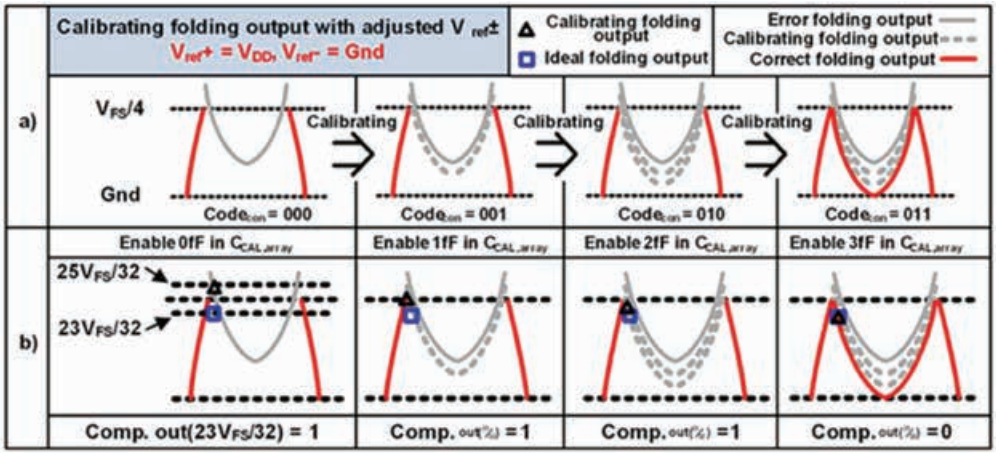


Fig. 2. Folding-reference calibration scheme and its signals behavior.

Publication(s):

[1] C.-H. Chan*, Y. Zhu*, S.-W. Sin*, S.-P. U*, R. P. Martins*, and F. Maloberti, "A 5b 1.25GS/s 4X Capacitive Folding Flash ADC in 65nm CMOS," IEEE Journal of Solid-State Circuits, vol. 48, no. 9, pp. 2154 -2169, Sep. 2013.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

An 11b 900 MS/s Time-Interleaved Sub-ranging Pipelined-SAR ADC

Yan Zhu, Chi Hang Chan, Seng-Pan U, and Rui P. Martins

FEATURES

Hybrid ADC architecture
Channel Selection Embedded boostrap to reduce clock skew effect
Calibration onchip
~56 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a sub-ranging 6-way time-interleaved pipelined-SAR ADC that achieves 900MS/s and 9.3 ENOB in 65nm CMOS. The architecture optimization is based on a pipelined-SAR structure that obtains high-speed with an optimized number of channels, thus leading to relaxed calibration with higher efficiency in power and area consumption.

The proposed channel-selection-embedded bootstrap performs sampling instants synchronization without additional components, thus effectively suppressing the spurs from time skews below -65 dBFS. The mismatch errors due to offset and gain are all solved on-chip, whose spurs are suppressed below -67 dBFS. The prototype achieves 66 dB SFDR and 51.5 dB SNDR with a Nyquist input exhibiting a FoM of 56 fJ/conv.step.

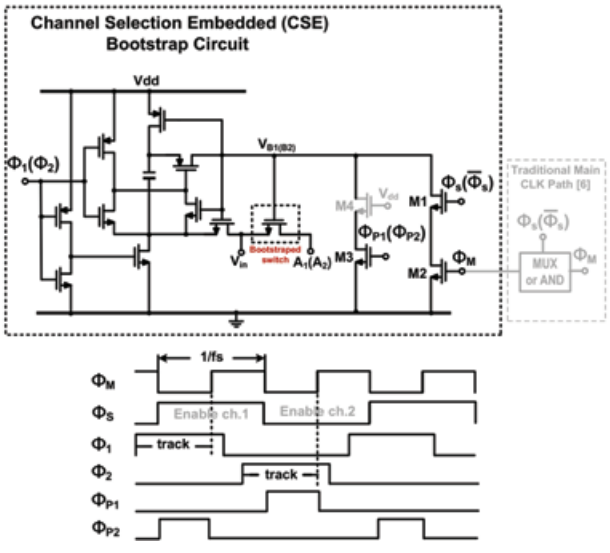


Fig. 1. Proposed Channel-Selection-Embedded bootstrap circuit and its control timing diagram.

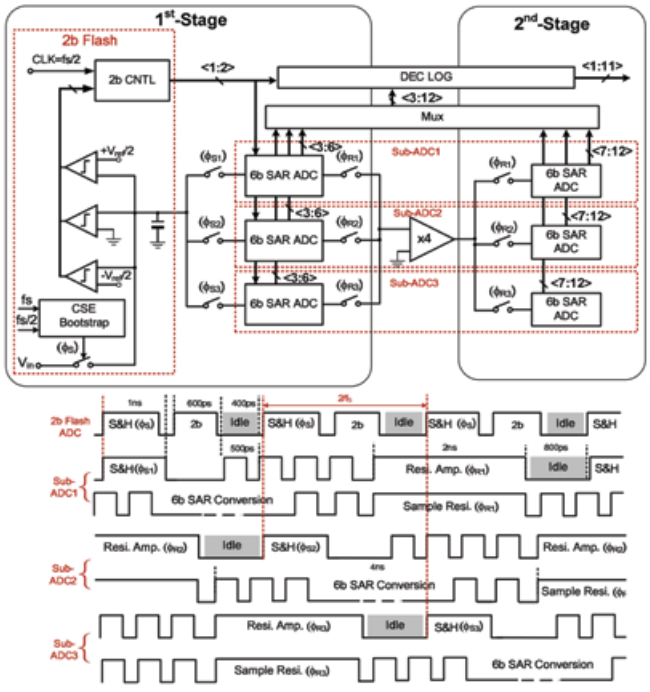


Fig. 2. Main channel ADC architecture and its timing diagram.

Publication(s):

[1] Y. Zhu, C. H. Chan, S.-P. U, and R. P. Martins, "An 11b 900 MS/s Time-Interleaved Sub-ranging Pipelined-SAR ADC", IEEE European Solid-State Circuit Conference – (ESSCIRC), pp.211-214, Sep-2014.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of the University of Macau

A 89fJ-FOM 6-bit 3.4GS/s Flash ADC with 4x Time-Domain Interpolation

Jianwei Liu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Time-based Flash-Subranging ADC
On-Chip Calibration
4x Time-Domain Interpolation Technique
Low power consumption, 12.6mW
Very High Sampling Rate, 3.4GS/s
Excellent Power efficiency, 89fJ/step
Very Small Active Area, 0.034mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 6-bit 3.4 GS/s flash ADC in 65 nm CMOS. The proposed 4x time-domain interpolation technique allow reducing reduction of the number of comparator from conventional 63 to 16 in a 6-bit flash ADC.

Without extra clocking and calibration in the interpolated stage, the proposed scheme effectively achieves 4x interpolation factor with simply SR-latches.

Offset calibration only applies in the comparators and is implemented on-chip. (how about the time-offsets?) Measurement results show that the prototype can achieve 3.4 GS/s with a total power consumption of 12.6 mW at 1 V supply. Besides, it exhibits a 34.219 dB SNDR at Nyquist, which yields a Walden FoM of 89 fJ/conversion-step.

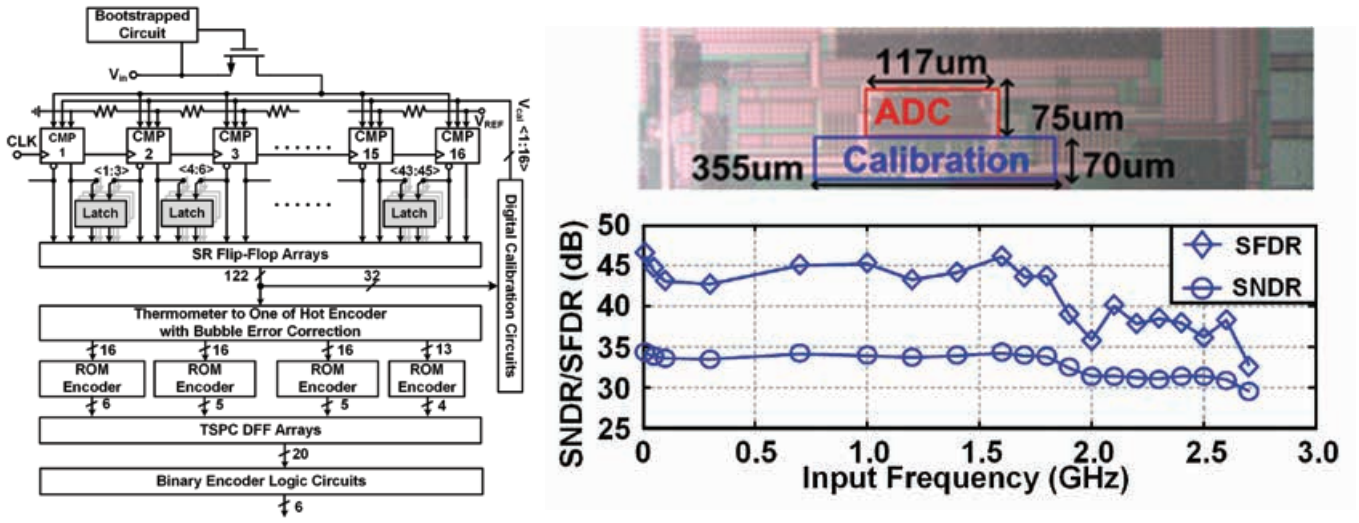


Fig. 1. The ADC architecture, the Chip Photograph and Dynamic Performance.

Publication(s):

[1] J. Liu, C.-H. Chan, S.-W. Sin, S.-P., U, R. P. Martins, " A 89fJ-FOM 6-bit 3.4GS/s flash ADC with 4x time-domain interpolation", in IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 1-4, Nov 2015.

[2] J. Liu, C.-H. Chan, S.-W. Sin, S.-P., U, R. P. Martins, " A 4x Time-Domain Interpolation 6-bit 3.4GS/s 12.6mW Flash ADC in 65nm CMOS", in Journal of Semiconductor Technology and Science, Vol. 16, No. 4, pp. 395-404, Aug 2016.

* Contributors with University of Macau

Sponsorship:

Research Committee of University of Macau.

An 8-bit 0.7-GS/s Single Channel Flash-SAR ADC in 65-nm CMOS Technology

Dante Gabriel Muratore, Alper Akdikmen, U-Fat Chio, Edoardo Bonizzoni, Sai-Weng Sin, Rui Paulo Martins, Franco Maloberti,

FEATURES

Single Channel Flash-SAR Subranging Scheme
Preamplifier with intepolated thresholds generation
Low power consumption, 6mW
High Sampling Rate, 700MS/s
Excellent Power efficiency, 87fJ/step
Very Small Active Area, 0.033mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents the prototype of a single channel 8-bit 0.7-GS/s A/D converter implemented in a 65-nm CMOS process. The result, comparable with the one obtained with smaller line-widths, benefits from an architecture made by the cascade of a 4-bit flash and a two-step SAR converter. Both steps determine 3-bit. The 4+3+3 bits give rise to the 8-bit output; the applied redundancy avoids calibration in the first two stages. The required thresholds are generated from the resistive interpolation embedded within the pre-amplifiers preceding the latches. The active area of the chip is 150 x 220 μm^2 and the total power consumption is 5.96 mW. At Nyquist, the ADC achieves 6.62 ENOB, resulting in a figure of merit equal to 86.7 fJ/conversion-step.

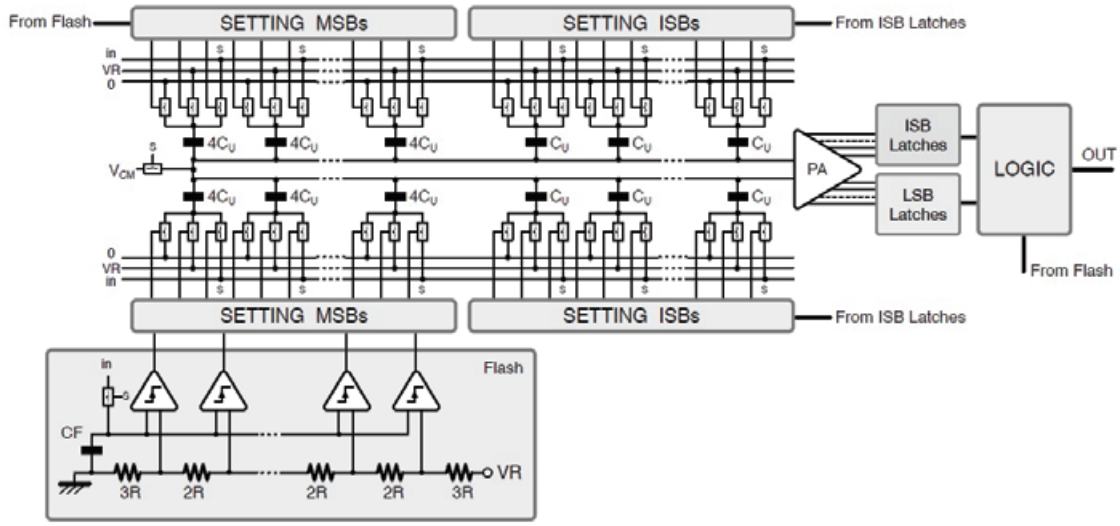


Fig. 1. ADC architecture

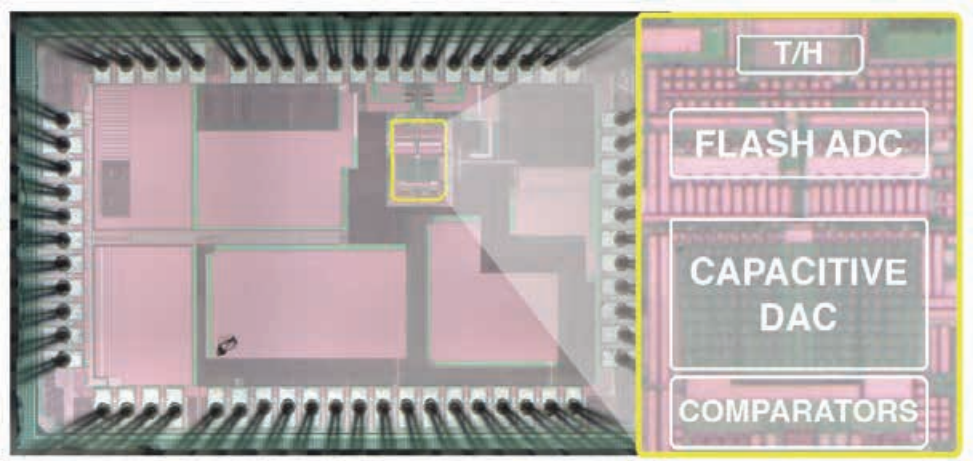


Fig. 2. Chip Photograph

Publication(s):

[1] 1. Dante Gabriel Muratore, Alper Akdikmen, U-Fat Chio*, Edoardo Bonizzoni, Sai-Weng Sin*, Rui Paulo Martins*, Franco Maloberti,"An 8-bit 0.7-GS/s Single Channel Flash-SAR ADC in 65-nm CMOS Technology ", in Proc. IEEE European Solid-State Circuits Conference – ESSCIRC 2016, pp. 421-424, Sept 2016.

* Contributors with University of Macau

Sponsorship:

Research Committee of University of Macau.

A 6-b 5GS/s 4-Interleaved 3b/cycle SAR ADC

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

3b/cycle SAR Architecture
VCM-less Switching
On-chip offset calibration
Boundary Detection Code Overriding
~39 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a 4x time-interleaved 6-bit 5 GS/s 3b/cycle SAR ADC. Hardware overhead induced by a 3b/cycle architecture is eased by an interpolation technique where around 1/3 of the hardware is saved. In addition, complicated switching controls are simplified with a proposed fractional DAC array switching scheme, thus reducing the design complexity and the hardware burden. A boundary detection code overriding is introduced to reduce error probability at the large error magnitude, by utilizing the extended time when the comparator is at reset and the DAC at settling.

The floorplan of the front-end is optimized for important interleaving clock distributions, and a master-clock-control bootstrapped-switch technique is adopted to suppress the timing skew effect among the channels. The unit capacitor has been designed to suit for the DAC structure which allows top-plate sharing in both directions, plus, the offset is calibrated on-chip with a clocking variable biasing transistor pair at the latch. Measurement results show that the prototype can achieve 5 GS/s with a total power consumption of 5.5 mW at 1 V supply in 65 nm CMOS technology. Besides, it exhibits a 30.76 dB SNDR and 43.12 dB SFDR at Nyquist, which yields a Walden FoM of 39 fJ/conversion-step.

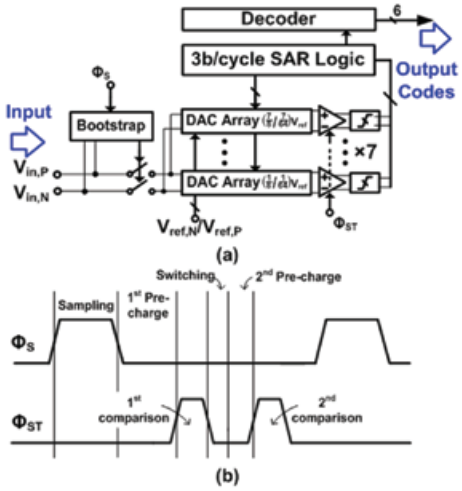


Fig. 1. The ADC (a) architecture and (b) timing diagram with time allocation.

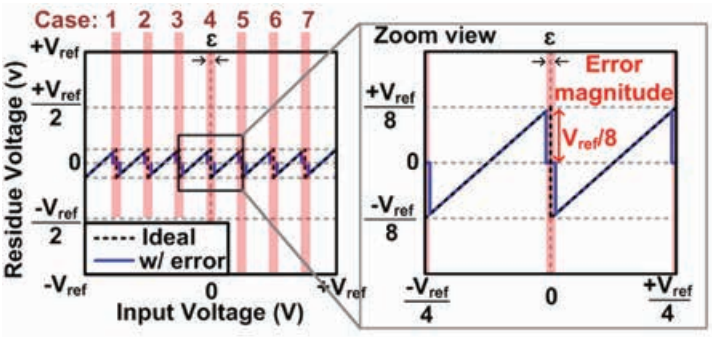


Fig. 2. Ideal and error (dot line) residue transfer curves of 6 bits 3b/cycle SAR with non-differential controls of the DACs in the red regions.

Publication(s):

[1] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 5.5mW 6-b 5GS/s 4-Interleaved 3b/cycle SAR ADC in 65nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 51, no. 2, pp. 365-377, Feb. 2016.

[2] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 5.5mW 6b 5GS/S 4×-interleaved 3b/cycle SAR ADC in 65nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), pp.1-3, Feb. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS

Yan Zhu, Chi Hang Chan, Seng-Pan U, and Rui P. Martins

FEATURES

Hybrid ADC Architecture
Flash + Pipeline SAR + Interleaving
Offset and gain calibration
~32 fJ/conversion-step Walden FoM
Silicon verified in GF 65nm CMOS

DESCRIPTION

This paper presents an 11 bit 450 MS/s three-way time-interleaved (TI) subranging pipelined-successive approximation register (SAR) analog-to-digital converter (ADC).

The proposed hybrid architecture combines the design benefits of different ADC structures to achieve a high conversion rate and accuracy with good power efficiency. The design employs multiple offset calibration schemes to compensate the offset mismatches at each stage.

The solutions require less calibration efforts, thus allowing the ADC to achieve a compact area. Furthermore, a dynamic SAR controller embedded with error-decision-correction (EDC) logic is proposed to reduce large transition error. Measurement results on a 65 nm CMOS prototype operated at 450 MS/s and 1.2 V supply show 7.4 mW total power consumption with a peak signal-to-noise distortion ratio (SNDR) of 60.8 dB and an FOM of 32 fJ/conv.step at Nyquist.

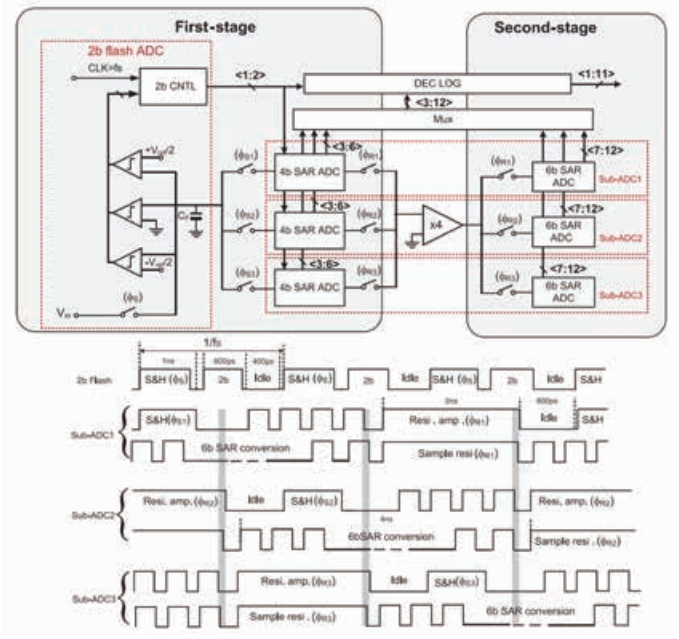


Fig. 1. Overall ADC architecture and its timing diagram.

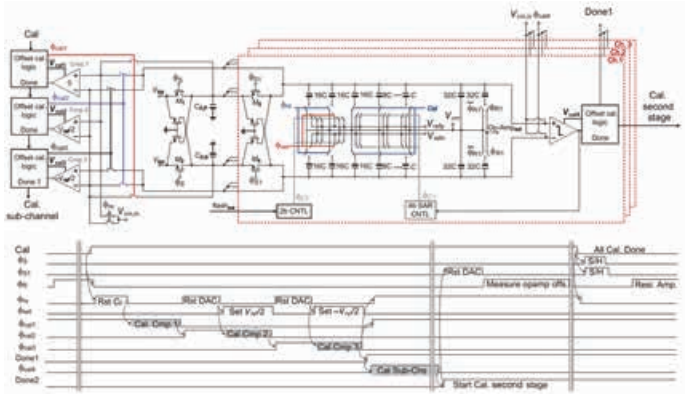


Fig. 2. Detailed circuit implementation of the first stage and offset calibrations for two stages together with its control timing diagram.

Publication(s):

[1] Y. Zhu, C. H. Chan, S.-P. U, R. P. Martins, "An 11b 450 MS/s three-way Time-Interleaved Sub-ranging Pipelined-SAR ADC in 65nm CMOS", IEEE Journal of Solid-State Circuits, Feb-2016.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial V_{cm}-Based Switching

Dezhi Xing, Yan Zhu, Chi Hang Chan, Sai Weng Sin, Fan Ye, Junyan Ren, Seng-Pan U, and Rui P. Martins

FEATURES

Partial Vcm-based switching
Low power and small common-mode variation
Offset calibration offchip
~48 fJ/conversion-step Walden FoM
Silicon verified in TSMC 65nm CMOS

DESCRIPTION

This brief presents a 7-bit 700-MS/s four-way time-interleaved successive approximation register (SAR) analog-to-digital converter (ADC). A partial V_{cm}-based switching method is proposed that requires less digital overhead from the SAR controller and achieves better conversion accuracy. Compared with switchback switching, the proposed method can further reduce the common mode variation by 50%. In addition, the impacts of such a reduction on the comparator offset, noise, and input parasitic are theoretically analyzed and verified by simulation.

The prototype fabricated in a 65-nm CMOS technology occupies an active area of 0.025 mm^2. The measurement results at the 700 MS/s sampling rate show that the ADC achieves signal-to-noise-and-distortion ratio of 40 dB at Nyquist input and consumes 2.72 mW from a 1.2 V supply, which results in a Walden FoM of 48 fJ/conversion step.

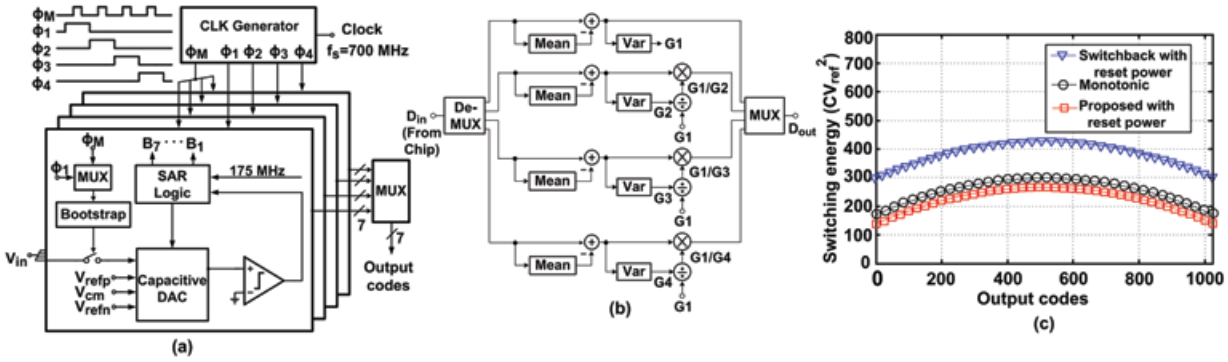


Fig. 1. (a) Overall ADC architecture. (b) Offset/gain mismatches calibration. (c) Switching energy versus output code of a 10-b SAR, including the reset power during sampling.

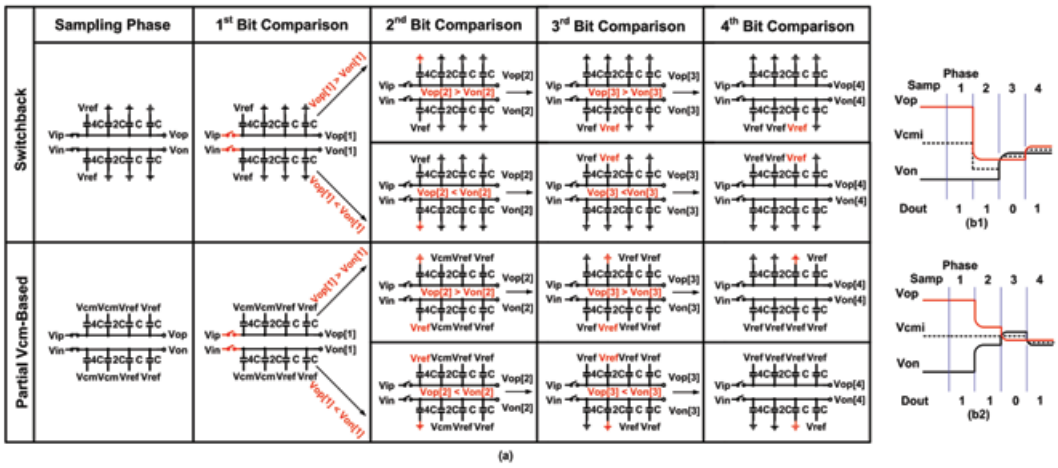


Fig. 2. (a) 4-b example of switchback and partial Vcm-based switching procedures. (b1) Comparator input common mode variation for switchback switching. (b2) Comparator input common mode variation for the proposed switching.

Publication(s):

[1] D. Xing*, Y. Zhu*, C. H. Chan*, S. W. Sin*, F. Ye, J. Ren, S.-P. U*, R. P. Martins*, "Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial Vcm-Based Switching", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Oct-2016.

* Contributors with University of Macau

Sponsorship:

National High-Tech Research and Development Program of China (863 Program), Research Committee of the University of Macau, Macau Science and Technology Development Fund

A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration

Chi-Hang Chan, Yan Zhu, Iok-Meng Ho, Wai-Hong Zhang, Seng-Pan U, and Rui P. Martins

FEATURES

1-then-2b operation
Merge Pre-charge Switching
Background offset calibration
Robust on PVT variation
~25 fJ/conversion-step Walden FoM
Silicon verified in GF 28nm CMOS

DESCRIPTION

This work features a 2x time-interleaved 7b 2.4GS/s 1-then-2b/cycle SAR ADC in 28nm. By quantizing 1b first followed by a 2b/cycle SAR and a dedicated arrangement of the SA control, the conventional pre-charging operation can be saved.

Offset among the comparators is calibrated in the background without requiring extra cycle or reference voltage. The design consumes 5mW with 40.05dB SNDR@Nyq., resulting in a Nyq.-FoM of 25.3fJ/conv.-step. SNDR@low stays >38dB with a wide range of V&T variation.

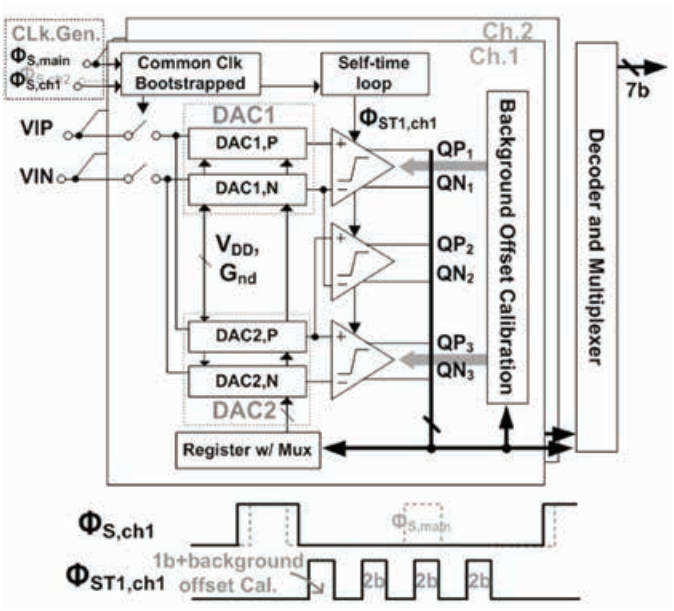
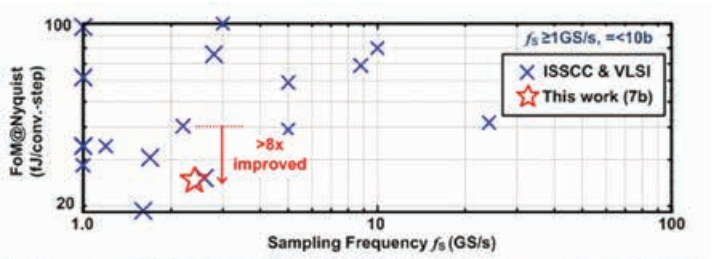


Fig. 1. Overall 2x interleaved 1-then-2bit/cycle SAR ADC architecture.



Publication	ISSCC'14 [5]	JSSC'15 [3]	ISSCC'13 [4]	This work	VLSI'16 [2]
Architecture	Folding Flash	2b/cycle SAR	SAR	2xTI 1-2b SAR	4xTI SAR*
Technology	40nm	45nm	32nmSOI	28nm	16nm
Supply (V)	1.1	1.25	1.0	0.9	0.95
Resolution	7b	7b	8b	7b	10b
f_S (GS/s)	2.2	1.0	1.2	2.4	1.6
SNDR@Nyq(dB)	37.4	40.8	39.3	40.05	50.3
Input Cap. (F)	300f	600f	128f	64f	N/A
Power (mW)	27.4	7.2	3.06	5.0	8.2
FoM@Nyq. (fJ/conv.-step)	205.7	80	34	25.3	19.23
DNL/INL	0.6/0.6	0.4/0.5	0.79/0.91	0.49/0.57	0.62/0.81
Area (mm^2)	0.052	0.016	0.0015	0.0043	0.023
Offset Cal.	No need	Foreground	Background	Background	Background

*Need Timing-skew calibration (offchip)

Fig. 2. Benchmark and table of comparison with the state-of-the-art ADCs.

Publication(s):

[1] C.-H. Chan, Y. Zhu, I. M. Ho, W.H. Zhang, S. P. U, and R. P. Martins, "A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration" IEEE International Solid-State Circuits Conference (ISSCC), pp. 282-283, Feb 2017.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 7.8mW 5b 5GS/s Dual-Edges-Triggered Time-Based Flash ADC

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Partial Vcm-based switching
Low power and small common-mode variation
Offset calibration offchip
~48 fJ/conversion-step Walden FoM
Silicon verified in TSMC 65nm CMOS

DESCRIPTION

This paper proposes a 5b 5 GS/s time-based flash ADC in 65 nm digital CMOS technology which utilizes both rising and falling edges of the clock for sampling and quantization. A dual-edge-triggered scheme reduces the dynamic power consumption of a voltage-to-time converter and the clock buffers by half.

We doubled both the reset and the available regeneration times by interleaving the time comparators. The ADC has a low input capacitance and the calibration circuit is included on-chip for suppressing various mismatches. The prototype running at 5 GS/s consumes 7.8 mW from a 1 V supply and achieves a SNDR of 26.19 dB at Nyquist. The resulting FoM is 94.6 fJ/conversion-step and the core area is only 0.004 mm2.

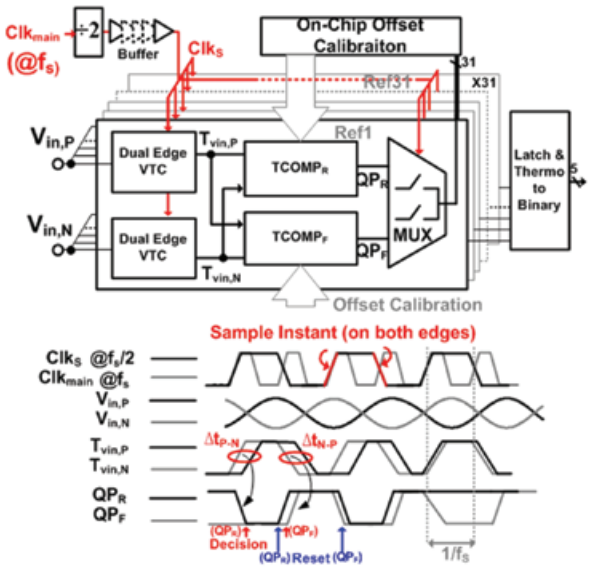


Fig. 1. Proposed ADC architecture and timing diagrams.

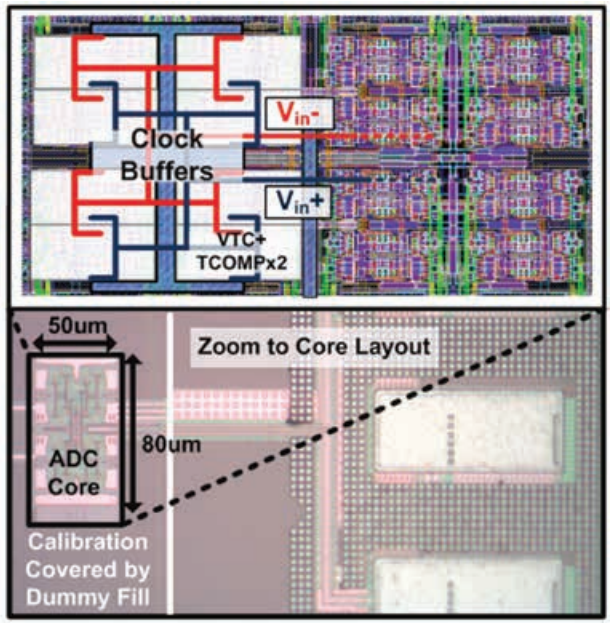


Fig. 2. Chip microphotograph and layout view.

Publication(s):

[1] C.-H. Chan*, Y. Zhu*, S.-W. Sin*, S. P. U*; R. P. Martins*, and F. Maloberti "A 7.8mW 5b 5GS/s Dual-Edges-Triggered Time-Based Flash ADC," IEEE Transactions on Circuits and Systems I: Regular paper, accepted, 2017.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Metastablility in SAR ADCs

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Boris Murmann, Seng-Pan U, and Rui P. Martins

FEATURES

Analysis metastability in SAR
Quantified the metastability error
Measurement result verification
Silicon verified in ST 65nm CMOS

DESCRIPTION

The fundamental limitation of Nyquist ADC architectures towards high speed is metastability. It refers to the inability of a latched comparator to produce a valid decision in a certain available time. This issue is usually severe in high-speed Successive-Approximation-Register (SAR) ADCs due to their serial conversion scheme, which includes the regeneration and the reset process of the comparator in a feedback loop, thus significantly reducing the available time for the regeneration. As the metastability phenomenon has already been explored and analyzed in Flash and Pipeline architectures, a SAR ADC is studied here.

Our analysis considers the probability of metastability errors as a function of their magnitude and is customized for a timer-based asynchronous SAR ADC (with loop time-out). The resulting framework can also quantify the metastability in a synchronous architecture and we provide a numerical comparison. To validate the analysis, measurement results of an 8-bit 130 MS/s SAR ADC in 90 nm CMOS are provided.

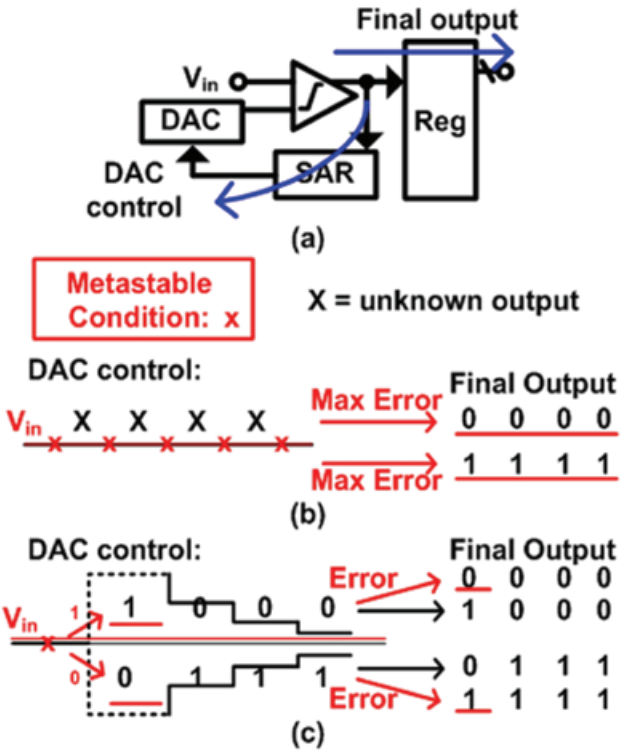


Fig. 1. (a) Conventional SAR block diagram (b,c) metastable error characteristics in the SAR ADC.

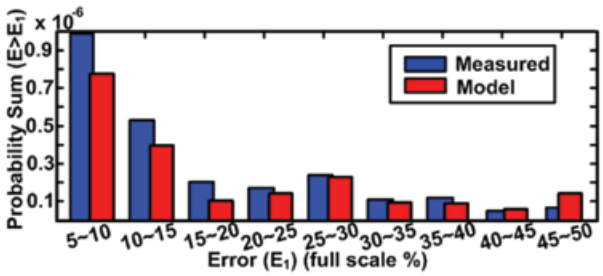


Fig. 2. Error rate versus error magnitude in histogram form with data grouped in 9 intervals.

Publication(s):

[1] C. H. Chan*, Y. Zhu*, S. W. Sin*, B. Murmann, S. P. U*, and R. P. Martins*, "Metastablility in SAR ADCs," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 2, pp. 111-115, Feb. 2017.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS
ANALOG AND MIXED-SIGNAL CIRCUITS

A Reconfigurable Low-Noise Dynamic Comparator with Offset Calibration in 90nm CMOS

Chi-Hang Chan, Yan Zhu, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Low noise dynamic comparator
Resolution is reconfigurable
On-chip offset calibration
Silicon verified in UMC 90nm CMOS

DESCRIPTION

This paper presents a reconfigurable, low offset, low noise and high speed dynamic clocked-comparator for medium to high resolution Analog to Digital Converters (ADCs). The proposed comparator reduces the input referred noise by half and shows a better output driving capability when compared with the previous work on state-of-the-art.

The offset, noise and power consumption can be controlled by a clock delay which allows simple reconfiguration. Moreover, the proposed offset calibration technique improves the offset voltage from 11.6mV to 533μV at 1 sigma. A prototype of the comparator is implemented in 90nm 1P8M CMOS with experimental results showing 320μV input referred noise at 1.5GHz with 1.2V supply.

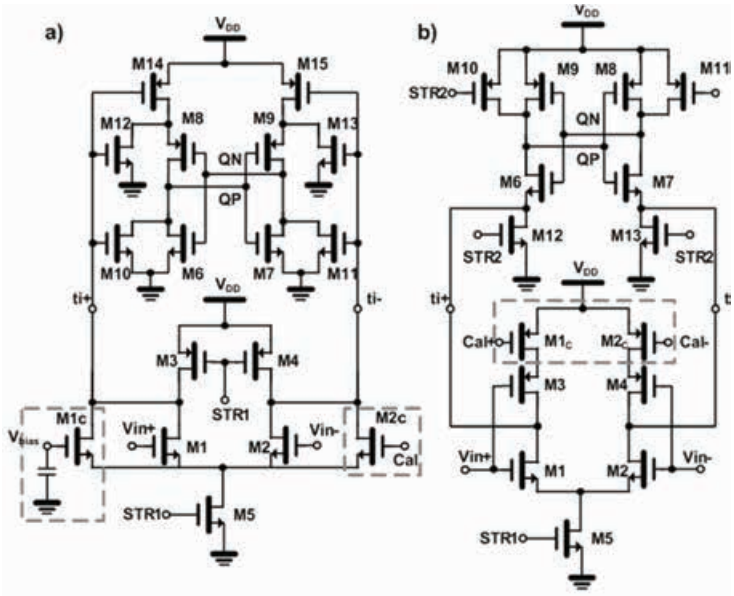


Fig. 1. Circuit schematic of two stage comparator with three times noise improved from conventional one (a) and the proposed comparators (b).

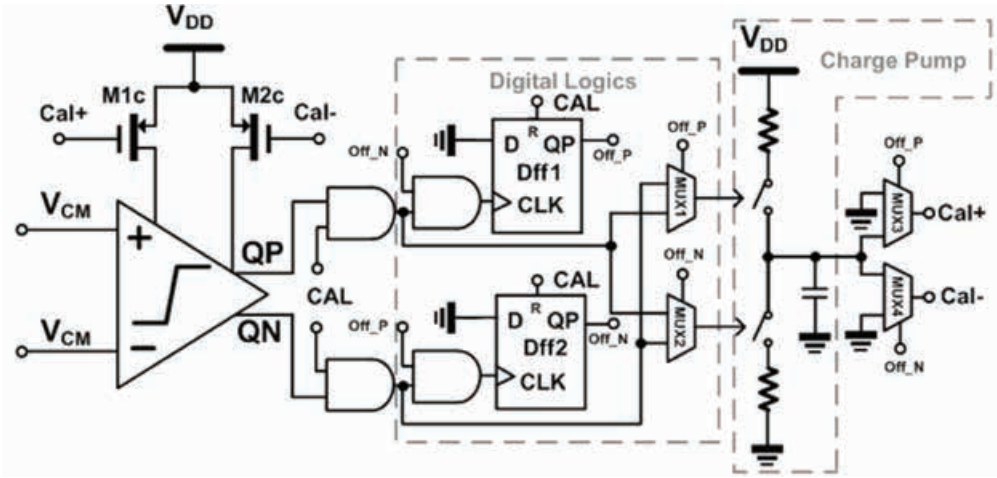


Fig. 2. Circuit schematic of the proposed offset calibration scheme.

Publication(s):

[1] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A reconfigurable low-noise dynamic comparator with offset calibration in 90nm CMOS" in IEEE Asia Solid-State-Circuit-Conference (A-SSCC), pp. 233-236, Nov.2011.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.016-mm² 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With > 0.95-MHz GBW

Zuzhu Yan, Pui-In Mak, Man-Kay Law, and Rui P. Martins

FEATURES

Wide loading range multi-stage amplifier
Current-buffer Miller compensation (CBMC) and parasitic-pole cancellation
Local feedback loop analysis
Silicon verified in standard 350nm bulk CMOS

DESCRIPTION

Most commercial buffer for LCD drivers require an external resistor (e.g., 20Ω for C_L=10 nF) in series with the output for ringing reduction. This regrettably penalizes the cost, settling time and high-frequency gain droop. This work describes a three-stage amplifier managed to afford particularly large and wide range of C_L with optimized power and die size. The control-centric Local Feedback Loop (LFL) Analysis enables effective analysis, comparison and design of three-stage amplifiers at the system level.

Fig. 1 shows the proposed scheme. The outer LFL is built upon CBMC, with the parasitic-pole cancelled by the LHP zero. The proposed active LHP zero circuit generates the desired LHP zero without introducing unwanted low-frequency poles. G_{mb2} offers V-to-I conversion for driving G_{mL} as well as isolation between V_2 and V_3 nodes. This resolve the problem of degraded owing to the passive LHP zero circuit.

Fig. 2 shows the schematic of the proposed three-stage amplifier. G_{m1} ($M_{1\text{-}10}$) is a folded cascode structure featuring a PMOS input differential pair ($M_{1\text{-}2}$). The active LHP zero circuit is embodied in G_{m2} ($M_{11\text{-}14}$) to enhance the power efficiency. G_{mL} (M_{15}) is combined with G_{mf} (M_{16}) to form a push-pull structure. The chip prototype is fabricated in standard 0.35-μm CMOS. Measured AC responses shows that C_L can be as large as 15 nF with 18.1-dB gain and 52.3° phase margins, and as small as 1 nF with 9.8-dB gain and 83.2° phase margins. The extrapolated DC gain is >100 dB. The GBW is 0.95 MHz at 15-nF C_L.

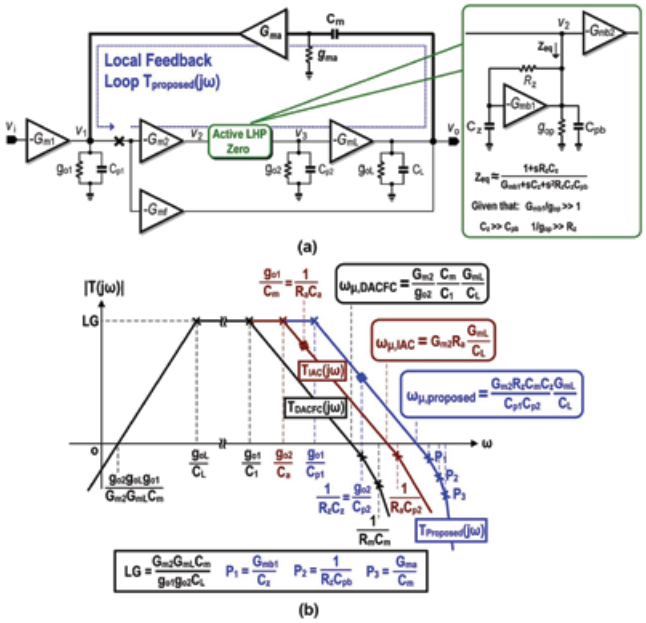


Fig. 1. Proposed scheme using CBMC plus parasitic-pole cancellation, and its (b) LFL bode plot.

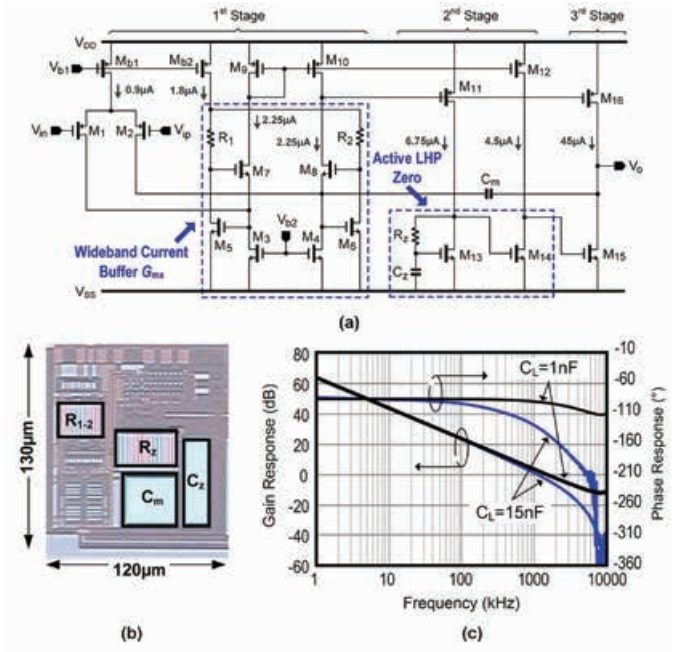


Fig. 2. Schematic of the proposed amplifier (top) and chip photo and measured AC response (bottom).

Publication(s):

[1] Z. Yan, P.-I. Mak, M.-K. Law and R. P. Martins, "A 0.016mm² 144μW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load With >0.95MHz GBW," IEEE Int. Solid-State Circuit Conference (ISSCC), pp. 366-367, Feb. 2012.

[2] Z. Yan, P.-I. Mak, M.-K. Law and R. P. Martins, "A 0.016-mm² 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With > 0.95-MHz GBW," IEEE Journal of Solid-State Circuits, vol. 48, no. 2, pp. 527-540, Feb. 2013.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Nested-Current-Mirror Rail-to-Rail-Output Single-Stage Amplifier With Enhancements of DC Gain, GBW and Slew Rate

Zushu Yan, Pui-In Mak, Man-Kay Law, Rui P. Martins, and Franco Maloberti

FEATURES

Nested-current-mirror (NCM) single-stage amplifier
Improved area and power efficiencies
Improved DC gain, gain-bandwidth product (GBW) and slew rate (SR)
Rail-to-rail output
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

Column drivers for display applications exhibit extremely tight area and power budgets to meet the market pressure on cost and display quality. Plus, due to the fabrication spread and scale alternative of the panels, the buffer amplifiers should master a wide range of capacitive load (C_L) up to tens of nF, while securing adequately large DC gain (e.g., >66 dB for 10 bit resolution) and output swing.

This paper introduces a nested-current-mirror (NCM) single-stage amplifier that can alleviate the tight performance trade-offs in conventional single-stage amplifier topologies, including the fundamental DP amplifier. The prototyped 3-step and 4-step NCM amplifiers achieve favorable performances with respect to the standard DP amplifier, and are comparable with the state-of-the-art of three-stage amplifiers.

The description of the NCM technique consists of two steps (Fig. 1). The first step is to split the DP transistor of the current-mirror amplifier into N sub-transistors M_1 to M_N, and alternately connect their inputs with V_n and V_p. Next, the outputs of M_1 to M_N are combined in sequence via the NCM formed by subdividing a current mirror into pieces with different ratios, which concurrently increases the effective transconductance and output resistance beyond those of the DP, and other single-stage amplifiers. The schematic of a 3-step NCM amplifier is also shown in Fig. 1. The DP transistors are split into M_1-M_3. Their outputs are summed via the NCM mirrors realized by M_4-M_9. M_{10} collects the output of the left, to form the single-ended output together with M_9.

Fig. 2 shows the chip micrograph of the 3-step (top) and 4-step NCM (bottom) and their measured AC responses at C_L=0.15 and 15 nF, showing much improved performance when compared with DP amplifiers, while preserving a rail-to-rail output swing, and wide drivability without entailing any compensation capacitor or resistor.

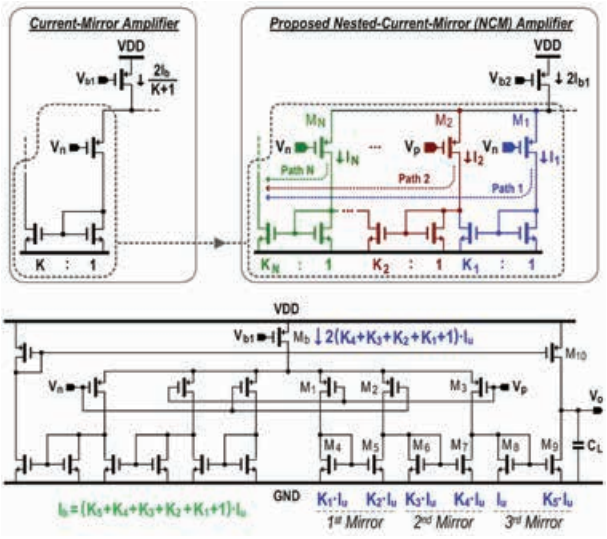


Fig. 1. Development of the NCM amplifier (top) and schematic of the 3-step NCM amplifier (bottom).

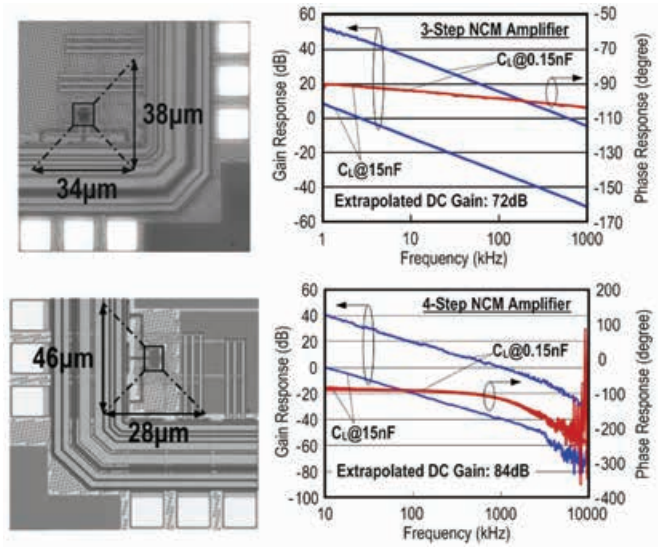


Fig. 2. Chip photo and the measured AC responses for 3-step NCM (top) and 4-step NCM (bottom).

Publication(s):

[1] Z. Yan, P.-I. Mak, M.-K. Law, R. P. Martins, and F. Maloberti, "Nested-Current-Mirror Rail-to-Rail-Output Single-Stage Amplifier with Enhancements of DC Gain, GBW and Slew Rate," IEEE J. of Solid-State Circuits, vol. 50, no. 10, pp. 2353-2366, Oct. 2015.

[2] Z. Yan, P.-I. Mak, M.-K. Law, R. P. Martins, and F. Maloberti, "A 0.0013mm² 3.6μW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Loads with >62° Phase Margin", IEEE Int. Solid-State Circuit Conference (ISSCC), pp. 288 - 289, Feb. 2014.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Precision CMOS Voltage Reference Exploiting Silicon Bandgap Narrowing Effect

Bo Wang, Man-Kay Law, and Amine Bermak

FEATURES

Silicon bandgap narrowing effect for BJT curvature reduction and residual curvature correction
Reduced temperature coefficient after batch trimming
Micropower consumption, 4.3 µA at 25 °C
Excellent Line sensitivity, 0.03%/V
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

To avoid dissipating power driving the curvature correction circuits, this work presents a BGR that only exploits the temperature characteristics of the BJT itself to reduce the $V_{be}(T)$ curvature and to perform residual curvature correction. As the silicon impurity doping concentration becomes particularly high (>10^{18} cm^{-3}), the silicon bandgap narrowing (BGN) occurs. For BJT, due to the BGN induced by the silicon lattice deformation in the heavily doped emitter, its forward current gain becomes strongly temperature dependent. This characteristic is utilized to achieve high precision voltage reference.

The proposed BGR topology with curvature reduction is shown in Fig. 1. A shunt-feedback loop, consisting of an amplifier A_1 and a pass transistor M_{p0}, regulates the voltage across R_{pt}. The input pair of A_1 consists of two matched vertical transistors $Q_{1,2}$ having an emitter ratio of 1:p under the same collector bias. Therefore, A_1 has a PTAT offset voltage $V_{pt}(T)$. $I_{pt}(T)$ mainly serves as Q_0's base bias and the results in curvature in $V_{be0}(T)$.$R_{c1,2}$ are used to amplify $V_{pt}(T)$, thereby compensating the first-order TC of $V_{be0}(T)$. After curvature reduction, the residual can still be large and further correction is preferred. In this work, three X_{TB}-related nonlinear signals can be used to linearize $V_{be0}(T)$, including Q_0's collector current I_{c0}, and the base currents $I_{b1,2}$ of $Q_{1,2}$, if their collector currents are PTAT.

Fig. 2 shows the micrograph of the prototype BGR, which occupies an area of 0.05 mm^2. The 3σ spread of the untrimmed V_{REF} is ±1.06% from −55 to 125 °C with an averaged TC of 36.5 ppm/°C. After batch trimming of R_{c1} at 25 °C for all 12 samples, the resultant spread is reduced to ±0.22%.

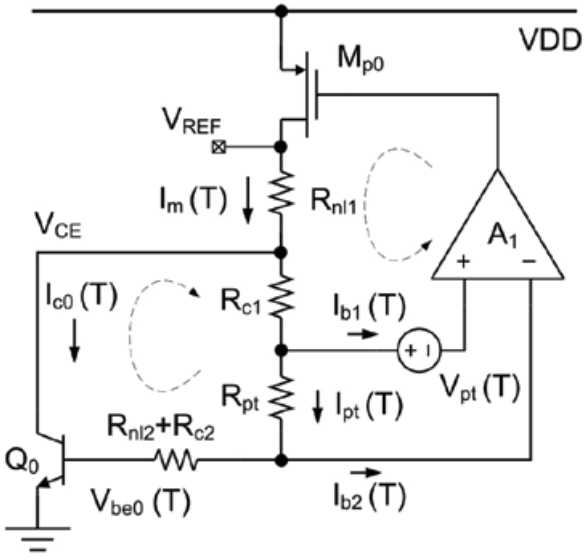


Fig. 1. Proposed BGR topology with curvature reduction and residual curvature correction utilizing the temperature dependency of BGN effect.

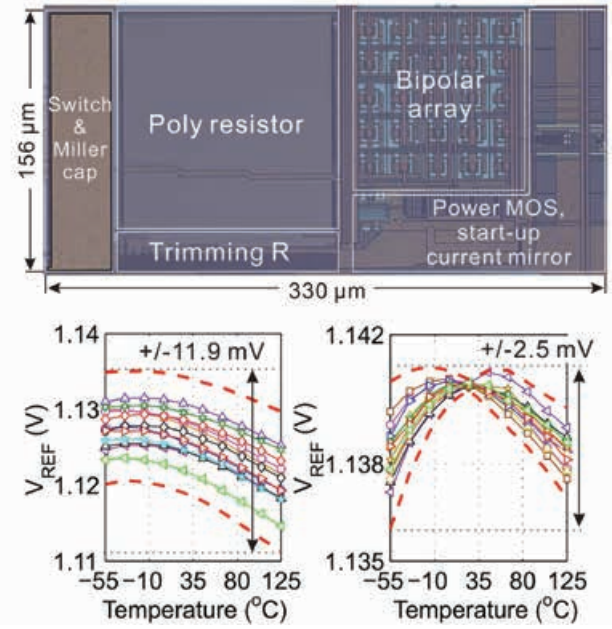


Fig. 2. Chip micrograph (top). Inaccuracy of V_{REF} from 12 samples without trimming (bottom left) and after batch trimming R_{c1} at 25 °C (bottom right).

Publication(s):

[1] B. Wang, M.-K. Law*, and A. Bermak, "A Precision CMOS Voltage Reference Exploiting Silicon Bandgap Narrowing Effect," IEEE Trans. on Electron Device, vol. 62, no. 7, pp. 2128-2135, Jul. 2015.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong Innovation and Technology Fund

BJT Process Spread Compensation Utilizing Base Recombination Current in Standard CMOS

Bo Wang, Man-Kay Law, and Amine Bermak

FEATURES

Minimize BJT inter-/intra-die spread and PTAT drift
Base recombination current for both process and temperature compensation
Standard deviation < 1.8 mV without trimming (30 dies in 2 batches)
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

The designing of a precision Bandgap Reference (BGR) with a temperature coefficient (TC) of 30 ppm/°C over a wide operating temperature is a non-trivial task due to the various error sources introduced during silicon fabrication. BGR error sources such as the amplifier offset, device mismatch and BJT base-emitter voltage (V_{be}) curvature can be mitigated by using circuit techniques like chopping, dynamic element matching and signal linearization. The PTAT drift in V_{be} introduced by BJT spreads (mainly due to the saturation current) ultimately limits the untrimmed BGR precision. This work presents a compensation topology which can minimize the V_{be} spreads of BJTs under different process conditions. This scheme only exploits the electrical properties of a standard BJT and no special process steps are required.

A BJT operating in its deep-saturation region (with tens of mV collector-emitter voltage V_{ce}) is exploited for I_s spread compensation. Under this condition, the electrons are trapped in the base region and strong electron-hole recombination occurs. It can be proved that a strong correlation exists between the recombination current I_r and I_s. As a result, the BJT process spread from I_s can be effectively compensated by injecting an I_r-dependent current into the collector of a BJT. Fig. 1(a) shows the schematic of the proposed BJT spread compensation circuitry, including the start-up block, the bandgap core and the bias/pseudo-supply generator. This design is fabricated in a standard 0.18-µm CMOS process, as shown in Fig. 1(b). The V_{be} STD of 15 standalone BJTs measures 3.24 mV at 25 °C using an external bias current. The compensated V_b (Fig. 1(a) from two batches with on-chip biasing measures only 1.8 mV at 25 °C, as shown in Fig. 1(c). This corresponds to a twofold reduction compared with that without compensation.

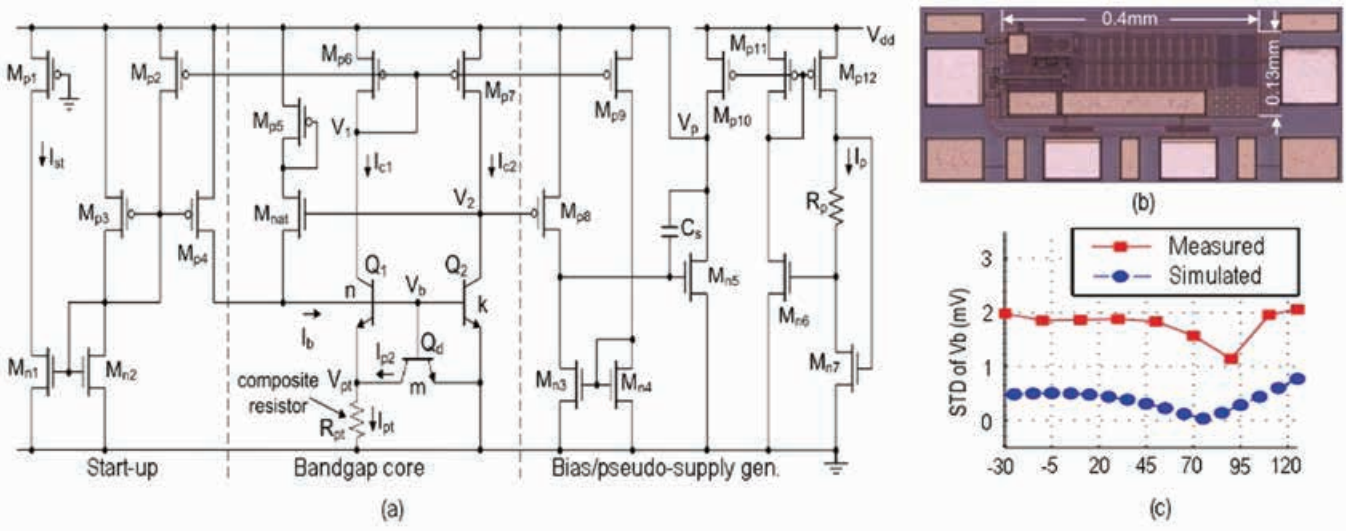


Fig. 1. (a) Schematic of the proposed BJT spread compensation circuitry. (b) Chip micrograph. (c) Measured/Simulated STD of the compensated V_b at different temepratures.

Publication(s):

[1] B. Wang, M.-K. Law*, and A. Bermak, "BJT Process Spread Compensation Utilizing Base Recombination Current in Standard CMOS," IEEE Electron Device Lett., vol. 36, no. 11, Nov. 2015.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong Innovation and Technology Fund

A 2 μW 45 nV/√Hz Readout Frontend With Multiple Chopping Active-High-Pass Ripple Reduction Loop and Pseudo-Feedback DC Servo Loop

Jiangchao Wu, Man-Kay Law, Pui-In Mak, and Rui P. Martins

FEATURES

Active-high-pass filter for filtering capacitor size reduction
Multiple-chopping for residue noise suppression
Pseudo-feedback DSL amplifier with 14nA current bias
Noise-efficiency-factor of 2.9
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

This work presents a fully integrated low noise chopper-stabilized CCIA with optimized power and area for neural recording applications. Fig. 1(a) presents the proposed neural recording frontend. A single-stage folded-cascode amplifier (G_{m1}) with internal chopping is utilized to achieve low power consumption without loading the amplifier output. The ripple reduction loop (RRL) employs an active high-pass filter composed of a gain stage G_{m2} and a buffer B_2 to further reduce the residual noise from the output and relax the value of C_3. The RRL output is fed back to the main amplifier internally instead of to the main amplifier output to increase the RRL loop gain. Reusing the current of G_{m1} can reduce the overall power consumption while avoiding additional poles that can degrade the system stability.

Multiple chopping is proposed to modulate the RRL offsets to high frequency and to suppress the output ripple. V_{OS2} and V_{OS3} are modulated by using a high chopping frequency f_{high}. As a result, V_{OS2} is modulated to f_{chop} at the input of G_{m3}, with additional high frequency images suppressed by C_3.

The remaining offsets (V_{OS3} at DC and V_{OS2} at f_{chop}) are then up-modulated by f_{high}, with the high order harmonics further filtered by C_3 and C_L. An ultra-low bandwidth pseudo-feedback buffer B_3 is inserted before G_{m4} to achieve a sub-Hz high-pass corner with reduced loading capacitance while dissipating only 14 nA using only a 15 pF on-chip capacitor. Instead of using a large loading capacitor to reduce the DSL induced IRN, the DSL output is fed back to the internal node of the main amplifier that can simultaneously reduce the IRN and the loading capacitor requirement.

The complete neural acquisition frontend was implemented in a standard 0.18 μm CMOS technology. The gain is designed to be approximately 34 dB with a chopping frequency of 20 kHz. This work achieves the smallest RRL + main amplifier (C_{RRL}+ C_L) and DSL (C_{DSL}) filtering/loading capacitance while preserving low IRN. The reduced power consumption by the RRL current reuse and the DSL pseudo-feedback amplifier with internal feedback leads to a NEF of 2.9.

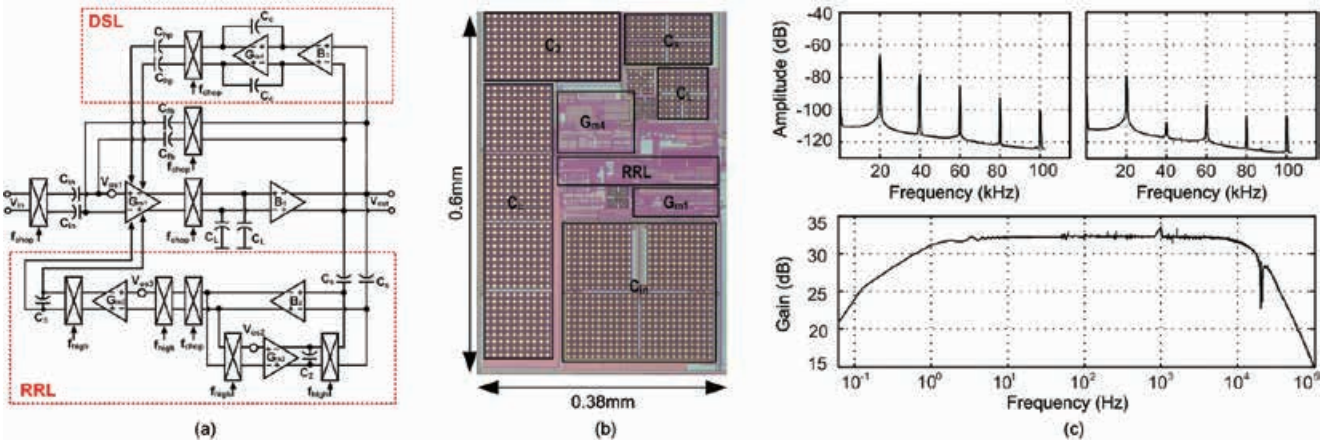


Fig. 1. (a) The proposed chopper-stabilized CCIA topology. (b) Chip photograph. (c) Measured output spectrum and transient waveform of the CCIA with f_{chop}=20 kHz and f_{high}=20 kHz (top left), f_{chop}=20 kHz and f_{high}=80 kHz (top right), and measured frequency response of the complete CCIA (bottom).

Publication(s):

[1] J. Wu, M.-K. Law, P.-I. Mak and R. P. Martins, "A 2 μW 45 nV/√Hz Readout Frontend With Multiple Chopping Active-High-Pass Ripple Reduction Loop and Pseudo-Feedback DC Servo Loop," IEEE Trans. on Circuits Syst. II, Exp. Briefs, vo. 63, no. 4, pp. 351-355, Apr. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong Innovation and Technology Fund

RESEARCH ABSTRACTS
BIOMEDICAL ELECTRONIC DEVICES

15-nW Biopotential LPFs in 0.35-μm CMOS Using Subthreshold-Source-Follower Biquads with and without Gain Compensation

Tan-Tan Zhang, Pui-In Mak, Mang-I Vai, Peng-Un Mak, Man-Kay Law, Sio-Hang Pun, Feng Wan, and Rui P. Martins

FEATURES

Subthreshold-source-follower (SSF) Biquads
Improved noise and nonlinearity performance
Simple filter order extension by cascading
Low input-referred noise, < 36 μVrms
Silicon verified in standard 350nm bulk CMOS

DESCRIPTION

Extremely-low-power analog circuits continue to play a key role in wearable or implantable devices to achieve maximum system lifetime. However, existing biopotential acquisition systems still consume power in the range of tens to hundreds of μW.

This work focuses on the nW-class lowpass filter (LPF) in biopotential acquisition systems. The proposed SSF Biquad consists of four MOSFETs, two current sources and two floating capacitors, with no common-mode feedback (CMFB) required. A positive feedback loop exists to realize a complex pole and sharpen the stopband attenuation. At ultra-low frequency, the nonlinearity arising from the body-effect is pronounced, and the distortion is reduced with a higher DC level. When the frequency increases, the frequency-dependent effect becomes more pronounced as more AC current passes through the capacitive load.

The frequency-dependent distortion can be optimized by choosing a ~1:2 ratio for the source and drain capacitors. To solve the gain-loss due to the body effect, a gain-compensated (GC) scheme constructed by an extra cross-connected differential pair for extra gain is proposed. It can be demonstrated that the linearity is frequency dependent, and harmonic cancellation is possible by optimizing the bias current.

Two 4th-order 100-Hz-bandwidth LPFs using Butterworth approximation were designed. Replace this line with your descriptions. The first design is a non-GC NMOS-based SSF Biquad followed by a PMOS one (Fig. 1). The second design is a GC NMOS-based SSF Biquad followed by a PMOS one (Fig. 2). The measured and simulated gain performances of both LPFs are also shown.

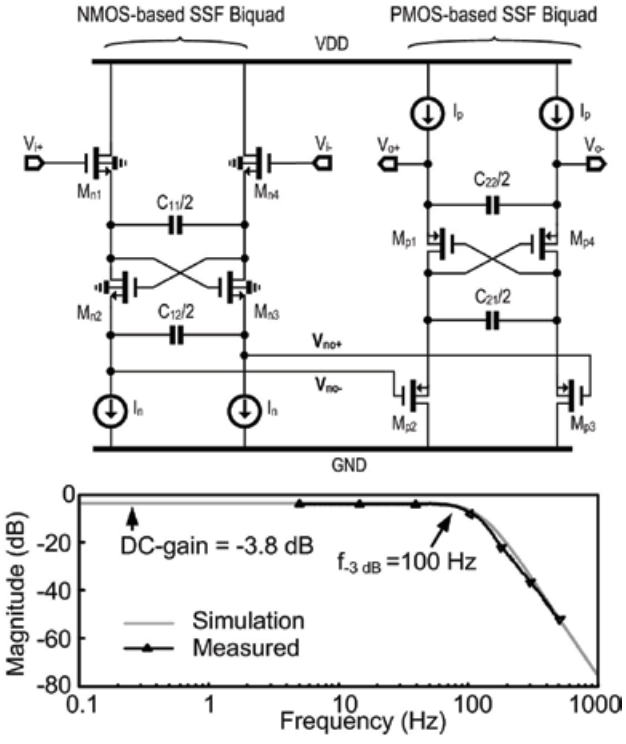


Fig. 1. Fabricated 4th-order non-GC LPF using SSF Biquads and measured gain performance.

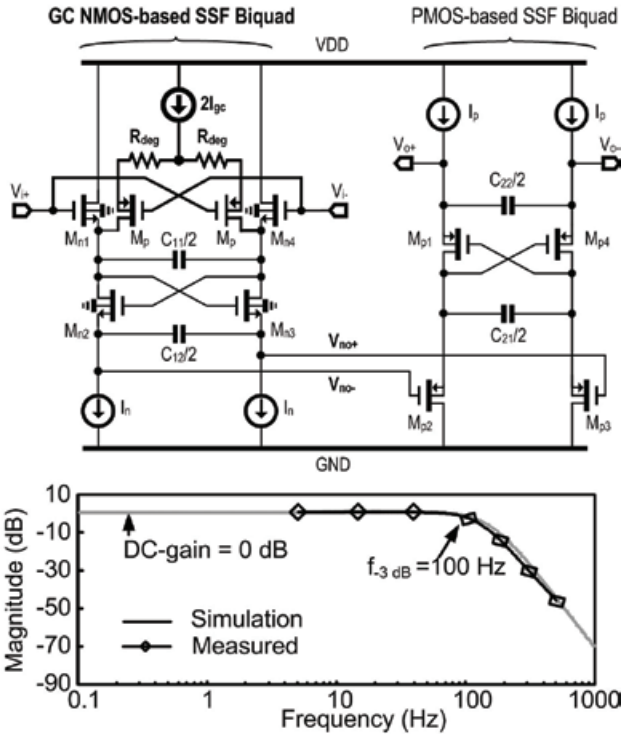


Fig. 2. Fabricated 4th-order GC LPF using SSF Biquads and measured gain performance.

Publication(s):

[1] T.-T. Zhang, P.-I. Mak, M.-I Vai, P.-U. Mak, M.-K. Law, S.-H. Pun, F. Wan, and R. P. Martins, "15-nW Biopotential LPFs in 0.35-μm CMOS Using Subthreshold-Source-Follower Biquads with and without Gain Compensation", IEEE Trans. Biomed. Circuits Syst., vol. 7, no. 5, pp. 690-702, Oct. 2013.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Energy Optimized Sub-threshold VLSI Logic Family with Unbalanced Pull-up/down Network and Inverse-Narrow-Width Techniques

Mingzhong Li, Chio-In Ieong, Man-Kay Law, Pui-In Mak, Mang-I Vai, Sio-Hang Pun, and Rui P. Martins

FEATURES

Low-voltage low-power sub-threshold logic cells
Unbalanced pull-up/down network with
Inverse-narrow-width technique
Transmission gate logic with logical effort optimization
High energy efficiency
Silicon verified in standard 0.18μm bulk CMOS

DESCRIPTION

Energy reduction achieved in sub-threshold operation is evidenced by the minimum energy point theory. However, the reduced overdrive voltage can dramatically worsen the device susceptibility in delay and noise margin due to process, voltage and temperature (PVT) variations, inevitably leads to sub-optimal performance in terms of power, delay and area, and even logic failure in the worst case.

This work presents a sub-threshold standard cell library targeting ultra-low-energy biomedical applications. In order to improve the energy efficiency, the unbalanced pull-up/down network, logical effort and inverse-narrow-width (INW) techniques are exploited. The unbalanced PU/PD network achieves a better energy efficiency as shown in Fig. 1(a), while the logical effort is utilized to qualitatively provide the delay spread estimate and distinguish dissimilar topologies of a particular logic for topology selection. The INW effect as shown in Fig. 1(b) is also exploited for circuit level optimization. Instead of using the smallest width per finger for both PMOS and NMOS transistors, analysis and silicon implementation of the INW effect using the power-delay-product (PDP) metric is initiated for optimal gate performance. An entity of 56 power-optimized sub-threshold logic cells using 0.3, 0.45 and 0.6V liberty files are implemented in standard 0.18μm CMOS (Fig. 1(c)). Measurement results from three 14-tap 8-bit FIR filters in Fig. 1(d) demonstrate substantial energy/cycle improvements.

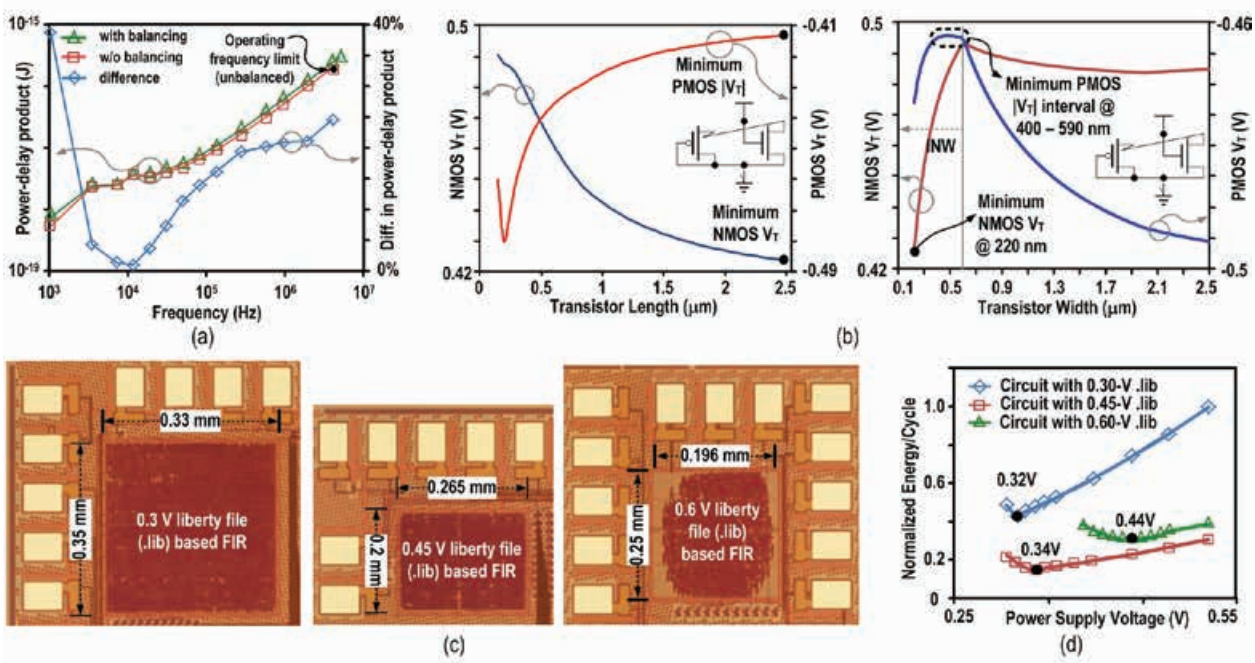


Fig. 1. (a) PDP of an inverter (FO4 loading) with balanced (P/N ratio = 5/1) and unbalanced (P/N ratio = 2/1) PU/PD network vs. operating frequency at 0.3 V. (b) NMOS/PMOS V_T vs. transistor length (RSC) (left) and transistor width (INW) (right) at V_{DD} = 0.3 V. (c) Die micrographs. (d) Normalized energy/cycle at different supplies.

Publication(s):

[1] M. Li, C.-I. Ieong, M.-K. Law, P.-I. Mak, M.-I Vai, S.-H. Pun, and R. P. Martins, "Energy Optimized Sub-threshold VLSI Logic Family with Unbalanced Pull-up/down Network and Inverse-Narrow-Width Techniques," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 12, pp. 3119-3123, Dec. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Multi-Channel Power-Supply Modulated Micro-Stimulator With Energy Recycling

Paul Jung-Ho Lee, Man-Kay Law, Amine Bermak, and Jun Ohta

FEATURES

Multi-channel stimulation with energy recycling
Adiabatic forward buck/reverse boost operation
Digital pulse-skipping PWM quasi-PID controller supporting wide output power dynamics
High stimulation efficiency up to 1.23mA
Silicon verified in standard 180nm BCDLite CMOS

DESCRIPTION

We propose a multi-channel power-supply modulated micro-stimulator capable of energy recycling. By tracking the instantaneous electrode voltage, the thermal dissipation of the current drivers is reduced. Multi-channel stimulation is achieved through decoupling electrodes from the power supply while providing isolation for improved safety. The D-PS-PWM-QPID controller is proposed to deliver the required charge for regulating the modulated power supply under various stimulation scenarios without parameter tuning or external passive components.

Fig. 1 shows the proposed micro-stimulator employing a global switch-mode power supply (SMPS) that can be shared among all the electrode drivers for online dynamic voltage scaling (DVS) according to the electrode voltage. The SMPS modulates the voltage at the intermediate energy storage capacitor (C_{IESC}) through the forward buck/reverse boost operation to either feed charges into the electrodes in the anodic phase, or drain charges in the cathodic phase. C_{IESC} allows the proposed topology to decouple the individual electrode drivers from the power supply, facilitating adiabatic energy recycling over multiple electrodes with reduced control overhead.

The prototype chip is fabricated in standard 180nm BCDLite CMOS, with the chip photo and voltage waveforms as shown in Fig. 2. With supply voltage modulation and electrode charge recycling, our work achieves a power saving of up to 70%. By decoupling the power supply from the electrode using C_{IESC}, our proposed micro-stimulator enables highly scalable stimulation applications.

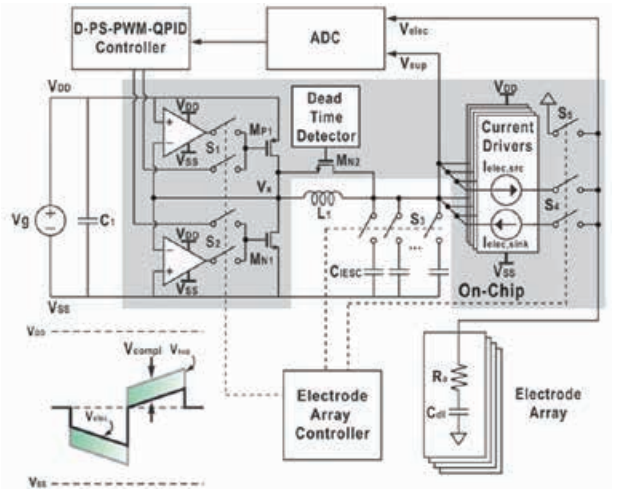


Fig. 1. Block diagram and of the proposed power-supply modulated micro-stimulator system and its output waveform during a biphasic stimulation cycle.

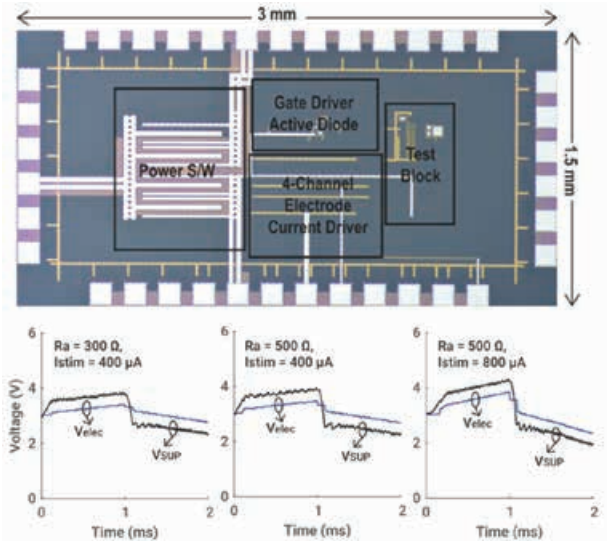


Fig. 2. Chip photo (top) and measured voltage waveforms during biphasic anodic first stimuli with different R_a and I_{stim}.

Publication(s):

[1] P. J.-H. Lee, M.-K. Law*, A. Bermak, and J. Ohta, "A Multi-Channel Power-Supply Modulated Micro-Stimulator With Energy Recycling," IEEE Des. Test, vol. 33, no. 4, pp. 61-73, Aug. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong RGC Research Grant

A 0.45-V 147-to-375 nW ECG Compression Processor with Wavelet Shrinkage and Adaptive Temporal Decimation Architectures

Chio-In Ieong, Mingzhong Li, Man-Kay Law, Pui-In Mak, Mang-I Vai, and Rui P. Martins

FEATURES

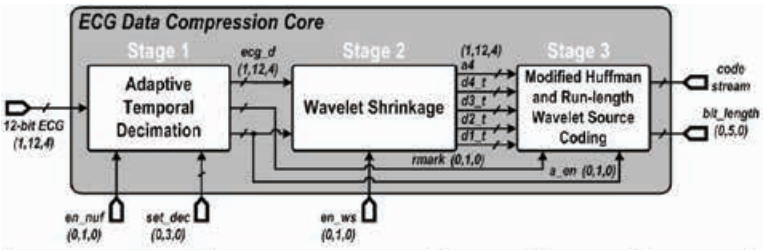
Wavelet shrinkage
Adaptive temporal decimation
Modified Huffman and run-length wavelet source coding
Low power consumption, 147 – 375nW
Wide compression ratio, 2.89 – 26.91
Low %-RMS-distortion, 0 – 3.11%
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

This work investigates the design of a specialized ECG compression processor using wavelet shrinkage (WS), adaptive temporal decimation (ATD) and a combined modified Huffman and run-length wavelet source coding (MHRLC) architectures. Also, a set of energy-efficient low-voltage digital logic circuits optimized for low frequency operation are custom designed and employed.

Fig. 1 shows the three main modules of the proposed processor. WT type (mother wavelet) and architecture are firstly selected and designed, balancing the accuracy, CR and hardware efficiency. WS is optimized to enable global threshold estimation without PRD degradation. ATD is exploited to decimate the ECG signal adaptively by discriminating the QRS wave and P/T waves. The sparse wavelet coefficients are then compressed using the MHRLC optimized for the application.

The single-channel ECG data-compression processor is fabricated in a 1P6M 0.18-μm CMOS process, with an active area of 0.86 mm^2. With a 0.45-V supply and an external 360-Hz clock, this work provides higher CR and lower power consumption, as well as succeeds in providing a wide range of CR across lossless and lossy compression while preserving a low PRD. Overall, the WT and shrinkage architecture optimizations contribute to 46% power reduction to the overall design power, while ATD and near-threshold circuit causes a power reduction of 56.8% and 30.02%, respectively. The proposed power-efficient real-time ECG processor achieves low power consumption (375 – 147 nW at 0.45 V), wide range of CR (2.89 – 26.91) and low PRD (0 to 3.11%), making it suitable for long-term ECG monitoring.



	This Work			Kim et al., Sym. VLSI'10	Chua et al., Tran. CE'11	Mamaghanian et al., EL'13
Verification Level	Experiment			Experiment	Simulation	Simulation
CMOS Tech. (nm)	180			180	65	180
VDD (V)	0.45			1.8	1	1
Operation Freq. (Hz)	360 (typical)			250-1k	24 M	100 M
Sampling Rate (Sa/s)	360 (typical)			250-1k	256	NA
BW (Bits)	12			16	10	NA
CR	2.89	5.24	26.91	8.4 or 2.1	2.38	2.43
PRD (%)	0	0.12	3.11	0.641	0	0
Power/Channel (μW)	0.313	0.375	0.147	6	56.6	36.4

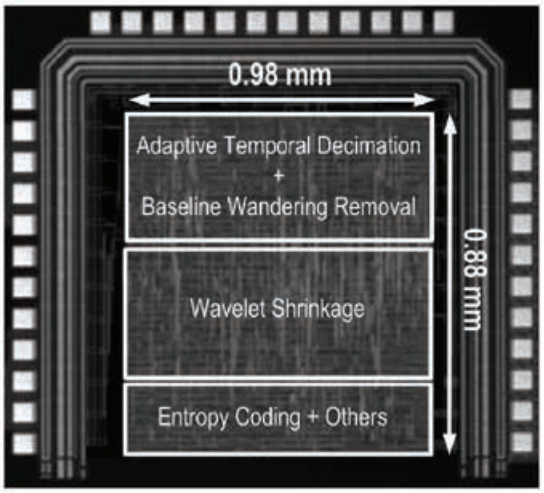


Fig. 1. Proposed ECG compression processor architecture (top left). Chip photograph (right). Performance comparison with state-of-the-art (bottom left).

Publication(s):

[1] C.-I. Ieong, M. Li, M.-K. Law, P.-I. Mak, M.-I Vai, and R. P. Martins, "A 0.45-V 147-to-375 nW Real-Time ECG Processor with Lossless-to-Lossy Data Compression for Wireless Healthcare Wearables," IEEE Trans. on Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 4, pp. 1307-1319, Jan. 2017.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

An Integrated Circuit for Simultaneous Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation

Changhao Chen, Elizabeth A. McCullagh, Sio Hang Pun, Peng Un Mak, Mang I Vai, Pui In Mak, A. Klug, and Tim C. Lei

FEATURES

Low input capacitance of the amplifier, 9.7pF
Low input referred noise of the amplifier, 4.57μV_{rms}
High SNR, 6.6
Adequate LED/laser drive-current, max. 330 mA

DESCRIPTION

The ability to record and to control action potential firing in neuronal circuits is critical to understand how the brain functions. The objective of this study is to develop a monolithic integrated circuit (IC) to record action potentials and simultaneously control action potential firing using optogenetics.

A low-noise and high input impedance (or low input capacitance) neural recording amplifier is combined with a high current laser/light-emitting diode (LED) driver in a single IC.

The low input capacitance of the amplifier (9.7 pF) was achieved by adding a dedicated unity gain stage optimized for high impedance metal electrodes. The input referred noise of the amplifier is 4.57 μV_{rms}, which is lower than the estimated thermal noise of the metal electrode. Thus, the action potentials originating from a single neuron can be recorded with a signal-to-noise ratio of at least 6.6. The LED/laser current driver delivers a maximum current of 330 mA, which is adequate for optogenetic control. The functionality of the IC was tested with an anesthetized Mongolian gerbil and auditory stimulated action potentials were recorded from the inferior colliculus. Spontaneous firings of fifth (trigeminal) nerve fibers were also inhibited using the optogenetic protein Halorhodopsin. Moreover, a noise model of the system was derived to guide the design.

A single IC to measure and control action potentials using optogenetic proteins is realized so that more complicated behavioral neuroscience research and the translational neural disorder treatments become possible in the future.

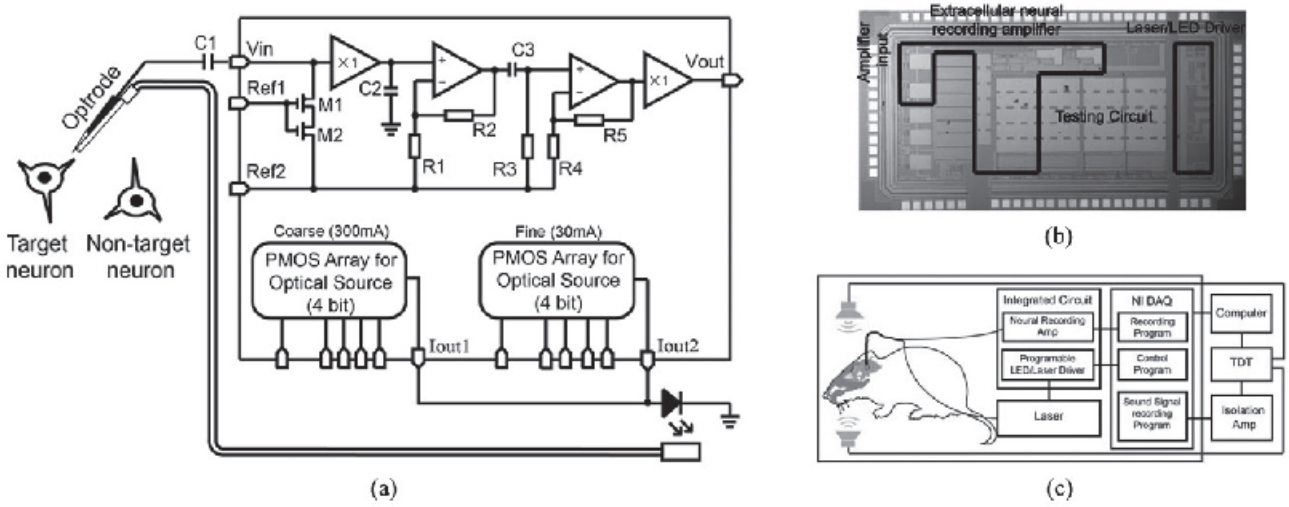


Fig. 1. (a) Schematic diagram of the IC integrating a high input impedance neural amplifier optimized of using a high impedance metal electrode for single neuron electrophysiology recording and two adjustable high current laser/LED drivers for optogenetic stimulation or inhibition; (b) Photograph of the fabricated IC with dimension of 2.9 mm × 1.6 mm. The actual neural amplifier and the laser/LED driver unit occupy about half of the space, with the rest of the space occupied by the additional testing circuits; (c) Experimental setup for simultaneous optogenetic inhibition and electrophysiological recordings from the brainstem of an anesthetized gerbil. The IC was connected to a data acquisition card (NI-DAQ) for signal digitization and laser power control. An isolation amplifier was used to isolate the neural amplifier from environmental noise. An audio signal processor (TDT) was used to generate a tonal signal to drive two speakers placed in the ears of the gerbil for auditory stimulation of the inferior colliculus.

Publication(s):

[1] C.H. Chen*, E. A. McCullagh, S.H. Pun*, P.U. Mak*, M.I Vai*, P.-I. Mak*, A. Klug, and T. C. Lei, "A Fully-Integrated Digital LDO with Coarse–Fine-Tuning and Burst-Mode Operation," IEEE Transactions on Biomedical Engineering, vol. 64, no. 3, pp. 557-568, Mar. 2017.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, National Institutes of Health (NIH) NIDDK and Optogenetics and Neural Engineering Core at the University of Colorado NIH/NINDS.

Design of a Collapse-Mode CMUT With an Embossed Membrane for Improving Output Pressure

Yuanyu Yu, Sio Hang Pun, Peng Un Mak, Ching-Hsiang Cheng, Jiujiang Wang, Pui-In Mak, and Mang I Vai

FEATURES

An embossed membrane CMUT is proposed to improve output pressure
Developed a beam model to analyze the embossed membrane
The optimum position for the embossed pattern is predicted by the beam model
The output pressure is improved by 55.1% and 88.1% by Si_3N_4 and nickel pattern

DESCRIPTION

Capacitive micromachined ultrasonic transducers (CMUTs) have emerged as a competitive alternative to piezoelectric ltrasonic transducers, especially in medical ultrasound imaging and therapeutic ultrasound applications, which require high output pressure. However, as compared with piezoelectric ultrasonic transducers, the output pressure capability of CMUTs remains to be improved. In this paper, a novel structure is proposed by forming an embossed vibrating membrane on a CMUT cell operating in the collapse mode to increase the maximum output pressure. By using a beam model in undamped conditions and finite-element analysis simulations, the proposed embossed structure showed improvement on the maximum output pressure of the CMUT cell when the embossed pattern was placed on the estimated location of the peak deflection.

As compared with a uniform membrane CMUT cell worked in the collapse mode, the proposed CMUT cell can yield the maximum output pressure by 51.1% and 88.1% enhancement with a single embossed pattern made of Si_3N_4 and nickel, respectively. The maximum output pressures were improved by 34.9% (a single Si_3N_4 embossed pattern) and 46.7% (a single nickel embossed pattern) with the uniform membrane when the center frequencies of both original and embossed CMUT designs were similar.

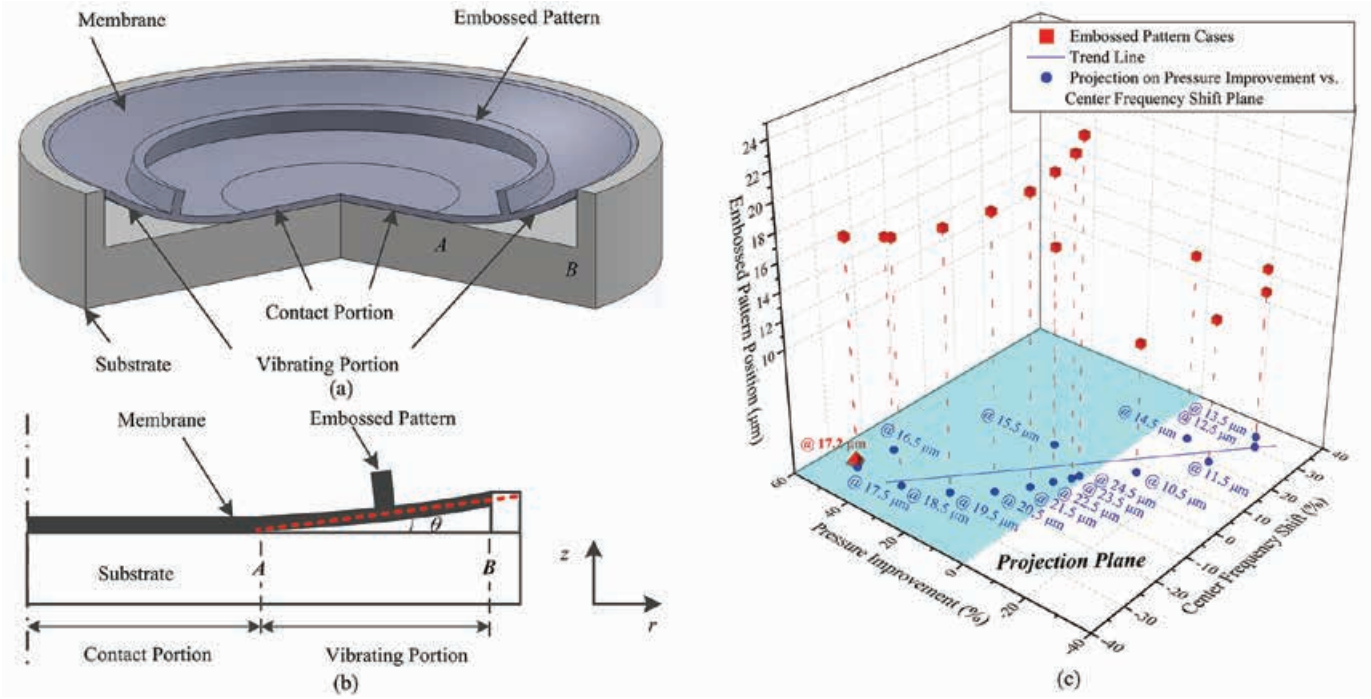


Fig. 1. (a) 3-D outlook view; (b) 2-D axisymmetric cross-sectional view of the proposed collapse-mode CMUT with an embossed membrane; (c) Relationship between pressure improvement and center frequency shift for various embossed positions.

Publication(s):

[1] Y.Y. Yu*, S.H. Pun*, P.U. Mak*, C.-H. Cheng, J.J. Wang*, P.-I. Mak*, and M.I Vai*, "Design of a Collapse-Mode CMUT With an Embossed Membrane for Improving Output Pressure," IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 63, no. 6, pp. 854-863, Jun. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Output Pressure Enhancement of CMUTs by Using Multiple Helmholtz Resonance Apertures

Yuanyu Yu, Xue Wen Cao, Sio Hang Pun, Peng Un Mak and Mang I Vai

FEATURES

Helmholtz resonant is applied in CMUTs design
Arrangement of Helmholtz resonant apertures are investigated
The output pressure is improved by 32.1%

DESCRIPTION

Capacitive micromcachined ultrasonic transducer (CMUT) is a new generation ultrasonic transducer, which is an alternative to the dominating piezoelectric ultrasonic transducer. However, the output pressure of CMUT is still low that limits its application. To improve the output pressure is one pursuit in CMUT design.

In this paper, Helmholtz resonant structure is applied in an air-coupled CMUT to improve the output pressure. The spring soften effect to the CMUT resonant frequency is taken into account in calculating the Helmholtz resonance apertures. 3-D finite element method (FEA) models are constructed to evaluate the performance of this design. Single and multiple Helmholtz resonance apertures are investigated and compared with a conventional CMUT. It is found that the output pressure can be improved by 32.1% with four Helmholtz resonance apertures placed symmetrically in the membrane.

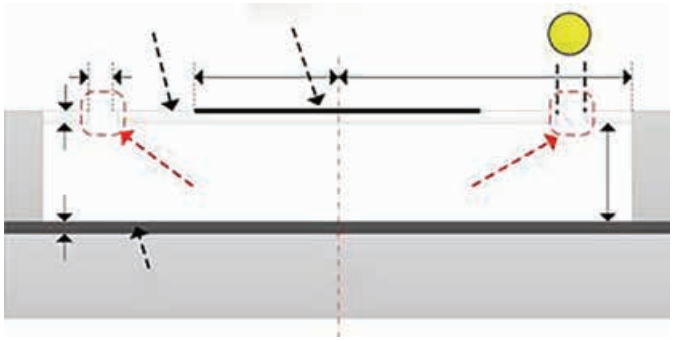


Fig. 1. Cross-section view of CMUT cell with Helmholtz resonance apertures (red dash line indicates central axis of CMUT cell (not in scale)).

Fig. 2. (a) 3D FEA model of CMUT cell and air domain: CMUT cell and air domain; (b) details of CMUT cell. All meshes except PML were smaller than 1/6 of wavelength of operating frequency; (c) Average output pressure over membrane: comparison between CMUTs with Helmholtz resonance apertures and conventional CMUT.

Publication(s):

[1] Y.Y.Yu, X.W. Cao, S.H. Pun, P.U. Mak and M.I Vai, "Output Pressure Enhancement of CMUTs by Using Multiple Helmholtz Resonance Apertures," Electronics Letters, vol. 51, no. 18, pp. 1390-1392, Sep. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Improved Analytical Modeling of Membrane Large Deflection With Lateral Force for the Underwater CMUT Based on Von Kármán Equations

Jiujiang Wang, Sio Hang Pun, Peng Un Mak, Ching-Hsiang Cheng, Yuanyu Yu, Pui-In Mak, and Mang I Vai

FEATURES

Low error in predicting displacement profile of conventional mode CMUT, <1%
Low error in predicting displacement profile of collapse mode CMUT, <4.7%

DESCRIPTION

This paper is to develop analytical models for the underwater capacitive micromachined ultrasonic transducer (CMUT) to understand its large deflection effect from the water pressure. To accurately model the displacement profile of the CMUT under the water pressure, Von Kármán equations and the perturbation method are employed to calculate the membrane deformation from a uniform pressure. The equations for an annular-ring plate model are first applied to calculate the displacement profile of the uniform CMUT membrane. The lateral force due to the membrane elongation is considered in the proposed model, which is used to calculate the displacement profiles for both conventional and collapse mode CMUTs under different external pressures.

When compared with finite-element method results, the proposed model can predict the displacement profiles of the conventional-mode CMUT under water pressure ranging from 0.8 to 4 MPa with an error of <1%. It can also estimate CMUT membrane that operates in collapse mode with an error in the deflection profile for <4.7% from 5 to 14 MPa. In addition, it is worth to mention that the proposed model can cover the small deflection scenarios but with relatively larger error under collapse mode.

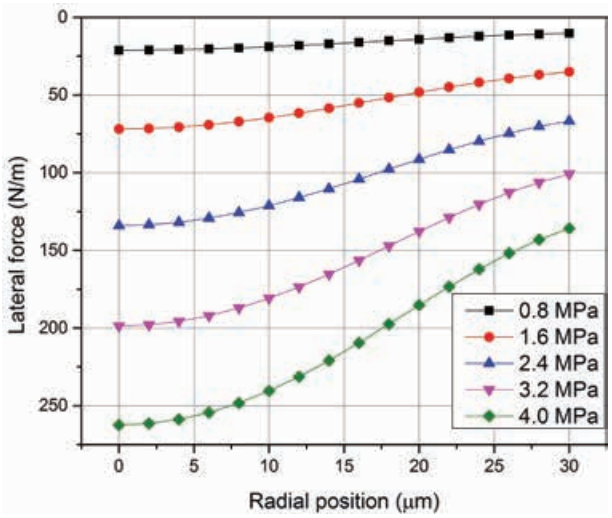


Fig. 1. Modeling results of lateral force for the large deflection membrane in conventional mode.

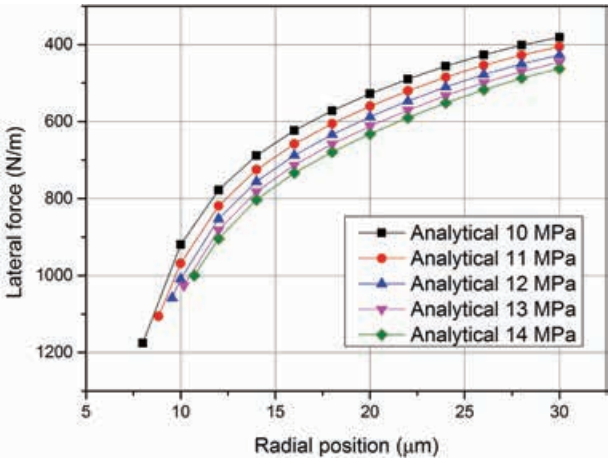


Fig. 2. Modeling results of the lateral force for the large deflection membranes in collapse mode.

Publication(s):

[1] J.J. Wang*, S.H. Pun*, P.U. Mak*, C.-H. Cheng, Y.YYu*, P.-I. Mak* and M.I Vai*, "Improved Analytical Modeling of Membrane Large Deflection With Lateral Force for the Underwater CMUT Based on Von Kármán Equations," IEEE Sensors Journal, vol. 16, no. 17, pp. 6633-6640, Sep. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Alpha neurofeedback training improves SSVEP-based BCI performance

Feng Wan, Janir Nuno da Cruz, Wenya Nan, Chi Man Wong, Mang I Vai, and Agostinho Rosa

FEATURES

Higher SSVEP signal SNR, 16.5% improved compared to the non-NFT control group
Higher BCI classification accuracy, 20.3% improved compared to the non-NFT control group

DESCRIPTION

Steady-state visual evoked potential (SSVEP)-based brain-computer interfaces (BCIs) can provide relatively easy, reliable and high speed communication. However, the performance is still not satisfactory, especially in some users who are not able to generate strong enough SSVEP signals. This work aims to strengthen a user's SSVEP by alpha down-regulating neurofeedback training (NFT) and consequently improve the performance of the user in using SSVEP-based BCIs.

An experiment with two steps was designed and conducted. The first step was to investigate the relationship between the resting alpha activity and the SSVEP-based BCI performance, in order to determine the training parameter for the NFT. Then in the second step, half of the subjects with 'low' performance (i.e. BCI classification accuracy <80%) were randomly assigned to a NFT group to perform a real-time NFT, and the rest half to a non-NFT control group for comparison.

The first step revealed a significant negative correlation between the BCI performance and the individual alpha band (IAB) amplitudes in the eyes-open resting condition in a total of 33 subjects. In the second step, it was found that during the IAB down-regulating NFT, on average the subjects were able to successfully decrease their IAB amplitude over training sessions. More importantly, the NFT group showed an average increase of 16.5% in the SSVEP signal SNR (signal-to-noise ratio) and an average increase of 20.3% in the BCI classification accuracy, which was significant compared to the non-NFT control group.

These findings indicate that the alpha down-regulating NFT can be used to improve the SSVEP signal quality and the subjects' performance in using SSVEP-based BCIs. It could be helpful to the SSVEP related studies and would contribute to more effective SSVEP-based BCI applications.

Group	Test	SSVEP SNR	Classification accuracy (%)
NFT	Test_1 (before NFT)	2.262 ± 0.685	65.4 ± 7.2
	Test_2 (after NFT)	2.635 ± 0.763	78.7 ± 6.3
Control	Test_1	2.431 ± 0.674	63.4 ± 14.7
	Test_2	2.378 ± 0.702	63.3 ± 14.6

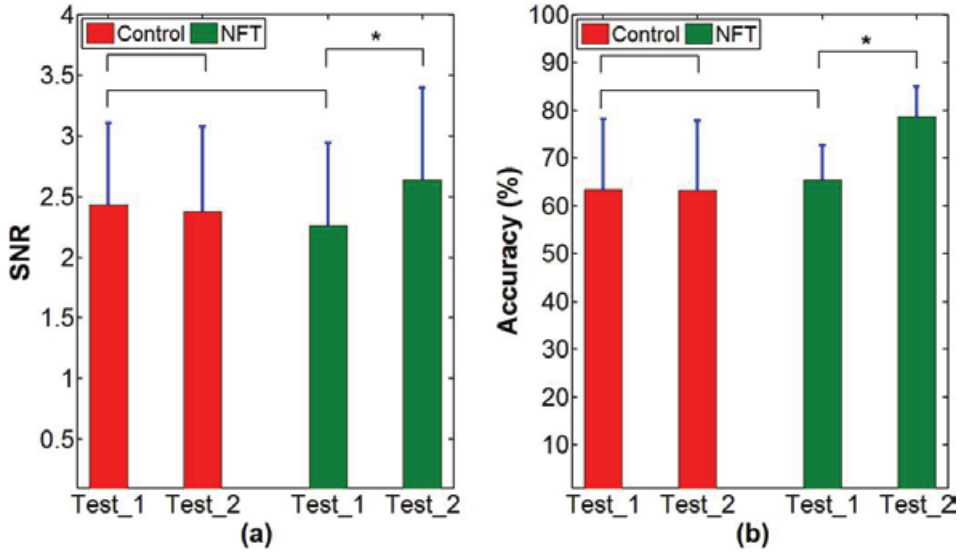


Fig. 1. Comparisons of the SSVEP-based BCI performance in the NFT and the control groups in terms of (a) the SSVEP SNR, and (b) the BCI classification accuracy. (Error bar indicates the SD, * represents the significant difference, $p < 0.05$).

Publication(s):

[1] F. Wan*, J. Nuno da Cruz*, W. Nan*, C.M. Wong*, M.I Vai* and A. Rosa, "Alpha neurofeedback training improves SSVEP-based BCI performance," Journal of Neural Engineering, vol. 13, no. 3, May 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Effects of Human Limb Gestures on Galvanic Coupling Intra-body Communication for Advanced Healthcare System

Xi Mei Chen, Sio Hang Pun, Jian Feng Zhao, Peng Un Mak, Bo Dong Liang, and Mang I. Vai

FEATURES

Revealed the dynamic behavior of galvanic coupling IBC channel

Provided suggestions for practical IBC system design

DESCRIPTION

Intra-Body Communication (IBC), which utilizes the human body as the transmission medium to transmit signal, is a potential communication technique for the physiological data transfer among the sensors of remote healthcare monitoring system, in which the doctors are permitted to remotely access the healthcare data without interrupt to the patients' daily activities.

This work investigates the effects of human limb gestures including various joint angles, hand gripping force and loading on galvanic coupling IBC channel. The experiment results show that channel gain is significantly influenced by the joint angle (i.e. gain variation 1.09–11.70 dB, $p < 0.014$). The extension, as well as the appearance of joint in IBC channel increases the channel attenuation while the other gestures and muscle fatigue have negligible effect (gain variation <0.77 dB, $p > 0.793$) on IBC channel. Moreover, the change of joint angle on human limb IBC channel causes significant variation in bit error rate (BER) performance.

The results reveal the dynamic behavior of galvanic coupling IBC channel, and provide suggestions for practical IBC system design.

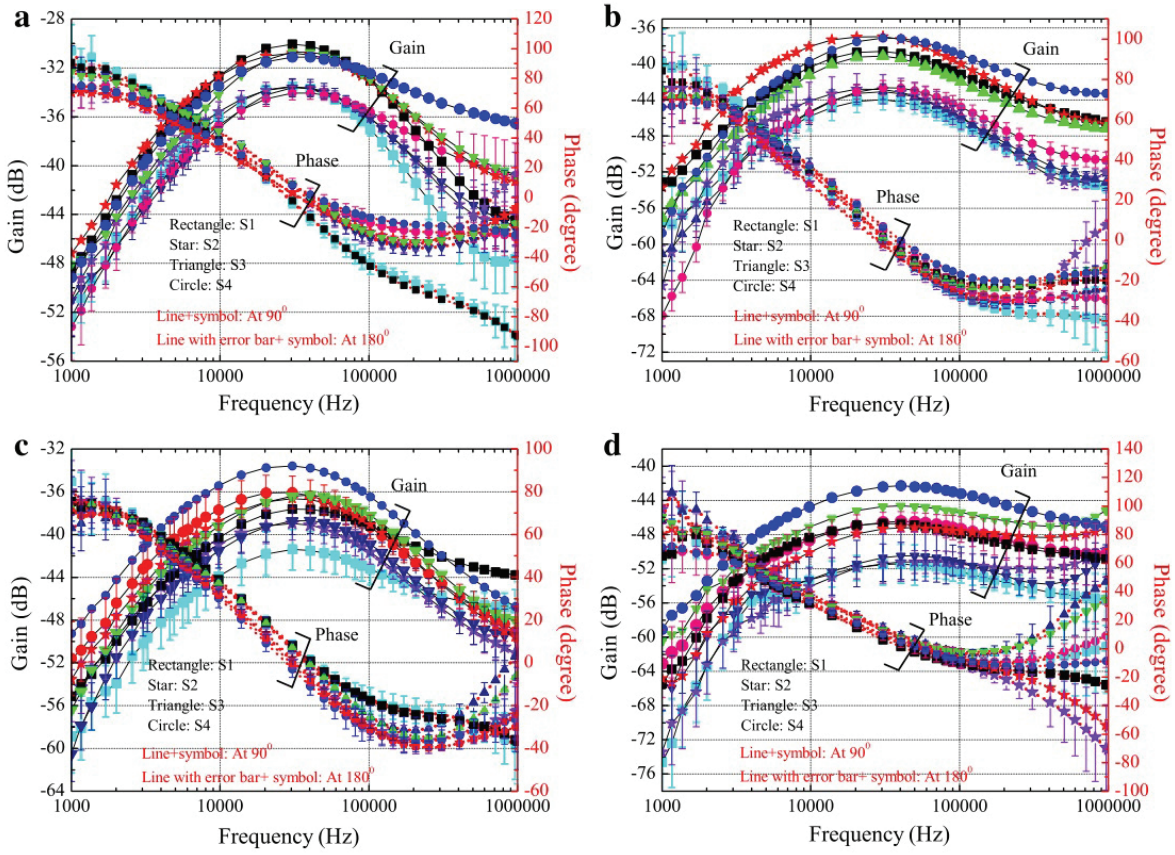


Fig. 1. Gain and phase at two joint angles for the four subjects. The values at 90° are depicted by lines with symbols. Lines with error bars (variance over 3 days measurement) and symbols represent the values at 180°. The values from channel A1A2, A1A3, B1B2 and B1B3 are displayed in sub-figure a, b, c and d, respectively. Lines with symbol rectangular, star, triangle and circle is for S1, S2, S3 and S4, respectively.

Publication(s):

[1] X.M. Chen*, S.H. Pun*, J.F. Zhao, P.U. Mak*, B.D. Liang and M.I. Vai*, "Effects of human limb gestures on galvanic coupling intra-body communication for advanced healthcare system," Biomedical engineering online, May 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Shenzhen Polytechnic and Guangdong Provincial Science and Technology Plan

Channel Modeling and Power Consumption Analysis for Galvalnic Coupling Intra-body Communication

Yue Ming Gao, Yan Ting Ye, Mang I Vai, Min Du, and Sio Hang Pun

FEATURES

Low Bit Error Rate, 10^{-6}
Low power consumption, 2.3 μJ/bit

DESCRIPTION

Intra-body communication (IBC), using the human body as the channel to transmit data, has lower power consumption, less radiation, and easier linking than common wireless communication technologies such as Bluetooth, ZigBee, and ANT+ . As a result, IBC is greatly suitable for body area network (BAN) applications, such as the medical and health care field. Furthermore, IBC can be implemented in wearable devices, including smart watches, sports bracelets, somatic game devices, and multimedia devices. However, due to the limited battery capacity of sensor nodes in a BAN, especially implanted sensor nodes, it is not convenient to charge or change the batteries. Thus, the energy effectiveness of the media access control (MAC) layer strongly affects the life span of the nodes and of the entire system. Certainly, analyzing MAC layer performance in a galvanic coupling IBC is of great importance for the overall system. To obtain the attenuation properties of IBC, in vivo experiments with seven volunteers were performed.

Meanwhile, an equalizer was used to compensate the frequency distortion in consideration of frequency-selective fading characteristics of intra-body channels. In addition, a comparison of the bit error rates (BER) of different modulation methods was carried out to obtain the best modulation method. Then, the attenuation characteristics of intra-body channels were applied in a multi-node physiological signal monitor and transmission system. Finally, TDMA and CSMA/CA protocols were introduced to calculate the bit energy consumption of IBC in the practical scenario. With stable characteristics of the intra-body channels, QPSK with an equalizer had a better performance than the tests without an equalizer. As a result, the modulation method of FSK could achieve a lower BER in lower signal-to-noise ratio situations and an FSK method with TDMA for the IBC had the lowest energy consumption under different practical scenarios.

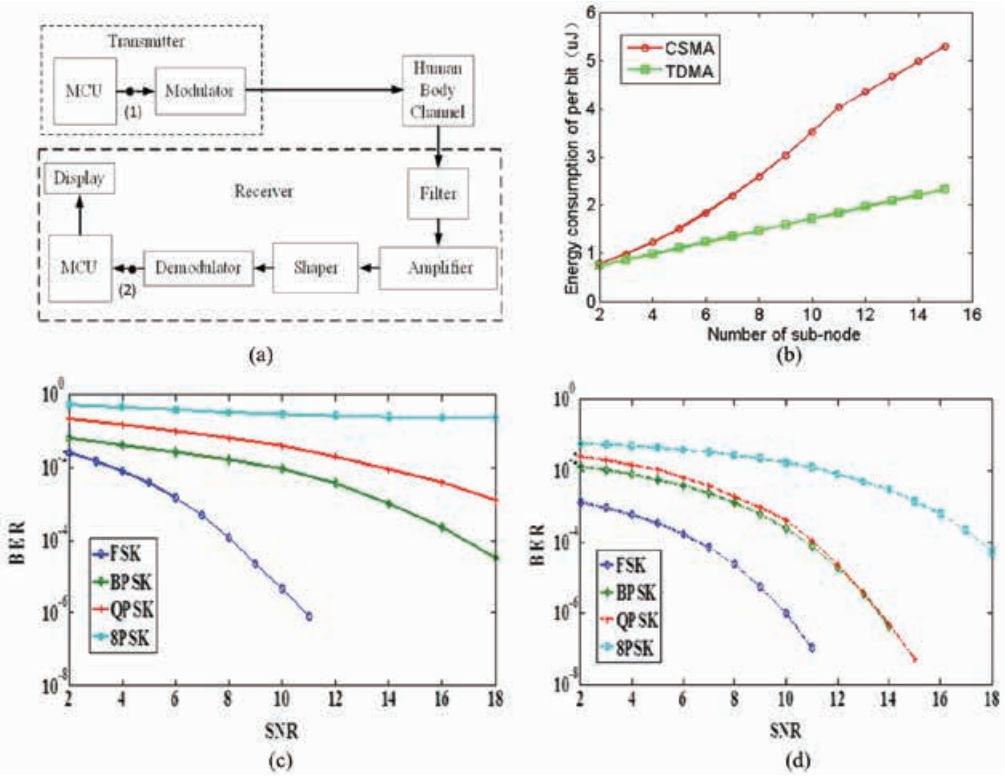


Fig. 1. (a) Diagram of intra-body communication; (b) Energy consumption comparisons of TDMA and CSMA/CA under the multi-node system; (c) BER versus SNR of four kinds of modulation method with equalizer and (d) without equalizer.

Publication(s):

[1] Y.M. Gao, Y.T. Ye, M.I Vai*, M.D. and S.H. Pun*, "Channel modeling and power consumption analysis for galvanic coupling intra-body communication," EURASIP Journal on Wireless Communications and Networking, vol. 2016, no. 106, Jun. 2016.

* Contributors with University of Macau

Sponsorship:

Chinese Ministry of Science and Technology, National Natural Science Foundation of China, Department of Education of Fujian Province and Department of Education of Fujian Province

A Novel Field-Circuit FEM Modeling and Gain Estimation for Galvanic Coupling Real IBC Measurements

Yue-Ming Gao, Zhu-Mei Wu, Sio-Hang Pun, Peng-Un Mak, Mang-I Vai, and Min Du

FEATURES

Low error, 3 dB in range of 10 kHz to 500 kHz,
9 dB in range of 500 kHz to 1 MHz

DESCRIPTION

Existing research on human channel modeling of galvanic coupling intra-body communication (IBC) is primarily focused on the human body itself. Although galvanic coupling IBC is less disturbed by external influences during signal transmission, there are inevitable factors in real measurement scenarios such as the parasitic impedance of electrodes, impedance matching of the transceiver, etc. which might lead to deviations between the human model and the in vivo measurements. This paper proposes a field-circuit finite element method (FEM) model of galvanic coupling IBC in a real measurement environment to estimate the human channel gain.

First an anisotropic concentric cylinder model of the electric field intra-body communication for human limbs was developed based on the galvanic method. Then the electric field model was combined with several impedance elements, which were equivalent in terms of parasitic impedance of the electrodes, input and output impedance of the transceiver, establishing a field-circuit FEM model. The results indicated that a circuit module equivalent to external factors can be added to the field-circuit model, which makes this model more complete, and the estimations based on the proposed field-circuit are in better agreement with the corresponding measurement results.

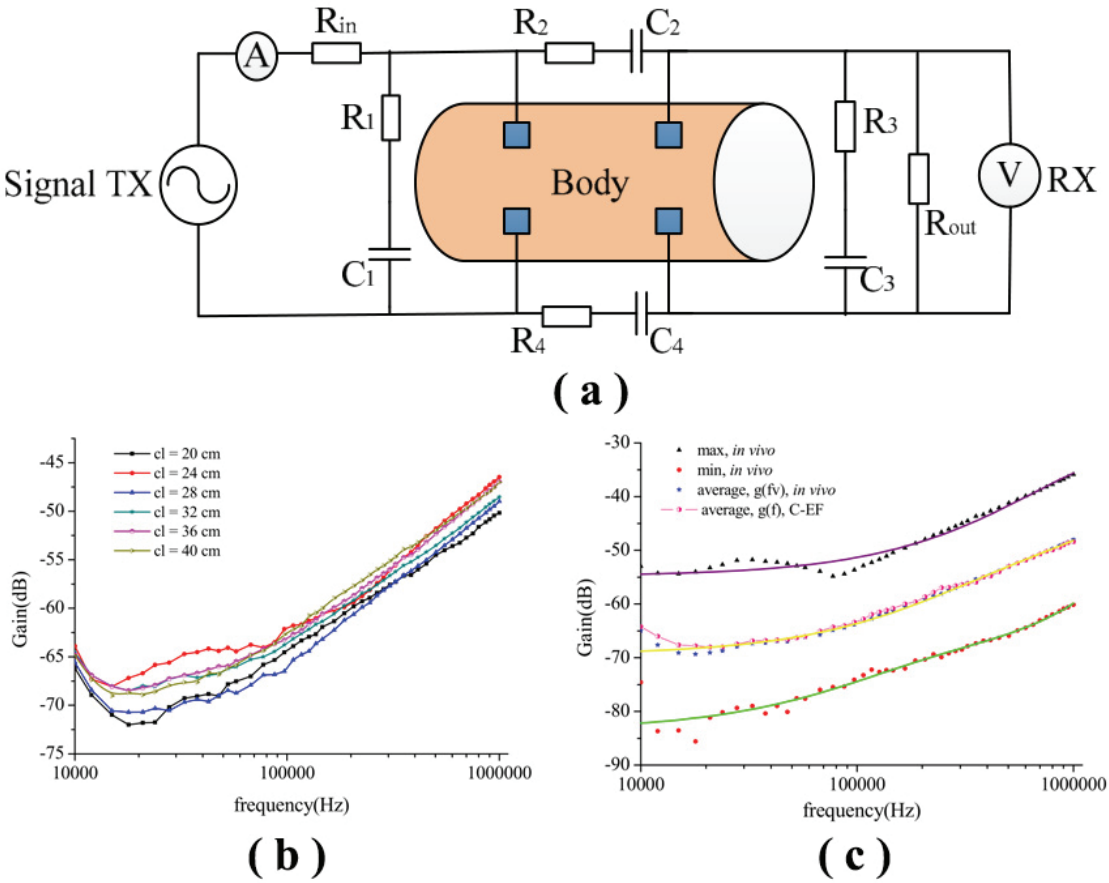


Fig. 1. (a) The field-circuit model of signal transmission path in the galvanic intra-body communication; (b) mean values of the long distance intra-body communication channel characteristic, measured on 10 subjects at different distances; (c) mean values of the long distance human body channel amplitude characteristic variation range, measured on 10 test subjects. The star curve and red dot line curve represent the average voltage gain for the channel length in the range of 20 cm.

Publication(s):

[1] Y.-M. Gao, Z.-M. Wu, S.-H. Pun*, P.-U. Mak*, M.-I Vai* and M. Du, "A Novel Field-Circuit FEM Modeling and Channel Gain Estimation for Galvanic Coupling Real IBC Measurements," Sensors, vol. 16, no. 471, 2016.

* Contributors with University of Macau

Sponsorship:

Chinese Ministry of Science and Technology, National Natural Science Foundation of China, and Department of Education of Fujian Province, China

Direct Measurement of Elbow Joint Angle Using Galvanic Coupling System

Xi Mei Chen, Shovan Barma, Sio Hang Pun, Mang I Vai, and Peng Un Mak

FEATURES

Low error, ±0.11 rad (6°)
High compatibility

DESCRIPTION

This paper proposes a simple approach to measure the elbow joint angle (EJA) using galvanic coupling system (GCS), directly; whereas, the traditional methods involved in either complex machine-learning task or arm movement models in which the consideration of model parameters are not accurate very often. First, a correlation between the EJA and GCS data has been established by defining a polynomial function based on a simple six-impedance model of human upper arm, where the EJA (θ) has been achieved by moving the forearm along the sagittal and transverse planes with different loads (empty hand, 1 and 2 kg). The coefficients of the polynomial are estimated based on the polynomial fit technique in which the actual angles (reference frame) are calculated by using motion data.

In total, eleven subjects (seven males and four females) with the age of 30 ± 6 years have been considered during the experiment. However, the GCS data of eight subjects are used to derive the correlation, exclusively. Furthermore, the influence of muscle fatigue and different loads on the derived correlation has been studied. Next, based on the derived correlation, the EJA has been measured in two parts–inside and outside tests by considering six subjects. The results show that the proposed idea can measure the EJA very effectively with error up to ±0.11 rad (6°). Moreover, in a performance comparison, the proposed approach shows its compatibility by indicating low complexity, higher accuracy, and easy to measure.

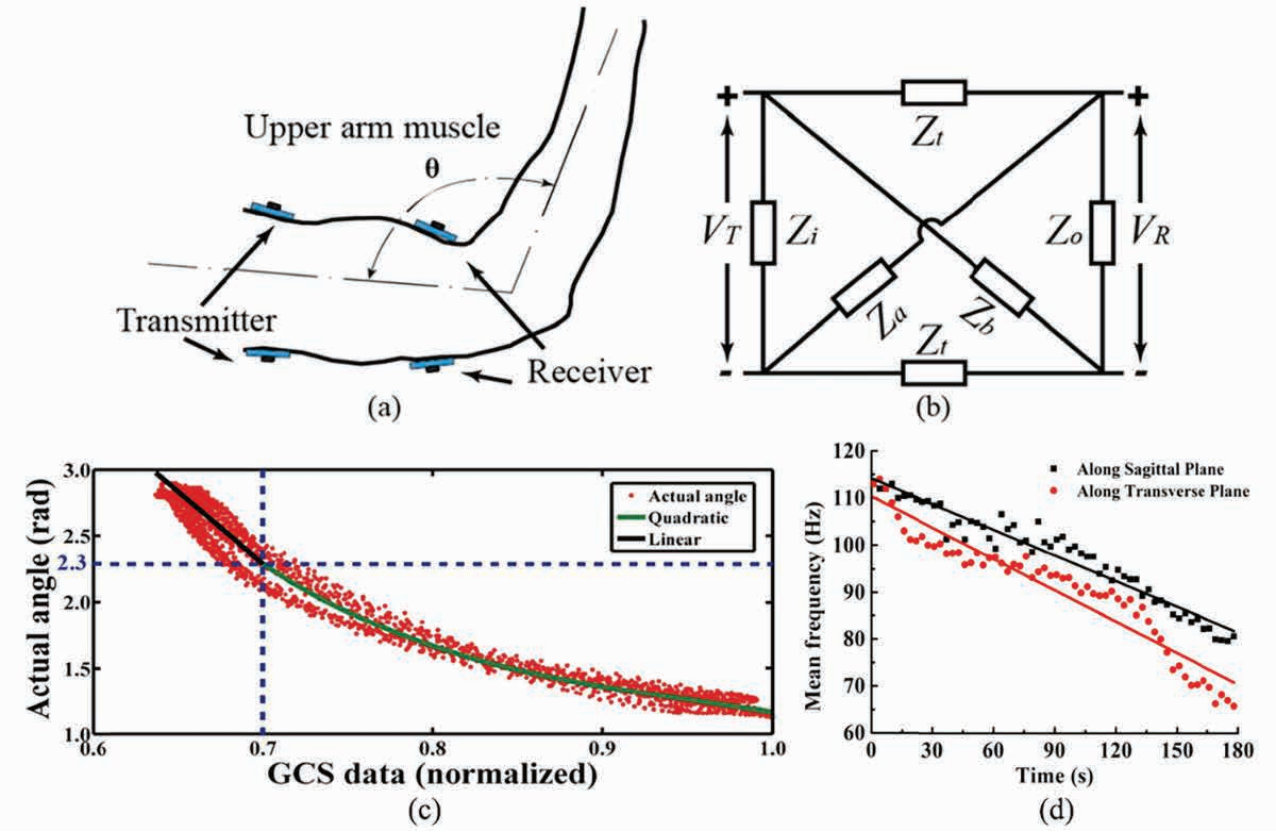


Fig. 1. (a) Schematic of the galvanic couple system on upper arm muscles; (b) Equivalent circuit model of upper arm; (c) Analysis of the curve fitting between GCS data and EJA; (d) Muscle fatigue during forearm movement (for 2 kg load).

Publication(s):

[1] X.M. Chen*, S. Barma*, S.H. Pun*, M.I Vai*, and P.U. Mak*,"Direct Measurement of Elbow Joint Angle Using Galvanic Couple System," IEEE Transactions on Instrumentation and Measurement, vol. 66, no. 4, pp. 757-766, Apr. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS
ENERGY HARVESTING AND SENSING CIRCUITS

A 12 pJ/pixel Analog-to-Information Converter based 816 x 640 Pixel CMOS Image Sensor

Denis Guangyin Chen, Fang Tang, Man-Kay Law, and Amine Bermak

FEATURES

Aanlog-to-Information conversion (AIC)
Pixel-level compression with bit-image processor
Area-efficient SAR-SS hybrid ADC
High energy efficiency, 12 pJ/pixel·frame
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

To achieve improved energy efficiency for image sensors, the most aggressive approach is to integrate image compression at or before the point of quantization. In this work, a column-parallel AIC based on visual pattern image coding (VPIC) is proposed. When compared with other algorithm classes, VPIC has the advantage of not requiring any matrix operations. The proposed AIC circuit is prototyped in a high-resolution image sensor. The charge-transfer-amplifier (CTA) integrates a charge-pump bit-image processor (BIP) with a successive approximation-register-single-slope (SAR-SS) hybrid ADC. The SAR-SS ADC's capacitor array is exploited to provide additional functionalities both as a load for the CTA and as a computational device to perform parts of the compression algorithm.

The basic algorithm is illustrated in Fig. 1(a). The mean u and gradient G is calculated for a 4x4 pixel block, and the bit-image B is quantized by comparing each pixel to u. If G is less than a threshold, then the pixel block is a uniform pattern (UP), otherwise, it is an edge pattern (EP). The entire column circuit is depicted in Fig. 1(b). A charge-transfer amplifier (CTA) is used to implement correlated double sampling (CDS). The chip prototype is fabricated in 0.18-μm CMOS, as shown in Fig. 1(c). Fig. 1(e) and (f) shows the captured image using the chip prototype in compression and raw mode respectively. This work achieves an energy consumption of 12 pJ/pixel, which is the most energy efficient CMOS image sensor to date.

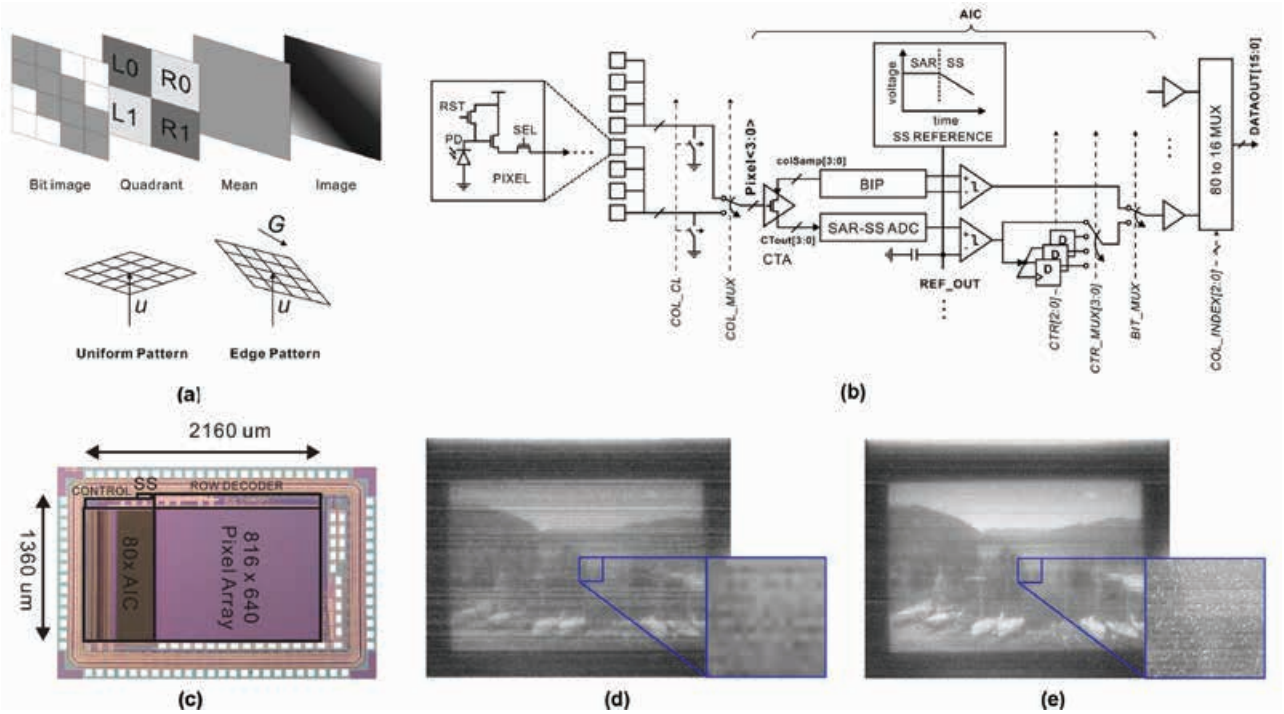


Fig. 1. (a) Components used in the image compression algorithm. (b) Column circuit: from pixel to AIC. (c) Chip micrograph. (d) Image captured from the chip prototype in compression mode. (e) Image captured in raw mode.

Publication(s):

[1] D. G. Chen, F. Tang, M.-K. Law* and A. Bermak, "A 12 pJ/pixel Analog-to-Information Converter based 816 x 640 Pixel CMOS Image Sensor," IEEE J. Solid-State Circuits, vol. 49, no. 5, pp. 1210-1222, May 2014.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Hong Kong Research Grant Council

A 64 fJ/step 9-bit SAR ADC Array With Forward Error Correction and Mixed-Signal CDS for CMOS Image Sensors

Denis Guangyin Chen, Fang Tang, Man-Kay Law, Xiaopeng Zhong, and Amine Bermak

FEATURES

Pilot-Digital-to-Analog Converter (pDAC)
Forward error correction
Mixed-signal correlated-double-sampling
Figure-of-Merit of 64 fJ/step
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

The main challenge of column parallel SAR ADCs for image sensors lies in achieving adequate resolution in a very small capacitor array. The pDAC described introduces input independent Forward-Error-Correction (FEC), mixed-signal CDS, parasitic effect reduction, and energy efficient dynamic comparators.

The basic pDAC operation is illustrated in Fig. 1. The input signal is sampled onto the top-plate of the capacitor array during sampling. During MSB phase, the pDAC array is one quarter of the size of the MSB array with the exception of C_{92}. Once the 4 MSBs are determined, the rest of the MSB and LSB capacitors are connected on the fifth clock without any trial-and-error. In FEC phase, the missing code issue is addressed by introducing a redundant bit-trial. During the error correction clock, C_{N-k} is restored to GND, this creates a negative perturbation on V_{DAC}. Both positive and negative errors from earlier bit-trials can be recovered by the C_{N2} weight (C_{92} in this case) under the accuracy of the full-sized capacitor array. In LSB phase, the 5 LSBs in the SAR ADC are obtained using the conventional switching sequence.

The chip prototype is fabricated in a standard 0.18-µm CMOS process. As shown in Fig. 2, the large DNL error due to missing codes at 125th and 350th code entry in the conventional DAC is resolved by the reported FEC algorithm. The INL, on the other hand, is limited by the accuracy of the full capacitor-array. The work achieves one of the smallest and most energy efficient designs with the best FoM among ADCs found in state-of-the-art image sensors.

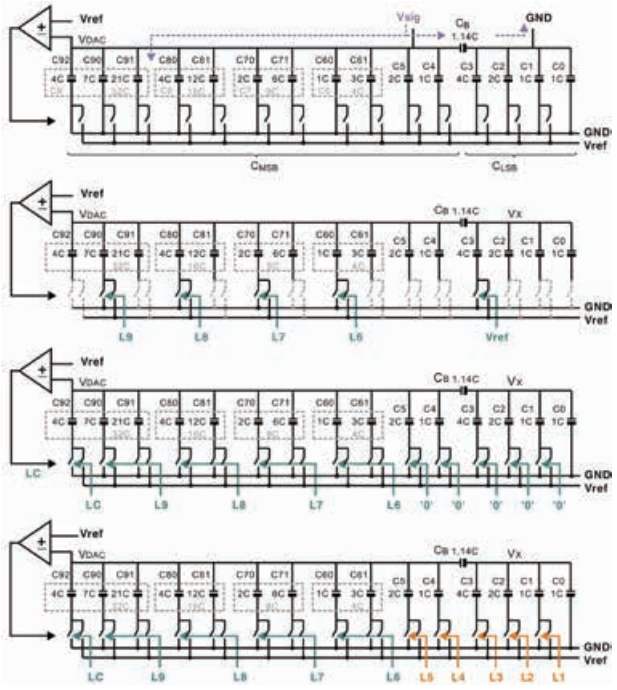


Fig. 1. (a) sampling; (b) MSB; (c) FEC; and (d)LSB.

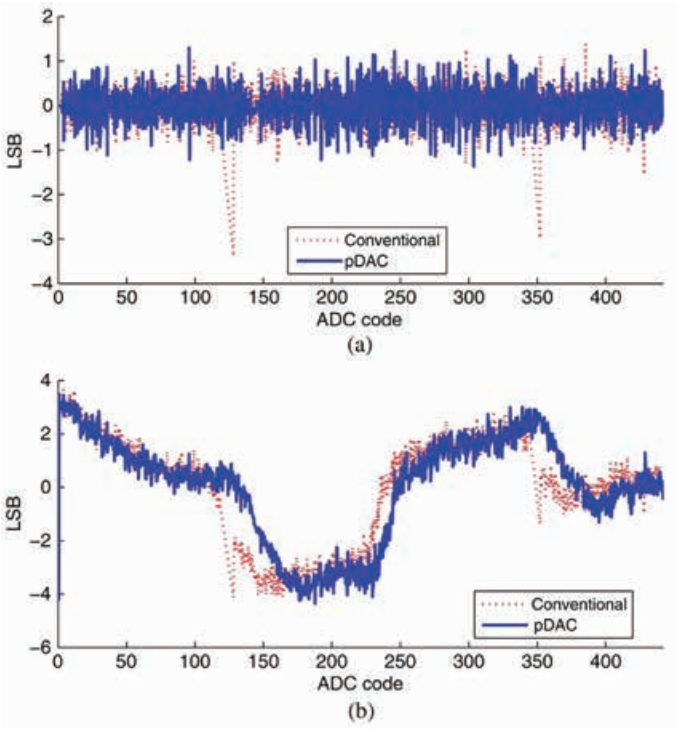


Fig. 2. (a) DNL and (b) INL of the 9 b SAR ADC.

Publication(s):

[1] D. G. Chen, F. Tang, M.-K. Law*, X. Zhong and A. Bermak, "A 64-fJ/step 9-bit SAR ADC Array with Forward Error Correction and mixed-signal CDS for CMOS Image Sensors," IEEE Trans. Circuits Syst.-I: Reg Papers, vol. 61, no. 11, pp. 3085-3093, Nov. 2014.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Passive RFID Tag Embedded Temperature Sensor With Improved Process Spreads Immunity for a -30°C to 60°C Sensing Range

Bo Wang, Man-Kay Law, Amine Bermak, and Howard C. Luong

FEATURES

Embedded CMOS temperature sensor in passive RFID tag system
Improved PVT spread immunity
High accuracy, ±0.15 °C (3σ) from -30 to 60 °C
Low power, 0.35 µA at 1-V supply
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

Embedding the temperature sensing function into passive RFID tag brings new challenges in terms of system design. Firstly, the embedded sensor should be ultra-low power (in the order of sub-µW) to prevent loss in the RFID tag's sensitivity; Secondly, the occupied sensor area and its calibration effort should be minimized to maintain low cost. Thirdly, for passive tags, as the sensor is supplied by the on-chip power management unit (PMU) and a good supply rejection is necessary to achieve accurate sensing.

This work targets at a -30 to 60 °C for cold chain food monitoring, medicines and health commodities storage range, as well as the general environment monitoring. A resistor, capacitor and on-chip clock frequency PVT variations compensation technique is embodied in a time-domain readout to improve the process spreads immunity. Fig. 1 shows the simplified circuit implementation of the embedded temperature sensor readout. It consists of three capacitor, C_{ref}, C_{pt} and C_{ct}, two comparator branches A_1 and A_2, and other digital blocks. Once the sensor is enabled by sen_EN, $M_{2\text{-}4}$ are turned on to steer the current signals from the sensor frontend. With all the capacitors initially reset, $I_{pt}(T)$ and $I_{ct}(T)$ charges C_{pt} and C_{ct}, respectively, while I_{ref} charges C_{ref}. At the end of integration, a temperature dependent pulse-width $t_{PW}(T)$ is generated, which is then digitized with a ripple counter. The calling edge of $t_{PW}(T)$ indicates the end of one sensing cycle.

Fig. 2 shows the chip prototype fabricated in a standard 180nm bulk CMOS process, with the temperature sensor is embedded in a passive RFID tag. Measurement results show that a sensing error of ±1.5 °C (3σ) is achieved from -30 to 60 °C. Our work achieves a good tradeoff among robustness, sensing power and sensing accuracy in the passive RFID platform. Moreover, this work requires only one-point calibration for its process immunity, which ensures the sensing tag to be low cost.

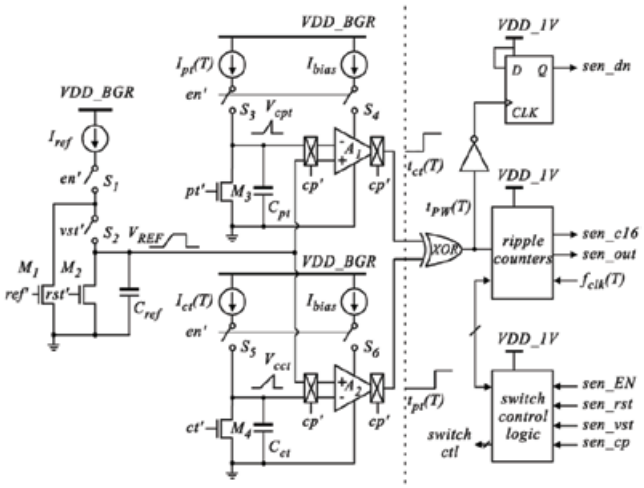


Fig. 1. Implementation of the proposed temperature sensor core.

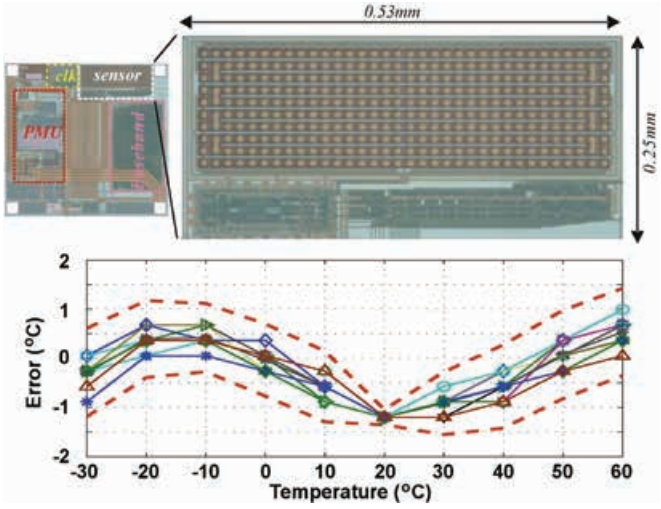


Fig. 2. Chip prototype in a RFID tag system (top) and measured inaccuracy of 12 sensor tag samples.

Publication(s):

[1] B. Wang, M.-K. Law*, A. Bermak and H. C. Luong, "A Passive RFID Tag Embedded Temperature Sensor With Improved Process Spreads Immunity for a -30 to 60 Sensing Range", IEEE Trans. Circuits Syst.-I: Reg. Papers, vol. 61, no. 2, pp. 337 – 346, Feb. 2014.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Low-power CMOS Laser Doppler Imaging using Non-CDS Pixel Readout and 13.6-bit SAR ADC

Denis Guangyin Chen, Man-Kay Law, Yong Lian, and Amine Bermak

FEATURES

Fully customized laser doppler imager (LDI)
Non-CDS pixel readout scheme
Column 13.6b SAR ADC
State of the art Figure-of-Merit, 23 fJ/state
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

The laser Doppler (LD) effect describes the difference in frequency–the Doppler Shift–between the incident light and its scattered parts from moving particles. This work aims to provide a circuit-level analysis on how LDI imposes a distinctively different set of noise requirements compared to general purpose imaging. Quantitative conclusions will be drawn on how ADC resolution and correlated-double-sampling (CDS) can impact on LDI instrumentation precision. A compact body-biased PMOS reset pixel is proposed for reducing reset-noise without CDS. A compact time-domain noise-averaging comparator is also developed to satisfy the ADC resolution requirements of LDI while enjoying the energy efficiency of the SAR architecture.

The CMOS LDI sensor depicted in Fig. 1(a) is composed of a 128x128 pixel array and 13 column parallel high-resolution SAR ADCs. Each ADC is shared between 16 neighboring pixel columns via transfer-gate multiplexers. The output of the source follower is sampled by the 16b SAR ADC which generates 19 bits of datafor each sample.

The schematic of the 16b SAR ADC is shown in Fig. 1(b). Its sub-radix-2 digital-to-analog converter (DAC) with 19 weights is split into 3 sections. The unit capacitor is a 28 fF MIM capacitor. During the sampling phase, the bottom-plates of all capacitors in the negative DAC, DAC_n, except for the MSB capacitor is connected to while their top-plates sample the input signal, V_{sig}. Meanwhile, the top-plates of all capacitors in the positive DAC, DAC_p, except for the MSB capacitor is connected to GND while their bottom-plates sample V_{sig}. As a result, the DC bias of the comparator input is determined by K, simplifying the comparator design. V_{sig} can also have an inherent 2x voltage gain through the sampling process. The chip micrograph is shown in Fig. 1(c). It is measured using phantom serum with results matching the expected theoretical values. It has the lowest FoM amonst published works making it suitable for future mobile LDI applications.

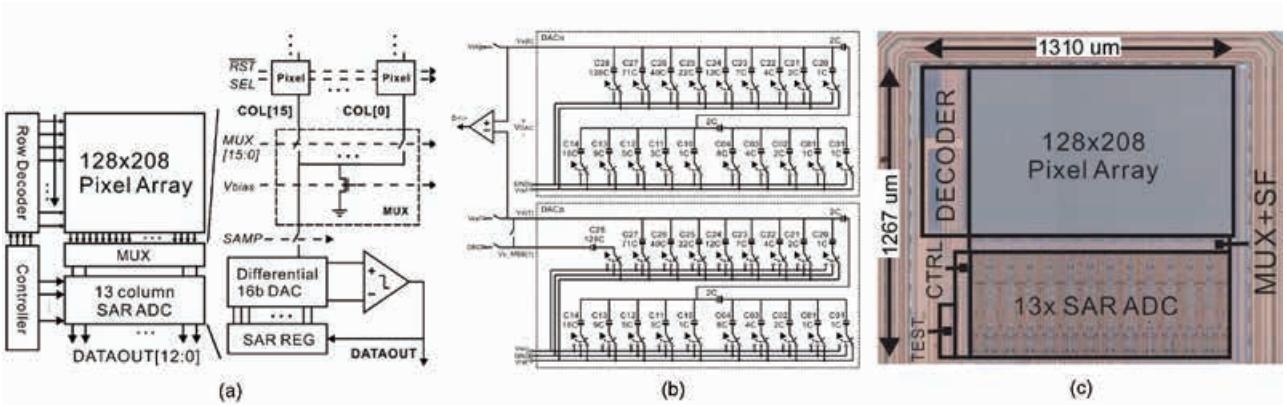


Fig. 1. (a) Block diagram of the LDI sensor chip and its column circuit from pixel to source follower to SAR ADC. (b) Schematic of the sub-radix-2 16b SAR ADC. (c) Prototype LDI sensor.

Publication(s):

[1] D. G. Chen, M.-K. Law*, Y. Lian and A. Bermak, "Low-power CMOS Laser Doppler Imaging using Non-CDS Pixel Readout and 13.6-bit SAR ADC," IEEE Trans. Biomed. Circuits Syst., vol. 10, no. 1, pp. 186-199, Feb. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong Research Grant Council

A 1.1 µW CMOS Smart Temperature Sensor with an Inaccuracy of ±0.2°C (3σ) for Clinical Temperature Monitoring

Man-Kay Law, Sanfeng Lu, Tao Wu, Amine Bermak, Pui-In Mak, and Rui P. Martins

FEATURES

Multi-ratio pre-gain stage
Block-based data weighted averaging (BDWA)
High accuracy, ±0.2°C(3σ) from 25 to 45 °C
Area-efficient SAR-SS hybrid ADC
Ultra-low power consumption
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

In this work, a CMOS temperature sensor is designed with high accuracy and ultra-low power consumption especially suitable for passively-powered clinical temperature monitoring applications where the human body temperature can be readily measured non-invasively. A multi-ratio pre-gain stage is proposed to relax the resolution requirement of the I-ADC by optimizing its input range utilization. BDWA is also proposed to alleviate the capacitor mismatch error while effectively relaxing the control overhead.

Fig. 1 (a,b) shows the block diagram of the conventional and proposed smart temperature sensor. We propose to integrate a multi-ratio pre-gain stage (k_{1-4}) to amplify the temperature signal while providing an offset to prevent integrator saturation under low voltage operation. This also relaxes the I-ADC requirement as only a moderate resolution is required (e.g. 12-bit for 0.1°C). The output bit-stream bs is then fedback for pre-gain update as well as processed by the off-chip digital filter to obtain the ratiometric output µ'.

BDWA is proposed to achieve multi-ratios with high accuracy while significantly reducing the routing cost. The key idea is to group a maximum number of unit capacitors into blocks while still providing the flexibility offered by the DWA. In this work, the number of control lines required is significantly reduced to 24, which is 4.8x less than that required for the conventional DWA.

This proposed smart temperature sensor is implemented in a standard 0.18µm CMOS process, occupying an active area of 0.198 mm². The sensor dissipates a measured power of 1.1 µW at 37°C with a conversion rate of 2 Sa/s. Measurement results show that an inaccuracy of ±0.1 °C (3 σ) is obtained from 37°C to 39°C (±0.2°C from 25°C to 45°C), demonstrating its suitability in human body temperature monitoring applications.

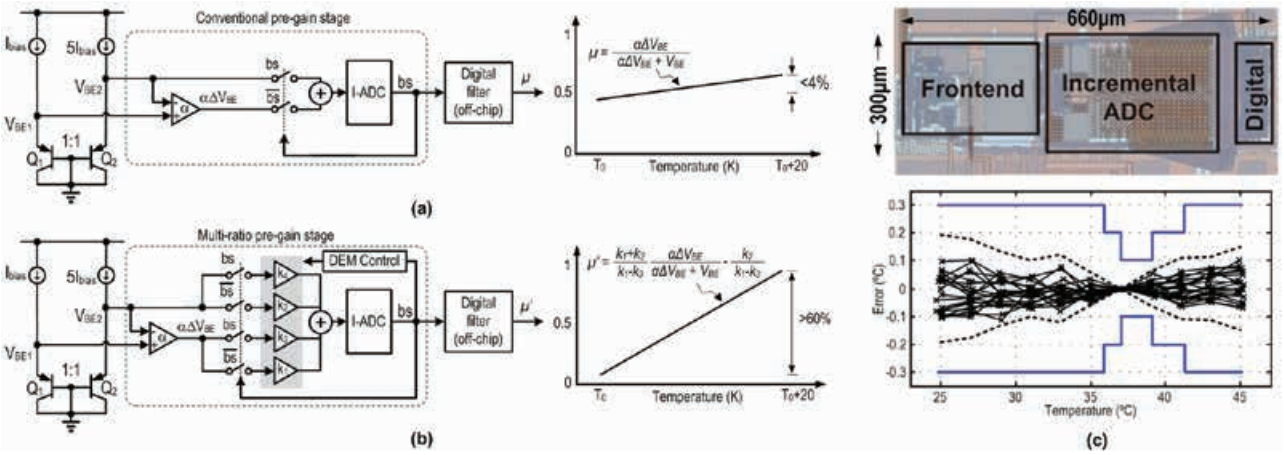


Fig. 1. (a) Block diagram of the conventional gain stage. (b) Block diagram of the proposed multi-ratio pre-gain stage. (c) Chip micro-graph (top) and measured inaccuracy from 20 chips samples after one-point calibration at 37°C, with bold dashed lines indicating the ±3σ values and blue solid lines showing the accuracy requirement.

Publication(s):

[1] M.-K. Law, S. Lu, T. Wu, A. Bermak, P.-I. Mak, and R. P. Martins, "A 1.1 µW CMOS Smart Temperature Sensor with an Inaccuracy of ±0.2oC (3σ) for Clinical Temperature Monitoring," IEEE Sensors J., vol. 16, no. 8, pp. 2272-2281, Feb. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Adaptive On/Off Delay-Compensated Active Rectifiers for Wireless Power Transfer Systems

Lin Cheng, Wing-Hung Ki, Yan Lu, and Tak-Sang Yim

FEATURES

Adaptive loops for reverse current control
ISM band frequency, 13.56MHz
Peak output power, 64.8mW
Peak efficiency, 91.4%
Silicon verified in AMS 0.35μm CMOS process

DESCRIPTION

An adaptive on/off delay-compensation technique is proposed to improve the performance of CMOS active rectifiers for wireless power transfer (WPT) systems. The effects of the on/off delays on the performance of the active rectifiers with either a parallel-resonant or a series-resonant circuit at the secondary coil are studied, which include power conversion efficiency (PCE), voltage conversion ratio (VCR) and output voltage ripple. By adding two feedback loops to the active diodes to generate the switched-offset currents for the comparators adaptively, both on- and off-delays are compensated for accurately against PVT variations and mismatches.

As a design example, a fully integrated active rectifier for biomedical applications with a parallel-resonant secondary was fabricated in a standard 0.35 μm CMOS process. With an AC input that ranges from 1.8 to 3.6 V, the measured VCR is higher than 90% and the measured PCE is higher than 89.1% for a load resistor of 500 Ω. In particular, the PCE is increased by 9% compared to the active rectifier without using the proposed technique.

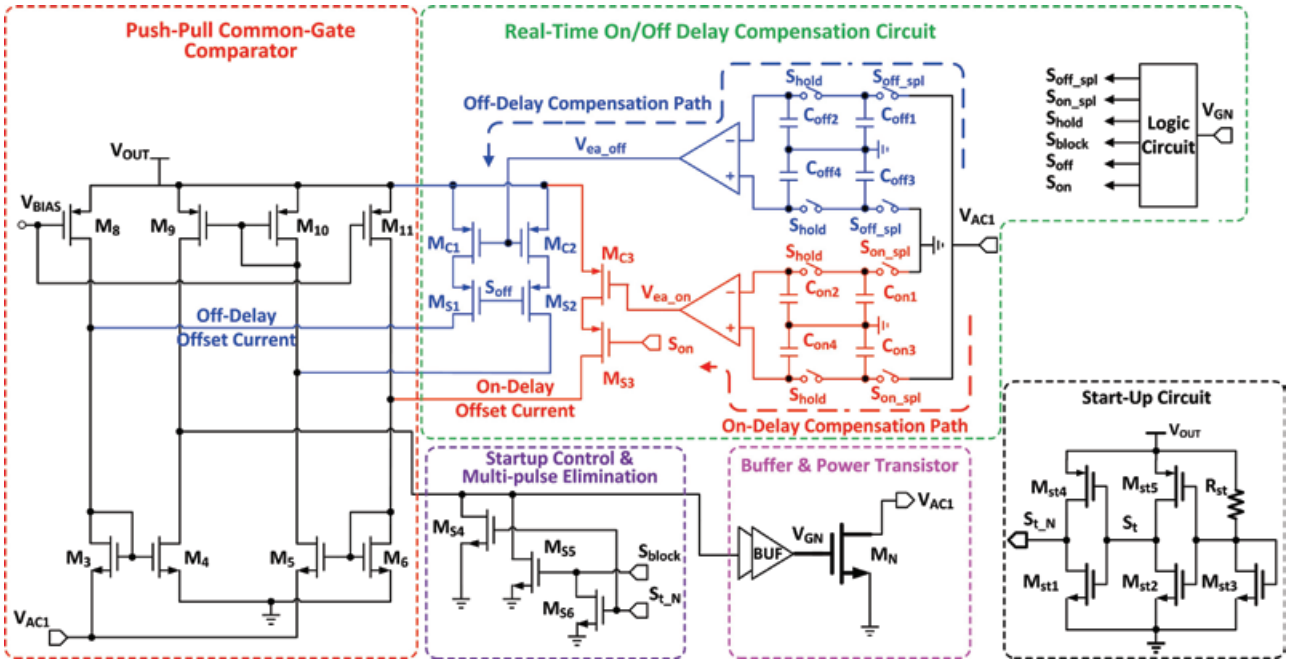


Fig. 1. Schematic of the active diode with the proposed adaptive on/off delay-compensation technique.

Publication(s):

[1] L. Cheng, W. H. Ki, Y. Lu*, and T. S. Yim, "Adaptive On/Off Delay-Compensated Active Rectifiers for Wireless Power Transfer Systems," IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 712–723, Mar. 2016.

* Contributors with University of Macau

Sponsorship:

N/A

A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes with a 67% Charge Pump Maximum Efficiency

Zhiyuan Chen, Man-Kay Law, Pui-In Mak, and Rui P. Martins

FEATURES

Solar energy harvesting IC with on-chip solar cell
Photodiode-assisted dual startup circuit (PDSC)
Auxiliary charge pump
Charge pump and solar cell area optimization
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

Solar energy harvesting has been recently demonstrated as a viable solution in applications including intraocular pressure monitoring and subdermal implant applications. Yet, the feasibility and co-optimization of a single-chip solar energy harvesting solution, that can boost the harvested voltage while achieving a high efficiency suitable for implantable applications, is yet to be demonstrated. We propose a single-chip solar energy harvesting system using a 3-stage integrated charge pump with on-chip photodiodes. An output power in the μW level is targeted for subdermal implant applications, where the key challenge is to achieve high energy efficiency at ultra-low power levels and in a small volume.

Fig. 1 shows the application scenario of a typical subdermal implant. This work focuses on the power management unit. The solar cell harvests the incoming solar energy and provides power to the other building blocks as well as to the load. To prevent noise coupling between modules, the solar cell is divided into three sub-blocks D_M, D_P and D_R to provide energy to the main/auxiliary charge pump, clock phase generator and voltage reference, respectively. The voltage reference generates a reference voltage V_{ref} for biasing the clock phase generator. PDSC is proposed to improve the voltage reference startup time while imposing minimum overhead. The clock phase generator provides a two-phase non-overlapping clock to the AQP and LCs using a 5-stage ring oscillator with body-biasing. An AQP is utilized to generate an auxiliary supply voltage V_{aux} to LC1 to ensure a low startup voltage while minimizing the reversion loss. High swing clock phases are utilized for improved conduction loss in the main charge pump.

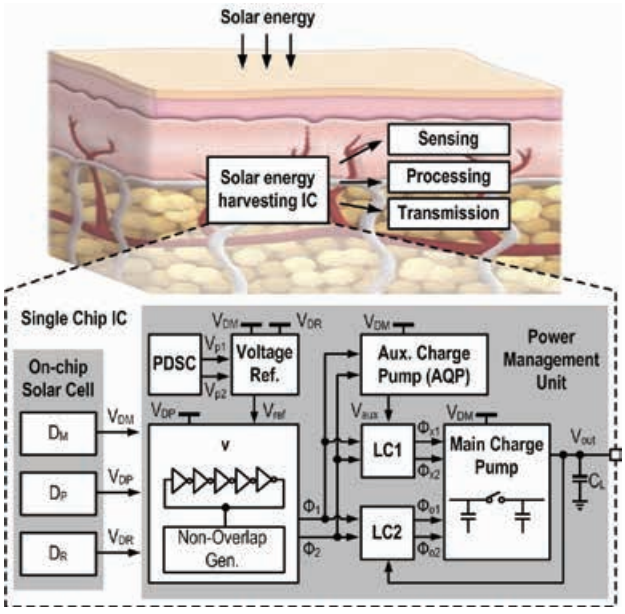


Fig. 1. Overview of the proposed single chip solar energy harvesting system.

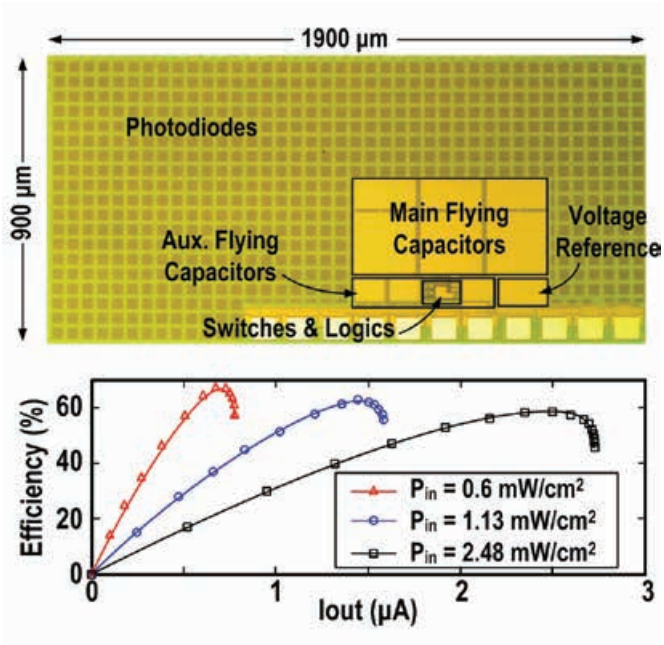


Fig. 2. Chip micrograph (top) and measured efficiency under different incident power levels (bottom).

Publication(s):

[1] Z. Chen, M.-K. Law, P.-I. Mak, and R. P. Martins, "A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes with a 67% Charge Pump Maximum Efficiency," IEEE Trans. Biomed. Circuits Syst., vol. 11, no. 1, pp. 44-53, Feb. 2017.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Reconfigurable Bidirectional Wireless Power Transceiver

Mo Huang, Yan Lu, Seng-Pan U, and Rui P. Martins

FEATURES

Reconfigurable without additional hardware
Maximum current charging mode
ISM frequency band, 6.78MHz
Battery-to-battery efficiency, 58.6%
Maximum charging power, 1.65W
Silicon verified in AMS 0.35μm 5V CMOS

DESCRIPTION

Wireless power transfer (WPT) is currently on the critical point of an explosive growth. Here, as projected in Fig. 1, we propose a future WPT eco-system of consumer electronics, which includes three layers: 1) wireless charging pads being the fundamental energy plants that can charge a wireless power bank and mobile devices; 2) wireless power banks that get energy from plants and feed mobile devices; 3) power hungry mobile devices that get energy from all the other sources.

Since the power transistors occupy a large silicon area, and the differential Class-D power amplifier (PA) and the full-wave (FW) active rectifier have very similar symmetrical architectures, to enable the mobile devices charging others without additional hardware, we propose a reconfigurable bidirectional 6.78 MHz WPT transceiver (TRX) that reuses the LC resonant tank and 4 area consuming power transistors for the differential Class-D PA and the full-wave rectifier. With such WPTTRX embedded, one can provide a first-aid to his/her smart watch or friend's device of which the battery is dying.

Fig. 2 shows the chip microphotograph and the measurement setup. The system was measured with two identical chips and two identical coils.

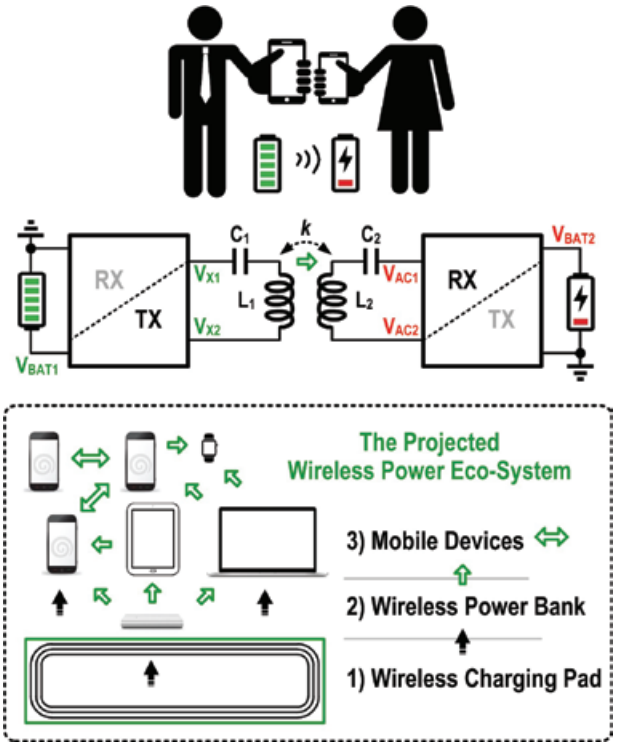


Fig. 1. The projected wireless power eco-system with mobile devices charging each other, enabled by the proposed reconfigurable bi-directional WPTTRX.

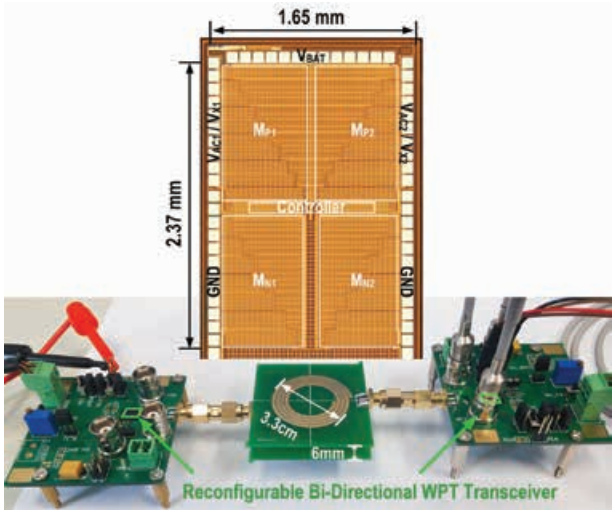


Fig. 2. Die micrograph and measurement setup of the reconfigurable bi-directional WPTTRX.

Publication(s):

[1] M. Huang, Y. Lu, S. P. U, and R. P. Martins, "A reconfigurable bidirectional wireless power transceiver with maximum-current charging mode and 58.6% battery-to-battery efficiency," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2017, pp. 376–377.

Sponsorship:

Research Committee of University of Macau, Macau Science and Technology Development Fund (FDCT)

A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting

Yan Lu, Haojuan Dai, Mo Huang, Man-Kay Law, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Dual-path RF energy harvesting
Wide input range, -16dBm to -5dBm
Silicon Verified in ST 65nm CMOS

DESCRIPTION

Energy harvesting has become increasingly important for a wide range of applications, including the wearable electronic devices, radio frequency identification (RFID), internet-of-things (IoT) and biomedical implanted devices. This work presents a dual-path CMOS rectifier with adaptive control for ultra-high frequency (UHF) RF energy harvesters. The input power range with high power convention efficiency (high-PCE) of the rectifier is extended by the proposed architecture which includes a low-power path and a high-power path.

The block diagram of the proposed rectifier is shown in Fig. 1. The dual-path rectifier consists of a low power path using LVTGP transistors for high-PCE at low input power and also for better input sensitivity, a high power path using LVTLP transistors designed for high-PCE at high input power, a reference path that generates a threshold voltage for the automatic path selection, and 3 switches S_1 through S_3 to enable/disable the low power path. Thus, the system can automatically choose the appropriate path according to the input power level to achieve a wider high-PCE range.

The dual-path rectifier with an adaptive control circuit is fabricated in a 65 nm CMOS process. Fig. 2 shows the chip micrograph of the proposed rectifier. The effective area excluding the pads is 250 × 190 μm². Operating at 900 MHz and driving a 147 kΩ load resistor, the measured PCE of this work can be maintained above 20% with an 11-dB input range from −16 dBm to −5 dBm, while only an 8 dB input range can be achieved with traditional single-path rectifiers. A sensitivity of −17.7 dBm is measured with 1 V output voltage across a capacitive load.

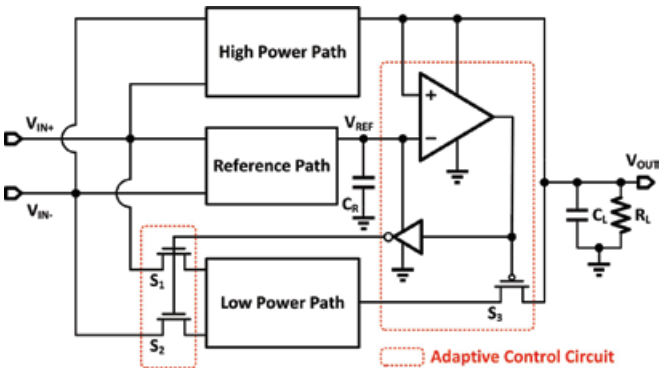


Fig. 1. System architecture of the dual-path rectifier.

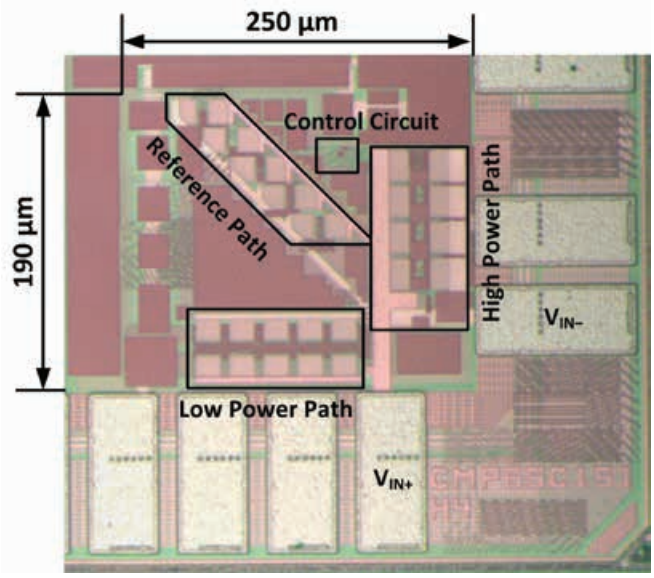


Fig. 2. Chip micrograph of the proposed dual-path rectifier.

Publication(s):

[1] Y. Lu et al., "A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 2, pp. 166-170, Feb. 2017.

Sponsorship:

Research Committee of University of Macau, Macau Science and Technology Development Fund (FDCT)

A Dual-Output Wireless Power Transfer System with Merged Active Rectifier and Three-Level Operation

Yan Lu, Mo Huang, Lin Cheng, Wing-Hung Ki, Seng-Pan U, and Rui P. Martins

FEATURES

Dual-output wireless power receiver
Three-level single-inductor dual-output operation
ISM frequency band, 6.78MHz
Maximum output power, 0.6W
Peak receiver efficiency, 80.5%
Silicon Verified in AMS 0.35μm 5V CMOS

DESCRIPTION

To cut the last wire of the electronic devices, this work presents a 6.78 MHz wireless power transfer (WPT) system for wirelessly powered flash drives that need multiple supplies with a total power of sub-1 W. A new architecture that merges an N-level single-inductor multiple-output switching converter with a multi-stage rectifier is proposed for the WPT receiver, and the regulated outputs attain small ripples. As shown in Fig. 1, the 3-level DC-DC and the SIMO techniques are merged with a 2X rectifier which readily has two DC supplies (3-level). When the V_{AC} amplitude is 3.2 V, V_{DC1} will be 2.7 V and V_{DC2} will be 5.5 V. The higher output voltage V_{O2} retrieves current from V_{DC2} and V_{DC1}, and can be programmed to range from 3.3 V to 5 V for I/O and memory circuits; and the lower output voltage V_{O1} retrieves current from V_{DC1} and Gnd, and can be ranged from 1.0 V to 1.8 V for core circuits. The SIMO converter switches at the WPT frequency of 6.78 MHz.

One benefit of operating the DC-DC converter at the WPT frequency is that, part of the discontinuous rectifier output currents will directly go to the DC-DC converter inputs in every half cycle, bypassing the rectifier load capacitors C_{DC1} and C_{DC2}, thus further reduces the output ripple.

The WPT system was fabricated in a 0.35 μm CMOS process using both 5 V and 3 V devices, and it was measured with the PCB coils shown in Fig. 2. A transmitter (TX) chip consists of a single-ended Class-D power amplifier driving a series LC resonant tank at 6.78 MHz was also fabricated for testing.

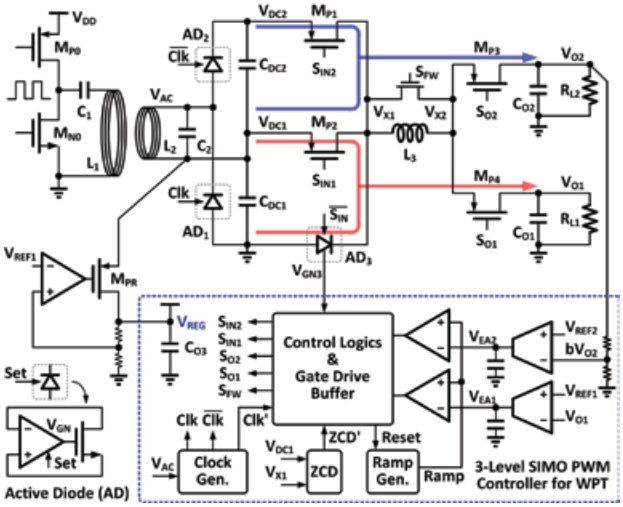


Fig. 1. WPT system with 2X rectifier and three-level SIMO converter.

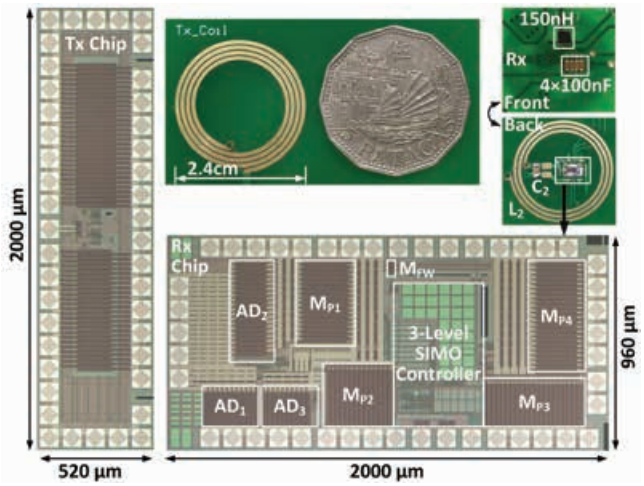


Fig. 2. Chip micrographs and off-chip components of the proposed system.

Publication(s):

[1] Y. Lu*, M. Huang*, L. Cheng, W. H. Ki, S. P. U*, and R. P. Martins*, "A Dual-Output Wireless Power Transfer System With Active Rectifier and Three-Level Operation," IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 927–930, Feb. 2017.

* Contributors with University of Macau

Sponsorship:

Research Committee of University of Macau, Macau Science and Technology Development Fund (FDCT)

RESEARCH ABSTRACTS
LAB-ON-A-CHIP

An Intelligent Digital Microfluidic System with Fuzzy-Enhanced Feedback for Multi-Droplet Manipulation

Jie Gao, Xianming Liu, Tianlan Chen, Pui-In Mak, Yuguang Du, Mang-I Vai, Bingcheng Lin, and Rui P. Martins

FEATURES

Control-engaged droplet manageability
Profiling ability of different droplet's hydrodynamics
Fuzzy-enhanced control saving 21% charging time
Expert manipulability of multi-droplet routings

DESCRIPTION

The electrowetting-on-dielectric (EWOD) behavior of microdroplets, under variable-charged surface electrodes, has inspired the development of digital microfluidic (DMF) systems for large-scale micro-reactors, which have underpinned a wide variety of chemical or biological applications in tiny droplet volumes e.g., molecular probe synthesis, proteomics, immunoassays, enzyme assays, clinical diagnostics, DNA sample processing and cell-based assays.

This work is an intelligent DMF technology to address the complexity of droplet hydrodynamics on a digital microfluidic (DMF) system. A wide variety of control-engaged droplet manageability is proposed and demonstrated through the operation of our modular DMF prototype, which comprises: (i) rigid profiling ability of different droplet's hydrodynamics under a real-time trajectory track of droplet-derived capacitance, permitting accurate and autonomous multi-droplet positioning without visual setup and heavy image signal processing; (ii) fuzzy-enhanced controllability saving up to 21% charging time when compared with the classical approach, enhancing the throughput, fidelity and lifetime of the DMF chip, while identifying and renouncing those weakened electrodes deteriorated over time, and (iii) expert manipulability of multi-droplet routings under counter-measure decisions in real time, preventing droplet-to-droplet or task-to-task interference. Altogether, this work exhibits the first modular DMF system with built-in electronic-control software-defined intelligence to enhance the fidelity and reliability of each droplet operation, allowing future manufacturability of a wide range of life science analyses and combinatorial chemical screening applications.

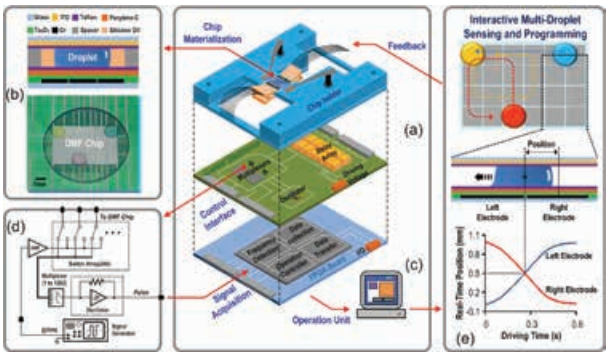


Fig. 1. Scheme of Kth stage of the proposed binary-search ADC.

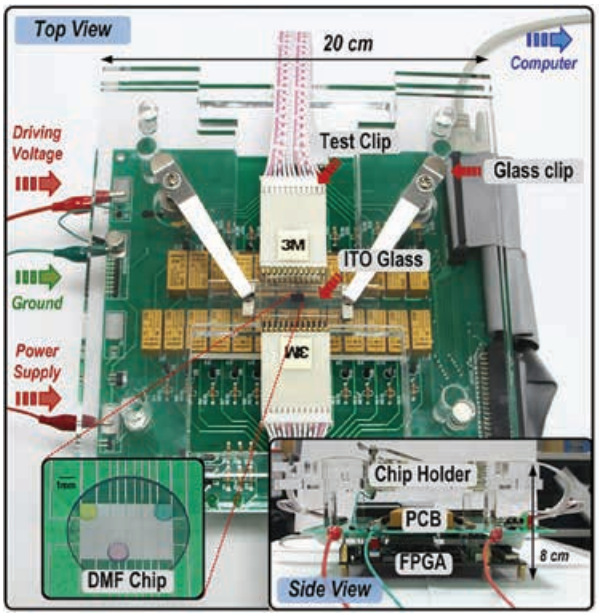


Fig. 2. Chip Photograph.

Publication(s):

[1] J. Gao*, X. Liu, T. Chen*, P.-I. Mak*, Y. Du, M.-I Vai*, B. Lin and R. P. Martins*, "An Intelligent Digital Microfluidic System with Fuzzy-Enhanced Feedback for Multi-Droplet Manipulation," Lab on a Chip, 2013, 13, 443-451.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Construction of a Microfluidic Chip, Using Dried-Down Reagents, for LATE-PCR Amplification and Detection of Single-Stranded DNA

Yanwei Jia, Pui-In Mak, Conner Massey, Rui P. Martins, and Lawrence J. Wangh

FEATURES

Microfluidic system
On-chip LATE-PCR
Single copy DNA detection
Multiplex PCR on-chip
Dried-down PCR reagents on-chip
Easy storage and transportation

DESCRIPTION

LATE-PCR is an advanced form of non-symmetric PCR that efficiently generates single-stranded DNA which can readily be characterized at the end of amplification by hybridization to low-temperature fluorescent probes. We demonstrate here for the first time that monoplex and duplex LATE-PCR amplification and probe target hybridization can be carried out in double layered PDMS microfluidics chips containing dried reagents.

Addition of a set of reagents during dry down overcomes the common problem of single-stranded oligonucleotide binding to PDMS. These proof-of-principle results open the way to construction of inexpensive point-of-care devices that take full advantage of the analytical power of assays built using LATE-PCR and low-temperature probes.

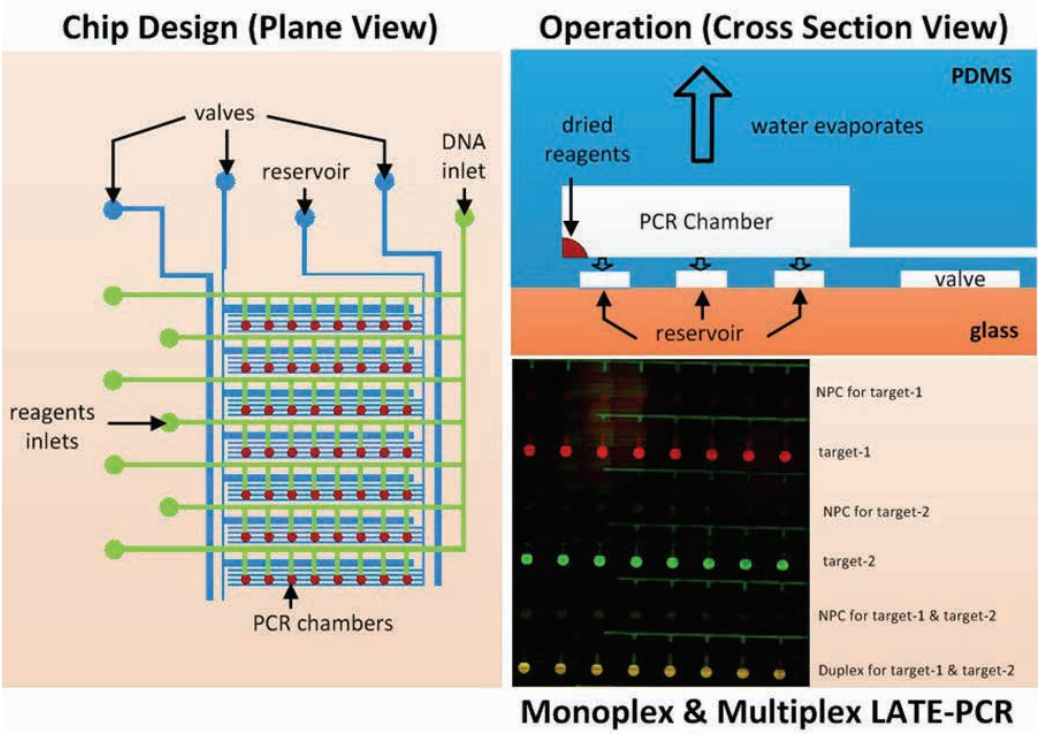


Fig. 1. preloading all of the reagents required for on-chip LATE-PCR amplification and detection of monoplex and multiplex single-stranded DNA products.

Publication(s):

[1] Y. W. Jia*, P. I. Mak*, C. Massey, R. P. Martins* and L. J. Wangh, "Construction of a Microfluidic Chip for LATE-PCR Amplification and Detection of Single-Stranded DNA using Dried-Down Reagents," Lab on a Chip, 13, 4635-4641, 2013.

* Affiliated with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Natural Discharge After Pulse and Cooperative Electrodes to Enhance Droplet Velocity in Digital Microfluidics

Tianlan Chen, Cheng Dong, Jie Gao, Yanwei Jia, Pui-In Mak, Mang-I Vai, and Rui P. Martins

FEATURES

Digital microfluidic system
Natural discharge after pulse
Cooperative electrodes charging
Droplet movement dynamics
Droplet actuation signal investigation

DESCRIPTION

Digital Microfluidics (DMF) is a promising technology for biological/chemical micro-reactions due to its distinct droplet manageability via electronic automation, but the limited velocity of droplet transportation has hindered DMF from utilization in high throughput applications.

In this paper, by adaptively fitting the actuation voltages to the dynamic motions of droplet movement under real-time feedback monitoring, two control-engaged electrode-driving techniques: Natural Discharge after Pulse (NDAP) and Cooperative Electrodes (CE) are proposed. They together lead to, for the first time, enhanced droplet velocity with lower root mean square voltage value.

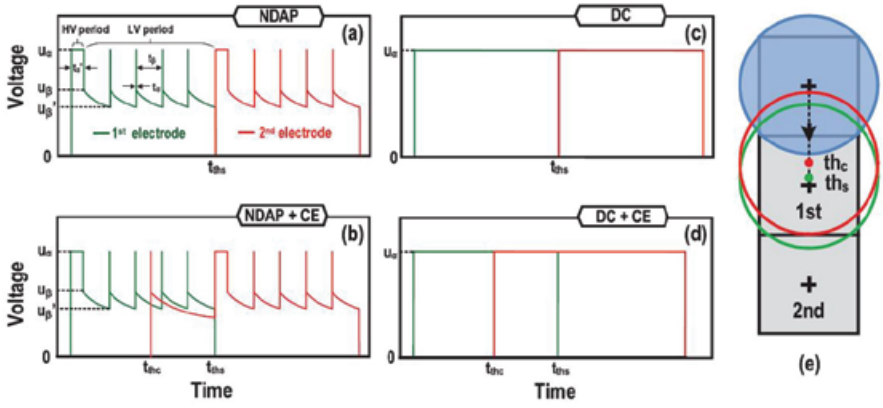


Fig. 1. Sketches of four possible electrode-driving schemes for droplet movements over two electrodes: (a)Natural Discharge after Pulse (NDAP): The high-voltage (HV) period lasts shorter, while the low-voltage (LV) under natural discharge lasts longer with short pulse recharging periodically. (b) DC signal. (c) NDAP with cooperative electrodes (CE) overlaps the charging time of neighboring electrodes. (d) DC plus CE driving. (e) Droplet moving toward two target electrodes and location of the two thresholds on the first target electrode.

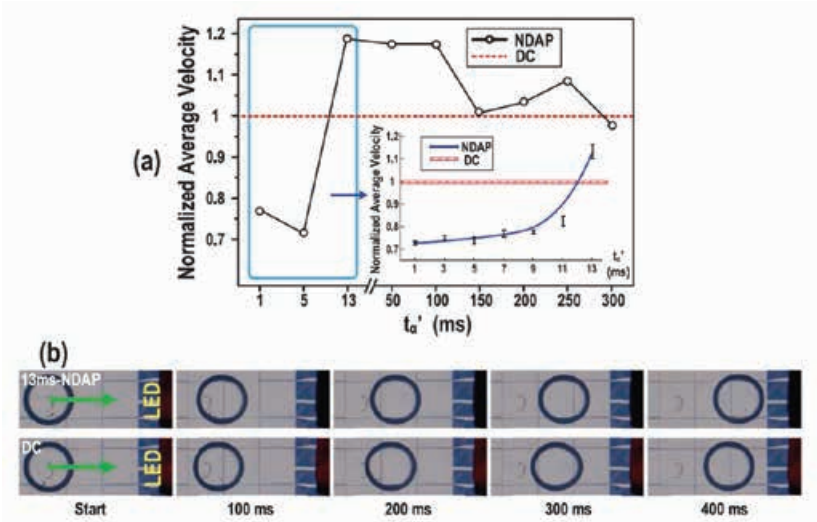


Fig. 2. (a) Normalized average velocity of a droplet under NDAP signals with different t_a and DC. Inserted curve shows the droplet velocities with t_a < 13 ms. The data were normalized at the average velocity under DC. (b) Video frames of a droplet actuated by NDAP and DC crossing 2 electrodes.

Publication(s):

[1] T. L. Chen, C. Dong, J. Gao, Y. W. Jia, P. I. Mak, M. I., Vai and R. P. Martins, "Natural discharge after pulse and cooperative electrodes to enhance droplet velocity in digital microfluidic," AIP Advances, 4, 047129, 2014.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Adhesion Promoter for a Multi-Dielectric-Layer on a Digital Microfluidic Chip

Jie Gao, Tianlan Chen, Cheng Dong, Yanwei Jia, Pui-In Mak, Mang-I. Vai, and Rui P. Martins

FEATURES

Digital microfluidic system
Multi-dielectric layer
Adhesion promoter
Low droplet actuation voltage, 5 V

DESCRIPTION

A silane-based adhesion promoter suitable for a multi-di-electric-layer coating on a digital microfluidic chip is reported. It measures >100 improvement in chip lifetime via transforming the bonding of the dielectric layers (Ta2O5 and Parylene C) from nonspecific to chemical.

The refined chip-fabrication protocol also allows low EWOD actuation voltages down to 5 V. Put some general descriptions here. Please keep in mind that the main targets of this AMSV research report is the researchers and engineers in our field.

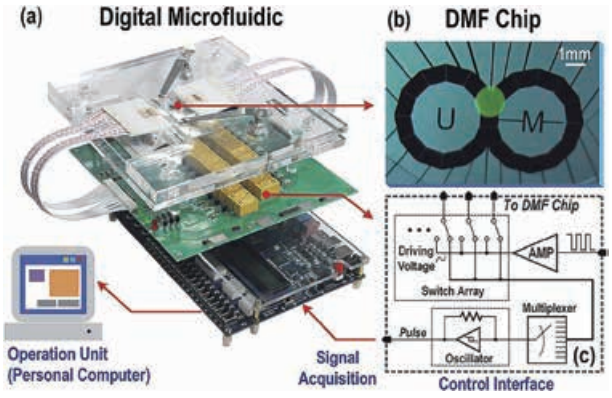


Fig. 1. Setup of the control-engaged DMF system.

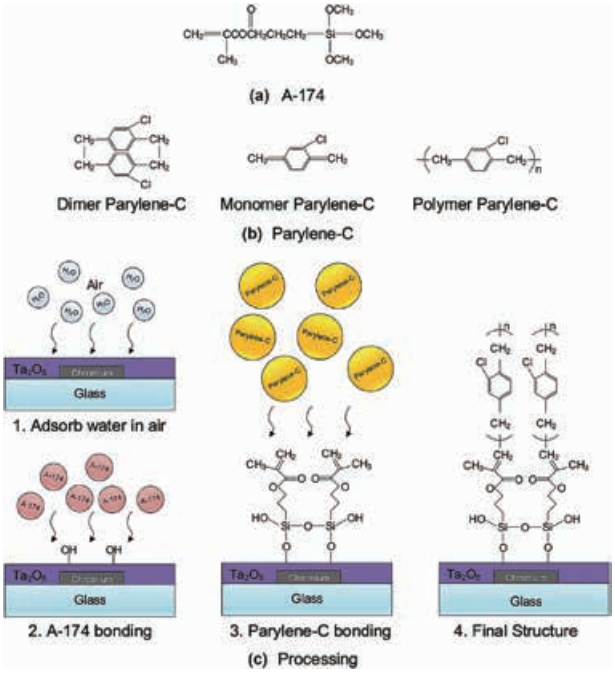


Fig. 2. Schematics of A-174 promoting adhesion between Ta2O5 and Parylene C.

Publication(s):

[1] J. Gao, T. L. Chen, C. Dong, Y. W. Jia, P. I. Mak, M. I. Vai, and R. P. Martins, "Adhesion Promoter for Multi-dielectric-layer on digital microfluidic chip," RSC Advances, 5, 48626-48630, 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

On the Droplet Vvelocity and Electrode Lifetime of Digital Microfluidics: Voltage Actuation Techniques and Comparison

Cheng Dong, Tianlan Chen, Jie Gao, Yanwei Jia, Pui-In Mak, Mang-I Vai, and Rui P. Martins

FEATURES

Digital microfluidic system
Improved droplet transportation velocity
Elongated electrode lifetime
Natural discharge after pulse
Actuation signal comparison

DESCRIPTION

The distinct manageability of digital microfluidics (DMF) has rendered it a promising platform for building large-scale micro-reactors on a single chip for closed-loop automation. However, the limited velocity of the droplet transportation has hindered DMF from being utilized in high-throughput applications. This work investigates a control-engaged droplet actuation technique involving regular electronic hardware and computer-based software to simultaneously raise the velocity of the droplet transportation and elongate the electrode lifetime by lowering the root-mean-square value of the actuation voltage. The technique is based on a series of direct current (DC) pulses and multi-cycles of natural discharge coordinated with the droplet dynamic motions, facilitating realtime droplet position sensing.

We found that the proposed technique was superior to both DC and AC in terms of the velocity. As to the electrode lifetime, all showed excellent performance under normal dielectric coating conditions, while AC (alternating current) performed the best under critical conditions. Altogether, this work exhibits a control-engaged electrode-driving scheme with a higher velocity and a longer lifetime compared with traditional DC actuation and for the first time provides a fundamental comparison among the techniques engaging different actuation signals.

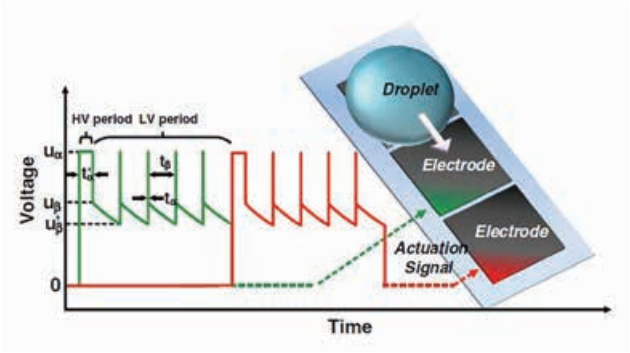


Fig. 1. Profiles of the electrode-driving signal, Natural Discharge after Pulse (NDAP), for a droplet moving across two electrodes. The high-voltage uα (HV) period lasts a period of t′. The low-voltage (LV) period includes multi-cycles of natural discharges (tβ) and DCpulse (tα). uβ is the instantly decreased voltage when disconnecting an electrode. u′ is the lowest voltage to maintain the movement of a droplet.

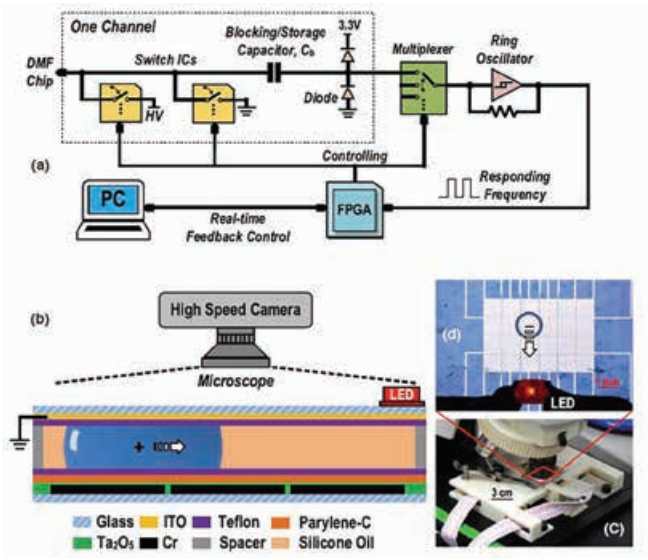


Fig. 2. Experimental setup for measuring the droplet dynamics under different electrode-driving signals.

Publication(s):

[1] C. Dong, T. L. Chen, J. Gao. Y. W. Jia. P. I. Mak, M. I. Vai and R. P. Martins, "On the droplet velocity and electrode lifetime of digital microfluidics: voltage actuation techniques and comparison," Microfluidics and Nanofluidics, 18, 673-683, 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Sub-7-Second Genotyping of Single-Nucleotide Polymorphism by High-Resolution Melting Curve Analysis on a Thermal Digital Microfluidic Device

Tianlan Chen, Yanwei Jia, Cheng Dong, Jie Gao, Pui-In Mak, Rui P. Martins

FEATURES

Digital microfluidic system
Ultrafast DNA melting curve analysis, 7 second
High resolution, single nucleotide discrimination

DESCRIPTION

We developed a thermal digital microfluidic (T-DMF) device enabling ultrafast DNA melting curve analysis (MCA). Within 7 seconds, the T-DMF device succeeds in differentiating a melting point difference down to 1.6 °C with a variation of 0.3 °C in a tiny droplet sample (1.2 μL), which represents 300 times faster, and 20 times less sample spending, than the standard MCA (35 minutes, 25 μL) run in a commercial qPCR machine. Such a performance makes it possible for a rapid discrimination of single nucleotide mutation, relevant to prompt clinical decision-making. Also, aided by electronic intelligent control, the TDMF device facilitates sample handling and pipelining in an automatic serial manner.

An optimized oval-shaped thermal electrode is introduced to achieve high thermal uniformity. A device-sealing technique averts sample contamination and permits uninterrupted chemical/biological reactions. Simple fabrication using a single chromium layer fulfills both the thermal and typical transport electrodes. Capable of thermally-modulating DNA samples with ultrafast MCA, this T-DMF device has the potential for a wide variety of life science analyses, especially for disease diagnosis and prognosis.

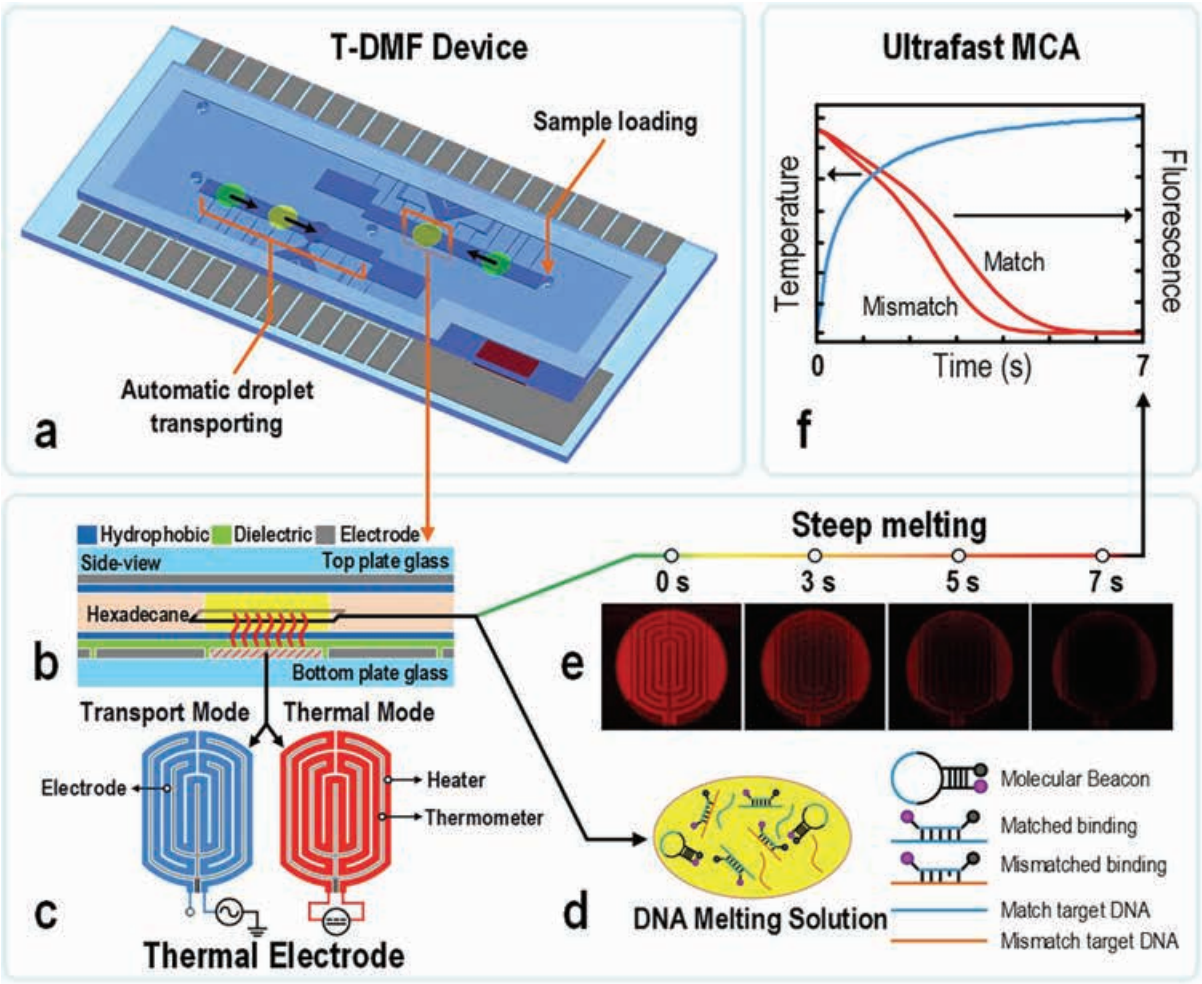


Fig. 1. Thermal digital microfluidic (T-DMF) device for ultrafast DNA melting curve analysis (MCA).

Publication(s):

[1] T. L. Chen, Y. W. Jia, C. Dong, J. Gao, P. I. Mak, and R. P. Martins, "Sub-7-second genotyping of single-nucleotide polymorphism by high-resolution melting curve analysis on a thermal digital microfluidic device," Lab on a Chip, 16, 743-752, 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A μNMR CMOS Transceiver Using a Butterfly-Coil Input for Integration with a Digital Microfluidic Device inside a Portable Magnet

Ka-Meng Lei, Pui-In Mak, Man-Kay Law, and Rui P. Martins

FEATURES

Co-integration of microelectronics (0.18-μm process) and digital microfluidics technologies.
Multi-sample manipulation
(and chemical/biological sensing)
inside portable magnet (1.2 kg, 0.46 Tesla).
Cross-domain optimized Butterfly-coil to expand the effective electrodes.
Flexible route projection and optimization.

DESCRIPTION

There is demand to develop a "Lab-on-a-Chip" device for in vitro diagnostic μNMR, which includes automated sample management capability. Lab-on-a-chip devices overcome miniaturization of healthcare diagnostic tools, allowing low-cost and rapid detection of specific targets in tiny fluid samples. This work reports the world-first electronic-automated μNMR relaxometer for multi-step multi-sample chemical/biological assays. Co-integration of microfluidic and microelectronic technologies allows association between droplet managements and μNMR assays inside a portable sub-Tesla magnet (1.2 kg, 0.5 Tesla). Targets in unprocessed biological samples, captured by specific probe-decorated magnetic nanoparticles, can be sequentially quantified by their spin-spin relaxation time (T_2) via multiplexed μNMR screening. A digital microfluidic device with capacitive sensing actuates and locates distinct droplet samples over the electrode arrays (15 electrodes, each 3.5 x 3.5 mm^2) in real time, and a Butterfly-coil-input 0.18-μm CMOS transceiver transduces between magnetic and electrical signals to/from a sub-10μ L droplet sample for μNMR screening. Auto-handling and identification of two biological samples with a pre-designed probe complete in 2.2 mins.

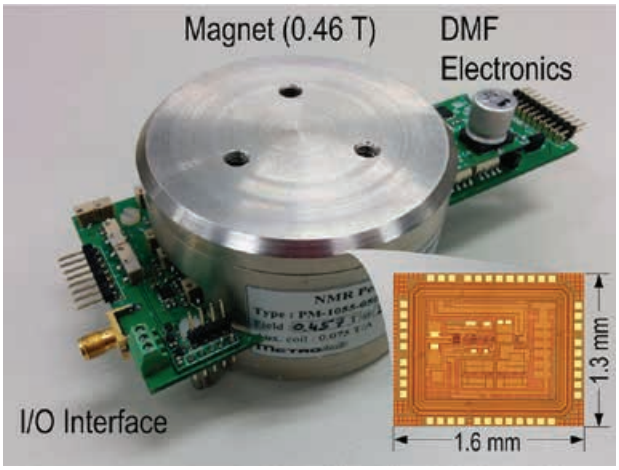


Fig. 1. The prototype of the platform and the fabricated CMOS NMR transceiver in 180nm process (inserted inside the magnet).

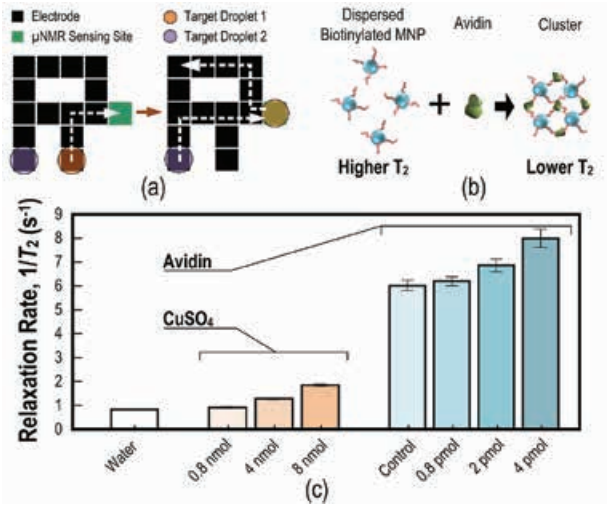


Fig. 2. (a) Multi-sample management scheme for the system. (b) Illustration of the sensing mechanism for avidin. (c) Relaxation rate ($1/T_2$) from various targets.

Publication(s):

[1] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A μNMR CMOS Transceiver Using a Butterfly-Coil Input for Integration with a Digital Microfluidic Device inside a Portable Magnet," IEEE J. Solid-State Circuits, vol. 51, no. 10, pp. 2274-2286, Oct. 2016.

[2] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A palm-size μNMR relaxometer using a digital microfluidic device and a semiconductor transceiver for chemical/biological diagnosis," Analyst, vol. 140, no.15, pp. 5129-5137, Aug. 2015.

[3] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A μNMR CMOS transceiver using a Butterfly-coil input for integration with a digital microfluidic device inside a portable magnet," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), pp. 1-4, Nov. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 3D Microblade Structure for Precise and Parallel Droplet Splitting on Digital Microfluidic Chips

Cheng Dong, Yanwei Jia, Jie Gao, Tianlan Chen, Pui-In Mak, Mang-I Vai, and Rui P. Martins

FEATURES

Digital microfluidic system
3D microblade structure
Precise droplet splitting
Multiple droplet generation with one-step splitting
Parallel DNA analysis
Sepsis pathogen detection

DESCRIPTION

Existing digital microfluidic (DMF) chips exploit the electrowetting on dielectric (EWOD) force to perform droplet splitting. However, the current splitting methods are not flexible and the volume of the droplets suffers from a large variation. Herein, we propose a DMF chip featuring a 3D microblade structure to enhance the droplet-splitting performance. By exploiting the EWOD force for shaping and manipulating the mother droplet, we obtain an average dividing error of <2% in the volume of the daughter droplets for a number of fluids such as deionized water, DNA solutions and DNA–protein mixtures.

Customized droplet splitting ratios of up to 20: 80 are achieved by positioning the blade at the appropriate position. Additionally, by fabricating multiple 3D micro-blades on one electrode, two to five uniform daughter droplets can be generated simultaneously. Finally, by taking synthetic DNA targets and their corresponding molecular beacon probes as a model system, multiple potential pathogens that cause sepsis are detected rapidly on the 3D-blade-equipped DMF chip, rendering it as a promising tool for parallel diagnosis of diseases.

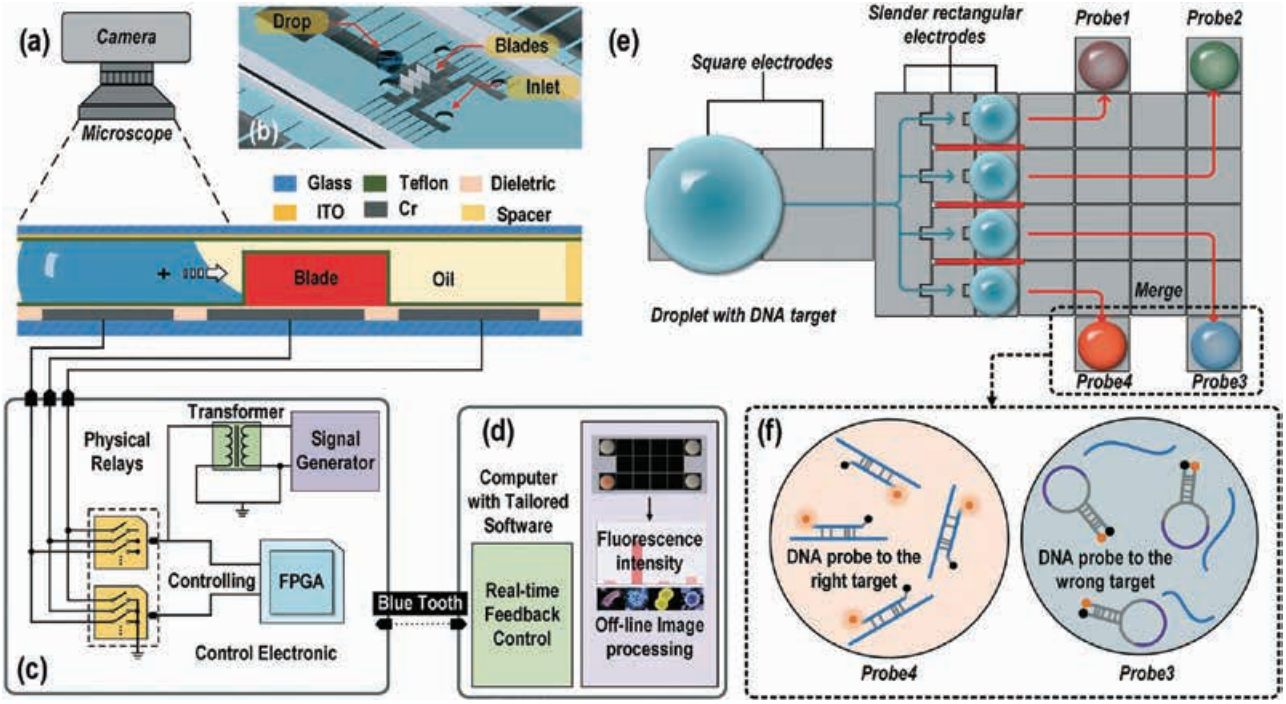


Fig. 1. Thermal digital microfluidic (T-DMF) device for ultrafast DNA melting curve analysis (MCA).

Publication(s):

[1] C. Dong, Y. W. Jia, J. Gao, T. L. Chen, P. I. Mak, M. I. Vai and R. P. Martins, A 3D microblade structure for precise and parallel droplet splitting on digital microfluidic chips, Lab on a Chip, 17, 896-904, 2017.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Handheld High-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays

Ka-Meng Lei, Hadi Heidari, Pui-In Mak, Man-Kay Law, Franco Maloberti, Rui P. Martins

FEATURES

First Micro-NMR CMOS Platform with close-loop magnetic field stabilization.
Handheld size platform powered by AA batteries for enhancing the portability.
Sensitive and selective biomolecule (protein and DNA) detection, down to 100pM of DNA from 2.5μL sample.

DESCRIPTION

Nuclear Magnetic Resonance (NMR) is promising for chemical and biological assays as it can reveal atomic level information and is quasi-label-free and washing-free for the samples. By integrating the transceiver and NMR sensing coil on CMOS chip, this micro-NMR platform can decrease the cost, volume, weight and sample consumption of the tool.

The CMOS transceiver can unify necessary electronic with minimal footprint. The transmitter programs pulses to perform NMR experiments while the receiver featured low-noise and low-distortion amplifies the NMR signal from the coil and downconvert it to baseband. The on-chip coil transduces between the magnetic signal of the nuclei and electrical signal of the transceiver. It reduces the sample consumption for the assays down to 2.5μL. This CMOS chip can significantly save the power and costs of NMR electronic.

A permanent NdFeB magnet is equipped to enhance the portability of the platform. To assure the robustness against temperature variation, a magnetic field stabilization module consisted of an on-chip vertical Hall sensor and current driver is entailed to soothe the temperature effect on the magnet. The hall sensor tracks the magnetic field variation and transduces the result, and the current driver feeds the corresponding current to the auxiliary coil of the magnet to stabilize the magnetic field at a certain level. This inspires the use of a simple crystal oscillator as LO and facilitates the electronics.

The micro-NMR platform is capable of detecting distinct bio-molecule selectively such as proteins and DNA with probe-decorated magnetic nanoparticles by analyzing the spin-spin relaxation time of the samples. For instance, with this micro-NMR platform, down to 100pM of E. faecalis derived DNA were detected from 2.5-μL sample.

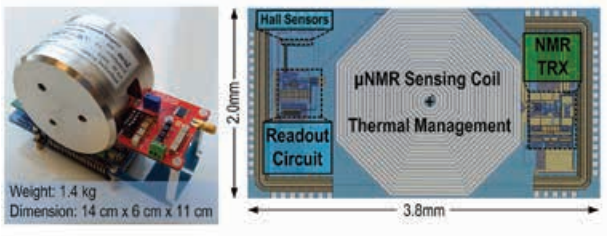


Fig. 1. The proposed NMR platform with magnetic field calibration and the chip micrograph.

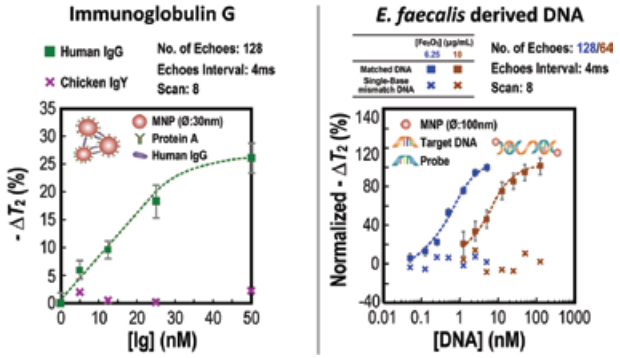


Fig. 2. Experimental results from the detection of Human IgG and synthesized DNA from E. faecalis.

Publication(s):

[1] K.-M. Lei*, H. Heidari, P.-I. Mak*, M.-K. Law*, F. Maloberti, and R. P. Martins*, "A handheld high-sensitivity micro-NMR CMOS platform with B-field stabilization for multi-type biological/chemical assays," IEEE J. Solid-State Circuits, vol. 52, no. 1, pp. 284-297, Jan. 2017.

[2] K.-M. Lei*, H. Heidari, P.-I. Mak*, M.-K. Law*, F. Maloberti, and R. P. Martins*, "A handheld 50pM-sensitivity micro-NMR CMOS platform with B-field stabilization for multi-type biological/chemical assays," in IEEE Int. Solid-State Circuits Conf. (ISSCC), 2016, pp. 474–475.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS
POWER MANAGEMENT AND CONDITIONING CIRCUITS

An Analog-Assisted Digital Low-Dropout Regulator with Tri-Loop Control

Mo Huang, Yan Lu, Seng-Pan U, and Rui P. Martins

FEATURES

Analog-assisted loop for instant transient response
Tri-loop control for reducing number of shift-registers
Output capacitor free
Freeze mode for low quiescent current, 3.2μA
Nonlinear coarse word control for glitch reduction
Silicon verified in TSMC 65nm GP CMOS

DESCRIPTION

Low-dropout regulators (LDOs) are widely distributed in SoC designs to supply individual voltage domains, and digital LDO (DLDO) is favorable for its low-voltage operation and process-scalability. However, as many SoCs generate a load current variation at sub-A/ns level, voltage regulators require a large area-consuming output capacitor (C_{OUT}) to maintain the output voltage (V_{OUT}) during fast transients. Conventional shift-register (SR) based DLDO suffers from a power and speed trade-off, thus requires a large C_{OUT}. Fig.1 shows the proposed AA technique in addition to the SR-based DLDO. The V_{SSB} nodes of the driving inverters of the power switches are not connected to Gnd as usual, but AC-coupled to V_{OUT} through a coupling capacitor C_C and DC-biased to Gnd with R_C. This forms an AA loop for bandwidth-extension and instant response.

Fig. 2 shows the overall architecture of the proposed AA-DLDO. A 9bit PMOS switch array is implemented for better V_{OUT} accuracy. This array is divided into 3 sub-sections (low, medium, and high) with carry-in/out between each other. These sub-sections are made of L, M, and H SR-bits respectively. A tri-loop control, including the 1) AA, 2) coarse- and 3) fine-tuning, is implemented. The driving inverters are sized proportionally to their corresponding switch strengths, and all the V_{SSB} nodes are AC-coupled to V_{OUT}. Besides, the coarse tuning is made by the medium and high SRs. The medium SR, triggered by a dead-zone comparator (DZ), outputs carry-in/out signals to drive the High SR. The fine tuning only composes of the low sub-section fed by a 1-bit quantization comparator (CMP). All these SRs are clock-gated for power loss reduction.

A nonlinear coarse word control for glitch reduction is also proposed, for details, please read the paper.

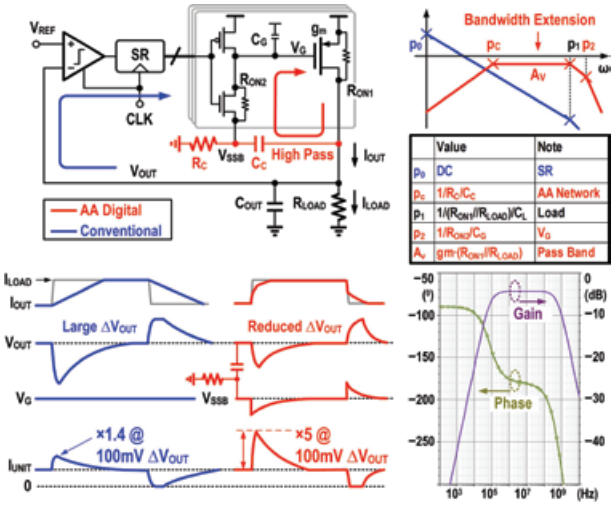


Fig. 1. AA-DLDO scheme and the poles of the AA loop; the transient waveforms of the AA and conventional schemes; and, the Bode plot of the AA loop.

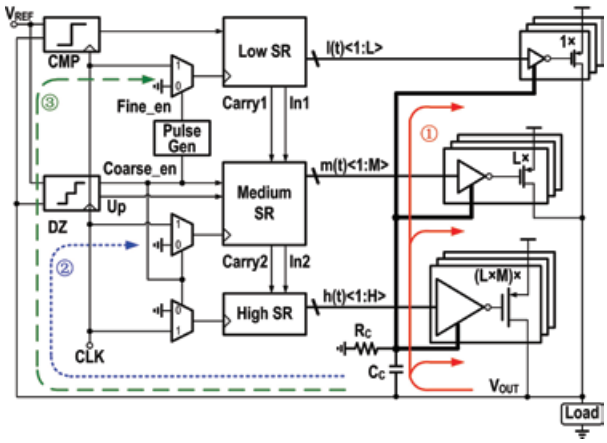


Fig. 2. Overall architecture of the proposed AA-DLDO, with the AA, coarse tuning, and fine tuning loops.

Publication(s):

[1] M. Huang, Y. Lu, S. P. U, and R. P. Martins, "An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control," in IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 342–343.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Dual-Symmetrical-Output Switched-Capacitor Converter with Dynamic Power Cells and Minimized Cross Regulation for Application Processors

Junmin Jiang, Yan Lu, Wing-Hung Ki, Seng-Pan U, and Rui P. Martins

FEATURES

Dual-symmetrical-output for reduced area overhead
Dynamic power cell reallocation for higher efficiency
Power density, 150mW/mm^2
Peak efficiency, 83.3%
Silicon verified in GF 28nm bulk CMOS

DESCRIPTION

Multi-core application processors in smart-phone/-watch require multiple voltages for each core. Highly-efficient fully integrated switched-capacitor (SC) converters that require zero external component, are promising candidates in these applications. Fig.1 shows the strategy of the shared power cells and dynamic allocation. The two outputs (V_{OUT1} and V_{OUT2}) are regulated by frequency modulation. So that the frequencies (f_1 and f_2) reflect the loading demands of each outputs. Assume the two channels start with the same no. of power cells, when the load of channel 1 (Ch1) is larger than that of channel 2 (Ch2), resulting $f_1 > f_2$, then more power cells will then be assigned to Ch1. That means the physical boundary of the two channels will go right, until f_1 and f_2 are close to each other. The dynamic allocation can balance the load demands by trying to operate at the optimized frequency with all the power cells, thus the switching and parasitic losses are reduced.

The number of power cells is designed to be 82 and work with interleaving-phase to reduce ripple. To enable the allocation with minimum the cross regulation, a dual-path VCO is proposed.

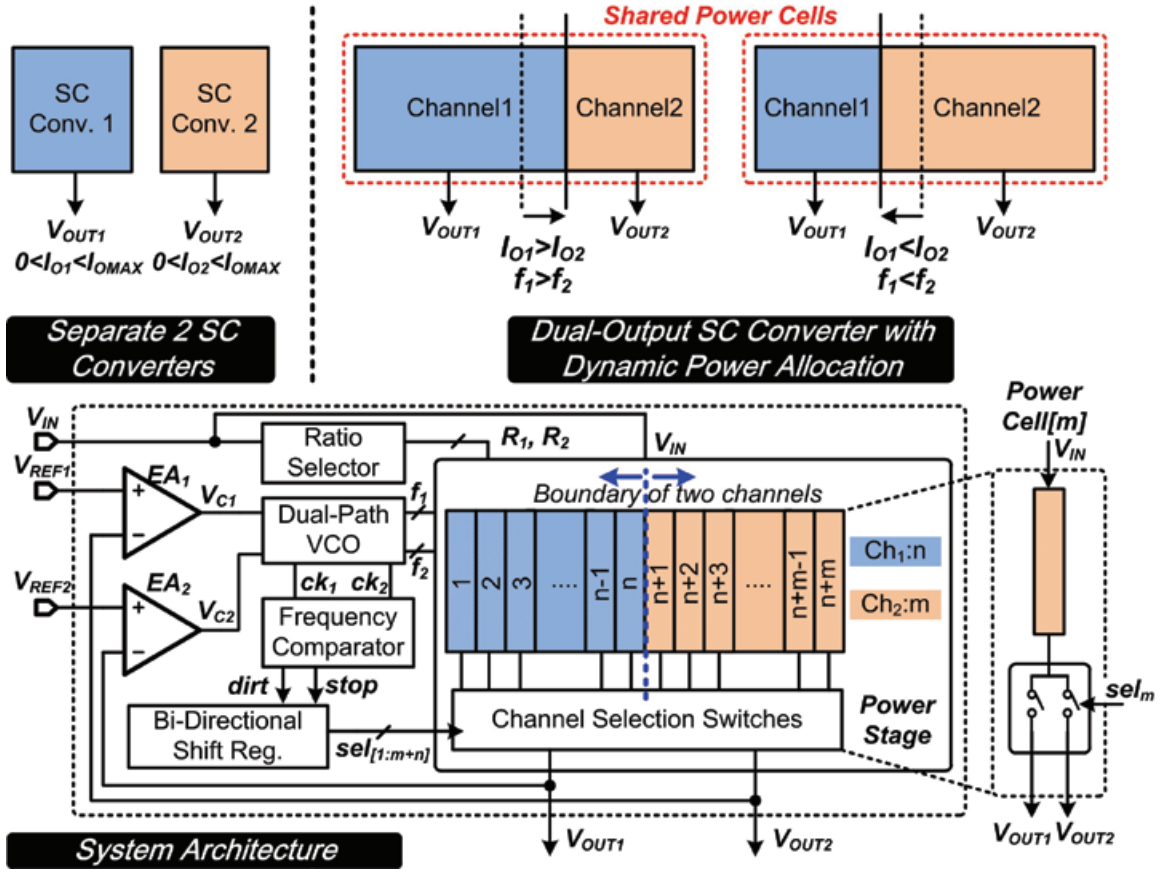


Fig. 1. Strategy of dynamic power-cell allocation and system architecture of proposed dual-output SC converter.

Publication(s):

[1] J. Jiang*, Y. Lu*, W. H. Ki, S. P. U*, and R. P. Martins*, "A dual-symmetrical-output switched-capacitor converter with dynamic power cells and minimized cross regulation for application processors in 28nm CMOS," in IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 344–345.

* Contributors with University of Macau

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A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors

Yan Lu, Junmin Jiang, Wing-Hung Ki, C. Patrick Yue, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Fast transient response, 3ns
Fast reference tracking, 2.5V/μs
75.8% efficiency at 0.13W/mm^2 power density
Silicon verified in UMC 65nm LL CMOS process

DESCRIPTION

Inspired by The Square of Vatican City, a fully-integrated step-down switched-capacitor DC-DC converter-ring with 100+ phases is designed with a fast-DVS (dynamic voltage scaling) feature for the microprocessor in portable/wearable devices. As shown in Fig. 1, this symmetrical ring-shaped converter surrounds its load in the square and supplies the on-chip power grid, such that a good quality power supply can be easily accessed at any point of the chip edges. There are 30 phases on the top edge and 31 phases on each of the other 3 edges, making 123 phases in total. The phase number and unit cell dimensions of this architecture can easily be adjusted to fit the floor plan of the load.

The pads of the converter-ring are placed at the corners, and will not affect the pads of the load. Moreover, by using the proposed V_{DD}-controlled oscillator (V_{DD}CO) the frequency of which is controlled by varying its supply voltage, a hitherto unexplored feature of the multiphase DC-DC architecture is exposed: the control-loop unity gain frequency (UGF) could be designed to be a few times higher than the switching frequency.

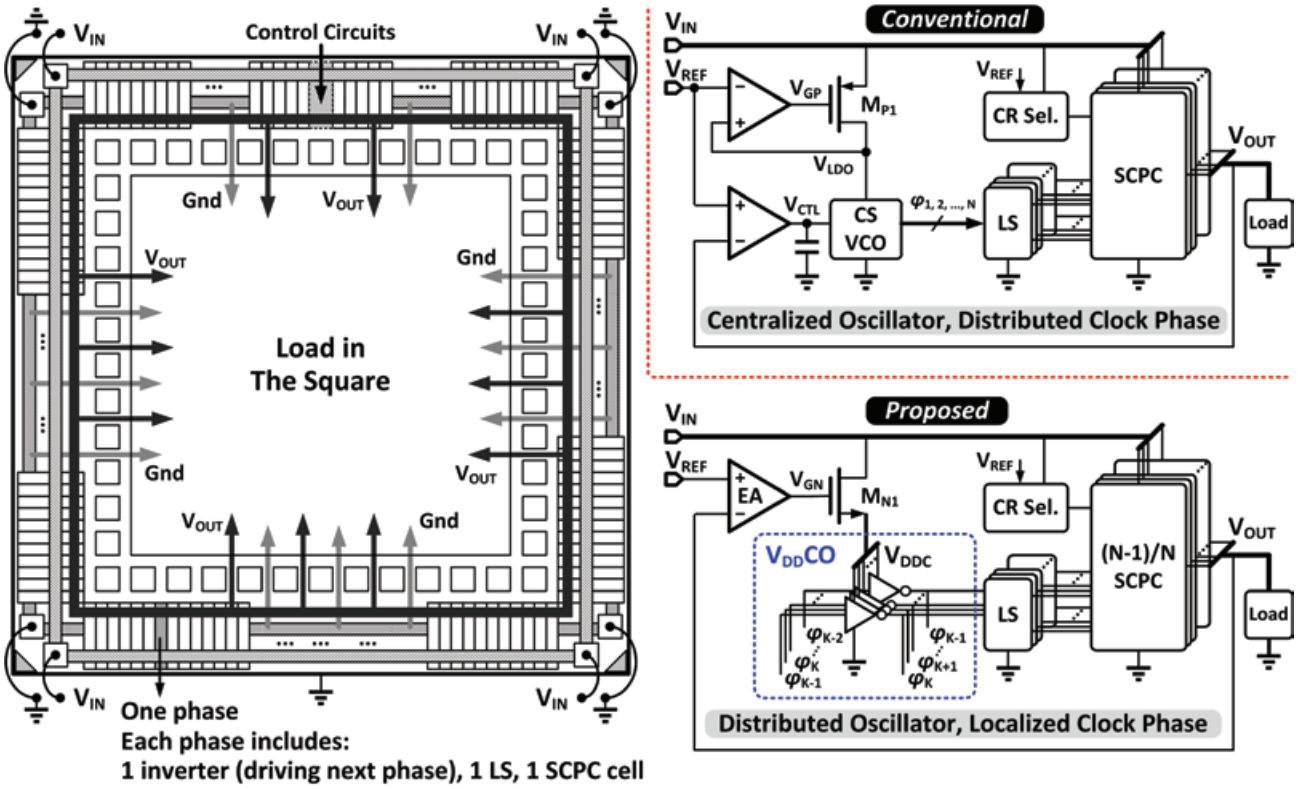


Fig. 1. Conceptual layout of the 100+ phases converter-ring for microprocessors; and the proposed system architecture with the V_{DD}CO and the (N-1)/N SCPC.

Publication(s):

[1] Y. Lu*, J. Jiang, W.-H. Ki, C. P. Yue, S.-W. Sin*, S.-P. U*, and R. Martins*, "A 123-phase DC-DC converter ring with fast-DVS for microprocessors," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2015, pp. 364–365.

[2] Y. Lu*, J. Jiang, and W. H. Ki, "A Multiphase Switched-Capacitor DC–DC Converter Ring With Fast Transient Response and Small Ripple," IEEE Journal of Solid-State Circuits, vol. 52, no. 2, pp. 579–591, Feb. 2017.

* Contributors with University of Macau

Sponsorship:

Research Grant Council of Hong Kong, Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Fully-Integrated Low-Dropout Regulator with Fast Transient Response and Full-Spectrum Power Supply Rejection

Yan Lu, Yipeng Wang, Quan Pan, Wing-Hung Ki, and C. Patrick Yue

FEATURES

Fully integrated voltage regulator
Full-spectrum power supply rejection
Fast transient response time, 1.15ns
Quiescent current, 50μA
43mV undershoot @ 0 to 10mA load step
Silicon Verified in TSMC 65nm CMOS

DESCRIPTION

A fully-integrated low-dropout regulator (LDO) with fast transient response and full spectrum power supply rejection (PSR) is proposed to provide a clean supply for noise-sensitive building blocks in wideband communication systems. With the proposed point-of-load LDO, chip-level high-frequency glitches are well attenuated, consequently the system performance is improved. A tri-loop LDO architecture is proposed and verified in a 65 nm CMOS process. In comparison to other fully-integrated designs, the output pole is set to be the dominant pole, and the internal poles are pushed to higher frequencies with only 50 μA of total quiescent current.

For a 1.2 V input voltage and 1 V output voltage, the measured undershoot and overshoot is only 43 mV and 82 mV, respectively, for load transient of 0 μA to 10 mA within edge times of 200 ps. It achieves a transient response time of 1.15 ns and the figure-of-merit (FOM) of 5.74 ps. PSR is measured to be better than -12 dB over the whole spectrum (DC to 20 GHz tested). The prototype chip measures 260 × 90 μm², including 140 pF of stacked on-chip capacitors.

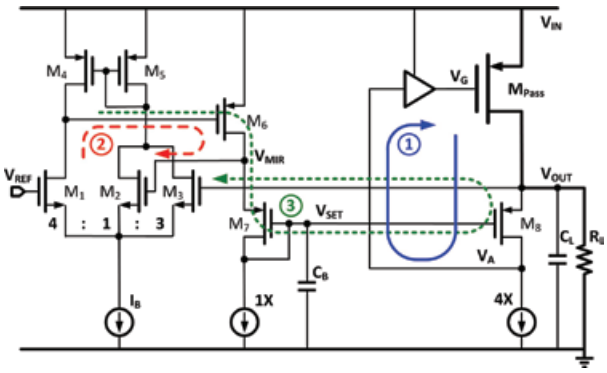


Fig. 1. Schematic of the proposed fully integrated tri-loop LDO.

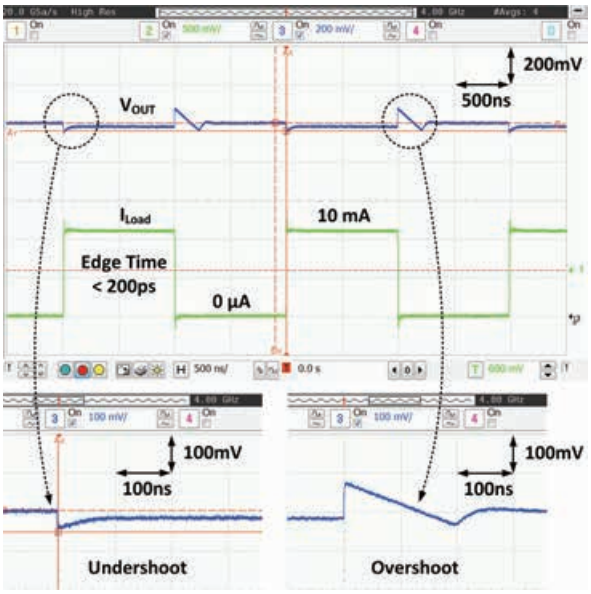


Fig. 2. Measured transient response with V_{IN} = 1.2 V, V_{OUT} = 1.0 V, and on-chip loading change from 0 μA to 10 mA within edge times of 200 ps.

Publication(s):

[1] Y. Lu*, Y. Wang, Q. Pan, W.-H. Ki, and C. P. Yue, "A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, pp. 707–716, Mar. 2015.

* Contributors with University of Macau

Sponsorship:

N/A

A Fully Integrated Digital LDO With Coarse–Fine-Tuning and Burst-Mode Operation

Mo Huang, Yan Lu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Fully integrated voltage regulator
Coarse-fine tuning and adaptive clock
55mV undershoot @ 2-to-100 mA load step
Quiescent current, 82μA
Silicon verified in ST 65nm CMOS process

DESCRIPTION

The digital low dropout regulator (D-LDO) has drawn significant attention recently for its low-voltage operation and process scalability. However, the tradeoff between current efficiency and transient response speed has limited its applications. In this work, a coarse–fine-tuning technique with burst-mode operation is proposed to the D-LDO. Once the voltage undershoot/overshoot is detected, the coarse tuning quickly finds out the coarse control word in which the load current should be located, with large power MOS strength and high sampling frequency for a fixed time.

Then, the fine-tuning, with reduced power MOS strength and sampling frequency, regulates the D-LDO to the desired output voltage and takes over the steady-state operation for high accuracy and current efficiency. The proposed D-LDO is verified in a 65-nm CMOS process with a 0.01-mm2 active area. The measured voltage undershoot and overshoot are 55 and 47 mV, respectively, with load steps of 2 to 100 mA with a 20-ns edge time. The quiescent current is 82 μA, with a 0.43-ps figure of merit achieved. Moreover, the reference tracking speed is 1.5 V/μs.

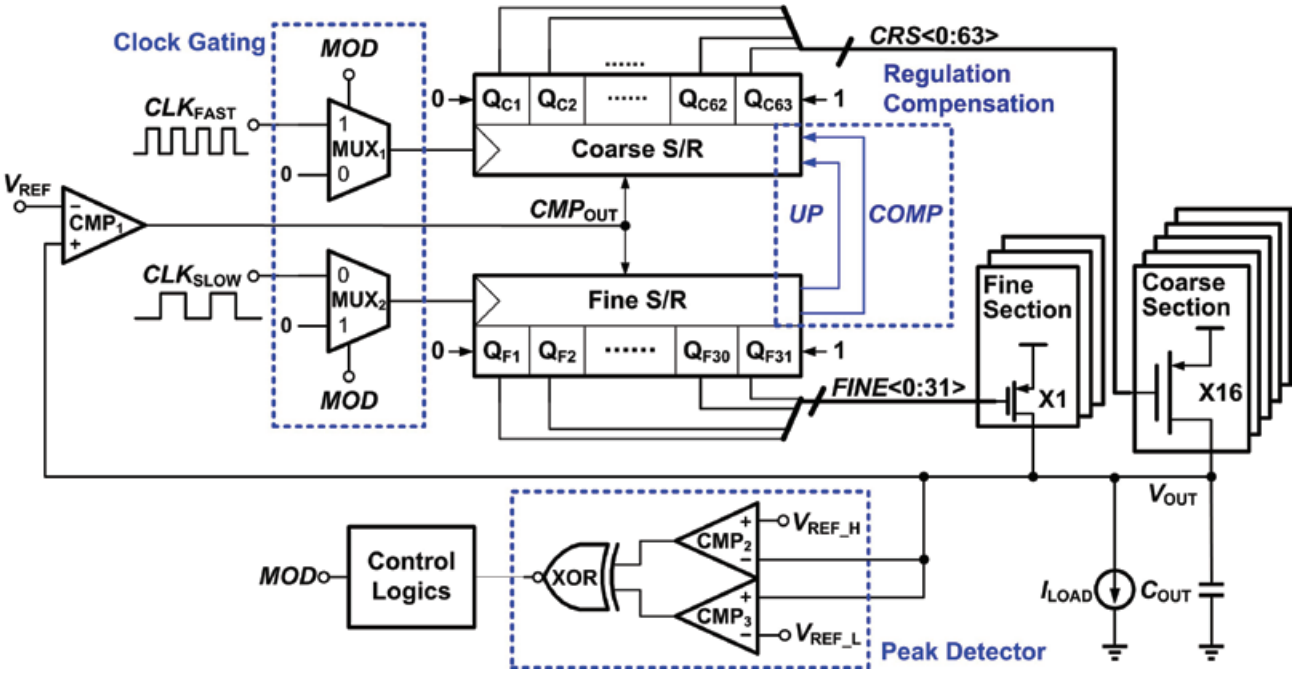


Fig. 1. Schematic of the proposed D-LDO.

Publication(s):

[1] M. Huang, Y. Lu, S. W. Sin, S. P. U, and R. P. Martins, "A Fully Integrated Digital LDO With Coarse–Fine-Tuning and Burst-Mode Operation," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 7, pp. 683–687, Jul. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators

Mo Huang, Yan Lu, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Wing-Hung Ki

FEATURES

Model analysis on the limit cycle oscillation (LCO)
Reduce the LCO mode of D-LDO to 1 with negligible area and power overhead
Simulated in ST 65nm CMOS

DESCRIPTION

The digital low-dropout regulator (D-LDO) has drawn significant attention recently for its low-voltage operation and process-scalability. However, the inherent quantization errors with this architecture will originate a steady-state limit cycle oscillation (LCO). As defined in literatures, the period of LCO is 2M times of the sampling period T_S, where M is the mode of LCO. In previous designs, LCO was reduced with a higher ADC resolution which increased circuit complexity, or using a dead-zone which sacrifices the output DC accuracy.

To address this issue, the modes and amplitudes of LCO are calculated in this work and verified by SPICE simulation in a 65-nm CMOS process. An LCO reduction technique for the D-LDO is then proposed, by adding two unit power transistors in parallel with the main power MOS array as a feedforward path, as shown in Fig. 1. This technique sets the LCO mode to 1 and effectively reduces the ripple amplitude for a wide (0.5–20 mA) load current range. When compared with the dead-zone scheme, this technique minimizes LCO with negligible circuit complexity and design difficulty.

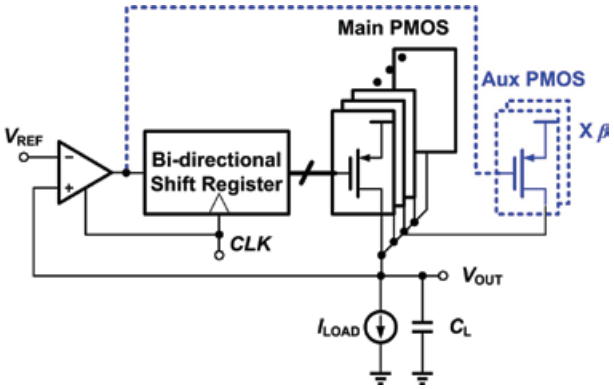


Fig. 1. Implementation of the modified D-LDO with LCO reduction.

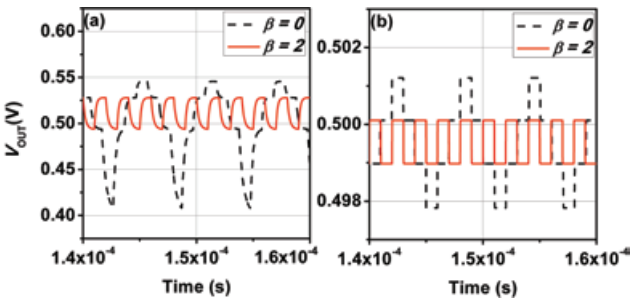


Fig. 2. Simulated results of the proposed D-LDO in β = 0 and 2 cases, with (a) 0.5- and (b) 20-mA load currents, at F_s = 1 MHz and V_{REF} = 0.5 V.

Publication(s):

1] M. Huang*, Y. Lu*, S. W. Sin*, S. P. U*, R. P. Martins*, and W. H. Ki, "Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 9, pp. 903–907, Sep. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

An NMOS-LDO Regulated Switched-Capacitor DC-DC Converter with Fast-Response Adaptive-Phase Digital Control

Yan Lu, Wing-Hung Ki, and C. Patrick Yue

FEATURES

Fully integrated voltage regulator
Cascaded switched-capacitor DC-DC with NMOS LDO
Adaptive-phase control for flatter efficiency curve
Peak DC-DC efficiency, 80.3%
Peak DC-DC + LDO efficiency, 76.2%
Output ripple, 2mV
Silicon Verified in TSMC 65nm CMOS

DESCRIPTION

A fully-integrated low-dropout regulated step-down multi-phase switched-capacitor DC-DC converter (a.k.a. charge pump, CP) with a fast-response adaptive-phase (Fast-RAP) digital controller is designed using a 65 nm CMOS process, as shown in Fig. 1 and Fig. 2.

Different from conventional designs, a low-dropout regulator (LDO) with an NMOS power stage is used without the need for an additional step-up charge pump for driving. A clock tripler and a pulse divider are proposed to enable the Fast-RAP control. As the Fast-RAP digital controller is designed to be able to respond faster than the cascaded linear regulator, transient response will not be affected by the adaptive scheme. Thus, light-load efficiency is improved without sacrificing the response time.

When the CP operates at 90 MHz with 80.3% CP efficiency, only small ripples would appear on the CP output with the 18-phase interleaving scheme, and be further attenuated at V_{OUT} by the 50-mV dropout regulator with only 4.1% efficiency overhead and 6.5% area overhead. The output ripple is less than 2 mV for a load current of 20 mA.

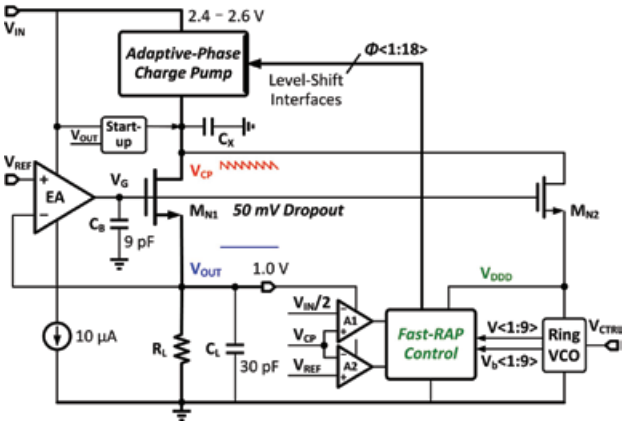


Fig. 1. Block diagram of the fully-integrated NMOS-LDO regulated switched-capacitor DC-DC converter with fast-response adaptive-phase (Fast-RAP) control.

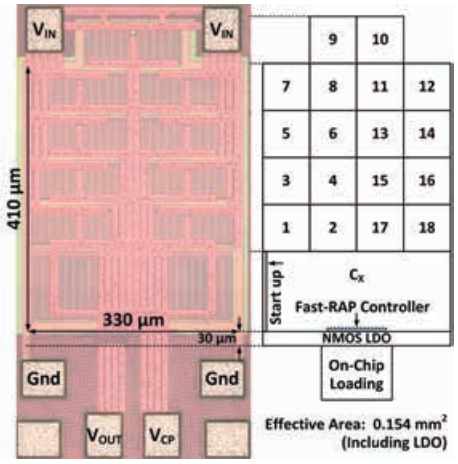


Fig. 2. Chip micrograph of the NMOS-LDO regulated charge pump.

Publication(s):

[1] Y. Lu*, W. Ki, and C. Patrick Yue, "An NMOS-LDO Regulated Switched-Capacitor DC–DC Converter With Fast-Response Adaptive-Phase Digital Control," IEEE Transactions on Power Electronics, vol. 31, no. 2, pp. 1294–1303, Feb. 2016.

* Contributors with University of Macau

Sponsorship:

N/A

A 312 ps Response-Time LDO with Enhanced Super Source Follower in 28 nm CMOS

Yan Lu, Cheng Li, Yan Zhu, Mo Huang, Seng-Pan U, and Rui P. Martins

FEATURES

Fully integrated voltage regulator
Enhanced super source follower
Fast transient response time, 312ps
Quiescent current, 100μA
26mV undershoot @ 0 to 10mA load step
Simulated in GF 28nm Bulk CMOS

DESCRIPTION

High quality fully integrated power supplies could notably improve the performances of the noise-sensitive building block in the ultra-wideband (UWB) communication systems.

The flipped-voltage-follower (FVF) based LDO is one of the most popular architectures, due to its simplicity and the potential for fast-transient-response. Since the FVF-based LDO is a single-ended topology, for a similar dynamic response, the FVF-based LDO only consumes 50% of the bias current compared a conventional LDO that using a differential error amplifier (EA). Although the FVF-based LDO also consists of an auxiliary differential EA, it is not in the main loop, and only serves as a bias voltage generator which consumes low current. Thus, the FVF-based LDO is more power-efficient

As shown in Fig. 1, double buffers are inserted into the cascode FVF topology to enable designing the dominant pole at the output node for better PSR and less voltage variation during load transient. An enhanced super source follower (E-SSF) is proposed in this work to further reduce the output impedance of the buffer that drives the power transistor. In the conventional SSF, only M_4 and M_6 are used, while in the proposed E-SSF, M_5 is inserted between M_4 and M_6, to provide an even lower output impedance.

The proposed idea is simulated in a 28 nm CMOS process, and consumes 100 μA quiescent current with 1.0 V input and 0.8 V output voltages. In total, 120 pF on-chip capacitors are used for filtering. The AC responses including the Bode plots and the PSR curves with the load current ranging from 0.1 to 10 mA are simulated. The loop UGF of the cascode FVF with the enhanced SSF is 1.28 GHz with 49° phase margin. Benefitting from the UHF bandwidth, full-spectrum PSR is achieved with the worst case of −18.9 dB happening at 1.55 GHz, while the low frequency PSR is around −27 dB. Meanwhile, a transient response time of 312 ps is achieved.

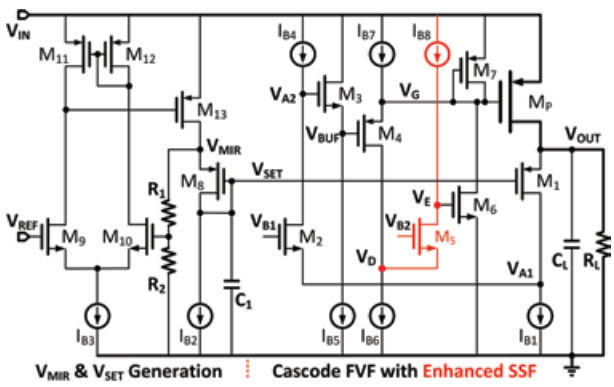


Fig. 1. Schematic of the proposed LDO with enhanced super source follower.

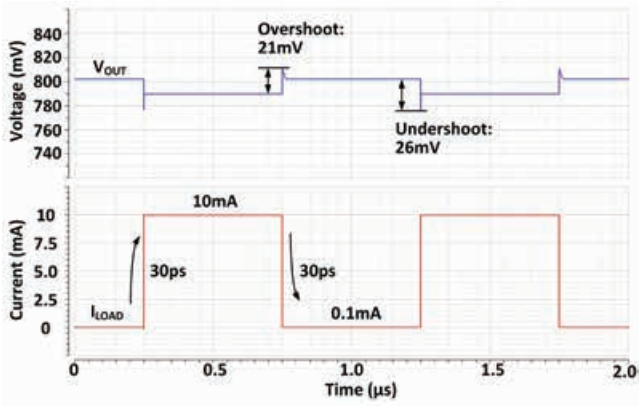


Fig. 2. Simulated load transient response of the LDO with 1.2 V input voltage and 1.0 V output voltage with voltage positioning.

Publication(s):

[1] Y. Lu, C. Li, Y. Zhu, M. Huang, S. P. U, and R. P. Martins, "A 312 ps response-time LDO with enhanced super source follower in 28 nm CMOS," Electronics Letters, vol. 52, no. 16, pp. 1368–1370, 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Self-Reconfiguration Property of A Mixed Signal Controller for Improving Power Quality Compensation during Light Loading

Man-Chung Wong, Yan-Zheng Yang, Chi-Seng Lam, Wai-Hei Choi, Ning-Yi Dai, Yajie Wu, Chi-Kong Wong, Sai-Weng Sin, U-Fat Chio, Seng-Pan U, and Rui P. Martins

FEATURES

Adaptive signal conditioning & programmability on-the-fly
Parallelism properties & higher redundancy
Higher accuracy, higher bandwidth, faster response time & low power
Algorithm complexity & simplicity of implementation

DESCRIPTION

When power quality compensator performance does not satisfy international standards, other PWMs can be selected, or the dc link voltage can be increased. However, it may be the case that neither of these methods will improve compensator performance during light loading due to the low resolution of the input signals compared with the error signal and the PWM error margin. The design of digital controllers is usually based on a full loading situation. The full analog-to-digital (A/D) conversion input signal range of a digital controller is therefore utilized, to avoid analog signal saturation. In a light load situation, the digital controller may suffer from the problem of low resolution, which significantly affects its compensation performance. There is presently no achievable control strategy to deal with power quality compensation issues during light loading.

A mixed signal controller for power quality compensator is proposed for enhancing the advanced performance that cannot be achieved by analog or digital controller alone and independently. The FPAA can be operated as an adaptive signal conditioning unit that pre-conditions and filters, according to the optimization of system performance. The modified signals then pass to the digital unit for further processing, assisted by the ADC. The digital system, FPGA/DSP, can work with a "backer" sub-program to optimize the system operation by reconfiguring the control system automatically, or to carry out self-testing and self-repairing tasks. When it is necessary to reconfigure the analog part, the re-programming data can be transferred directly through the digital path to the FPAA. Conversely, the FPAA can also send out control signals to the FPGA to modify the algorithm for protection, critical operations, etc.

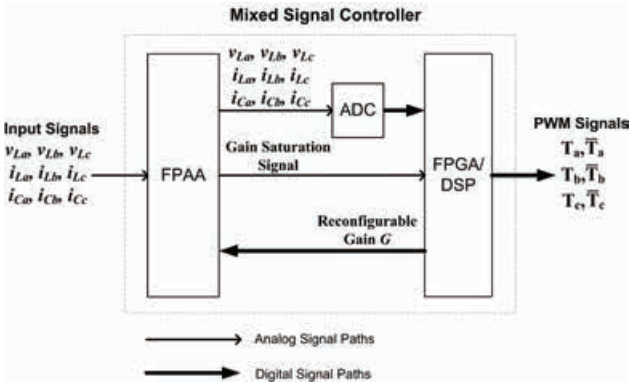


Fig. 1. Proposed mixed signal controller.

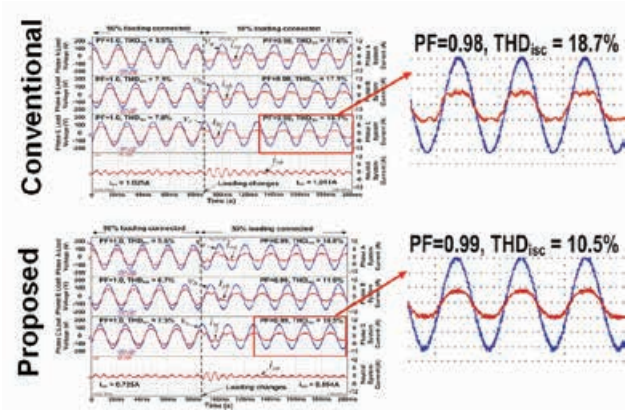


Fig. 2. Experimental compensation performance during loading changes by using conventional digital controller and proposed mixed signal controller.

Publication(s):

[1] M.-C. Wong, Y.-Z. Yang, C.-S. Lam, W.-H. Choi, N.-Y. Dai, Y.-j. Wu, C.-K. Wong, S.-W. Sin, U-F. Chio, S.-P. U, R.P. Martins, "Self-reconfiguration Property of A Mixed Signal Controller for Improving Power Quality Compensator during Light Loading," IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5938–5951, Oct. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

DCM Operation Analysis of KY Converter

Wen-Liang Zeng, Chi-Seng Lam, Wen-Ming Zheng, Sai-Weng Sin, Ning-Yi Dai, Man-Chung Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Deduce KY converter CCM/DCM operation boundary, DCM voltage gain & DCM small signal transfer function
Important for DCM closed-loop controller of KY converter IC design
MATLAB and 65 nm CMOS technology in Cadence confirm deduced DCM theory

DESCRIPTION

A KY converter has the characteristics of non-pulsating output current, low output voltage ripple and no right-half plane zero (RHPZ) in continuous conduction mode (CCM), which can overcome the drawbacks of the conventional boost and buck-boost converters. However, when the KY converter is implemented into an integrated circuit (IC), its discontinuous conduction mode (DCM) operation cannot be avoided due to a small inductor value.

The boundary for DCM operation region, DCM dc voltage and small signal transfer functions are proposed, which fill the gap of the DCM operation theory for the KY converter. Simulation results by using MATLAB and Cadence are provided to verify the deduced DCM operation theory of KY converter. Then, its DCM closed-loop controller design can be achievable in future.

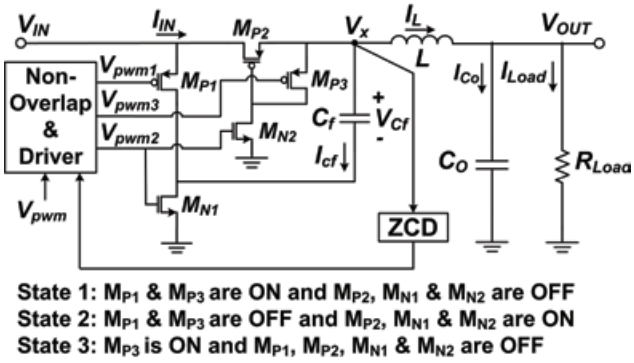


Fig. 1. Proposed KY converter IC topology for DCM.

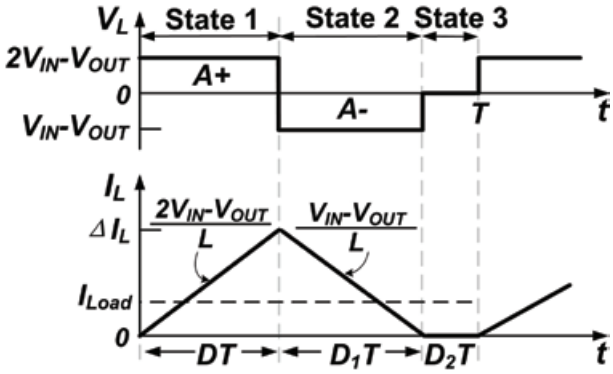


Fig. 2. KY converter idealized V_L and I_L waveforms for DCM.

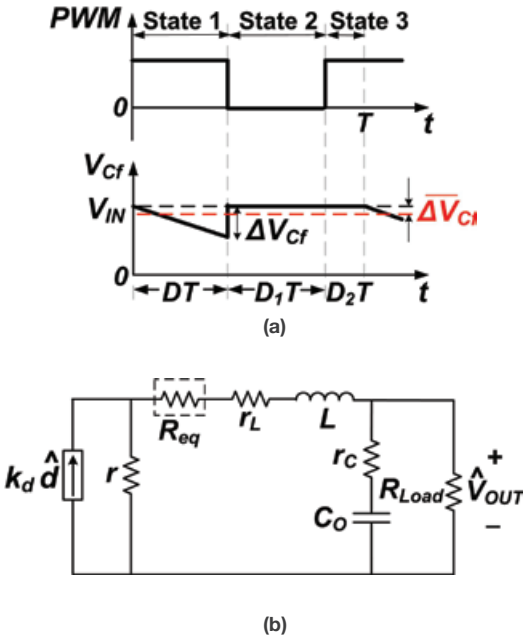


Fig. 3. Small signal model of KY converter for DCM: (a) Flying capacitor voltage V_{cf} deviation phenomenon and (b) Small signal model with V_{cf} deviation.

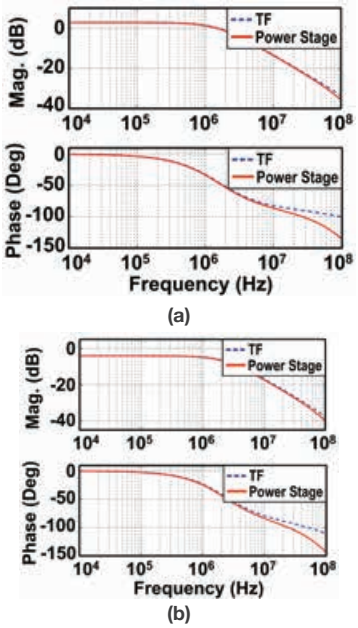


Fig. 4. KY converter open-loop bode plot for DCM: (a) When D=0.3 and (b) When D=0.5.

Publication(s):

[1] W.-L. Zeng, C.-S. Lam, W.-M. Zheng, S.-W. Sin, N.-Y. Dai, M.-C. Wong, S.-P. U, and R. P. Martins, "DCM Operation Analysis of KY Converter," IET Electron. Lett., vol. 51, no. 24, pp. 2037–2039, Nov. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

DCM Operation Analysis of 3-Level Boost Converters

Yi-Wei Tan, Chi-Seng Lam, Sai-Weng Sin, Man-Chung Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Deduce 3LB CCM/DCM operation boundary
DCM voltage gain & DCM small signal transfer function
Important for DCM closed-loop controller of
3LB converter IC design
MATLAB and 65 nm CMOS technology in Cadence
confirm deduced DCM theory

DESCRIPTION

The 3-level boost (3LB) converters have the characteristics of higher voltage conversion ratio and efficiency, lower inductor current ripples, output voltage ripples and voltage stresses on switches when compared with the conventional boost converters in continuous conduction mode (CCM). When implemented into an integrated circuit (IC) we cannot avoid the 3LB converter discontinuous conduction mode (DCM) operation due to a smaller inductance.

In this work, we deduce its DCM operation analysis, including CCM/DCM boundary, DCM voltage gain and DCM small signal transfer function, which are surprisingly different from the boost converter as they have the same CCM ones. We verify the deduced DCM operation theory using MATLAB and Cadence, to obtain a feasible DCM closed-loop controller design in future.

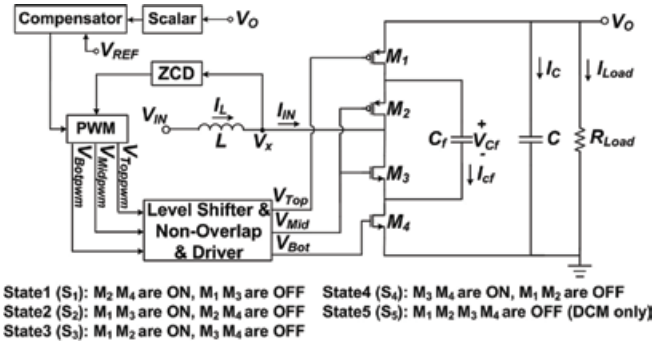
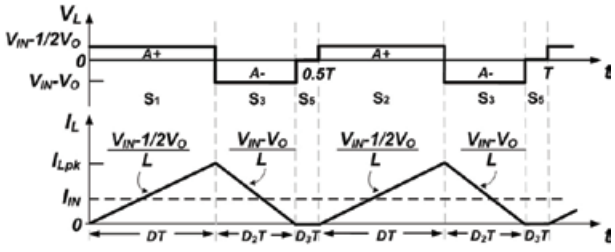
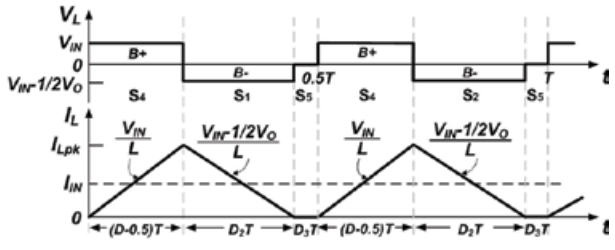


Fig. 1. Proposed 3LB converter IC topology for DCM.

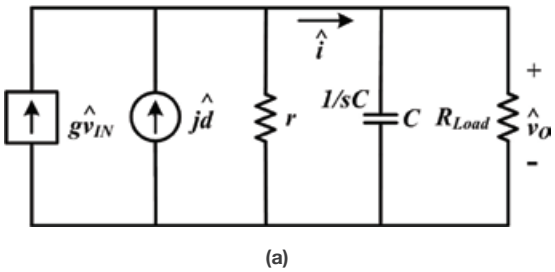


(a)

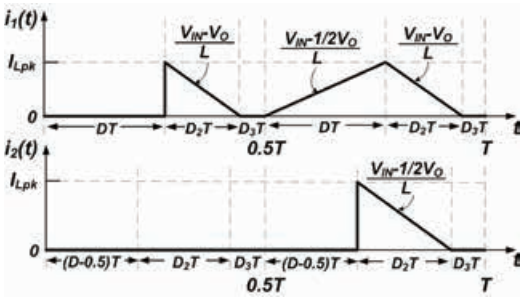


(b)

Fig. 2. 3LB converter idealized V_L and I_L waveforms for DCM: (a) when 0<D<0.5 and (b) when 0.5<D<1.

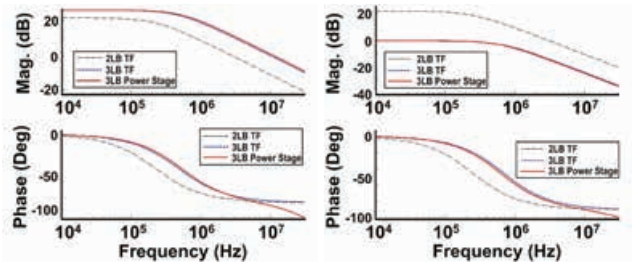


(a)



(b)

Fig. 3. Output side small signal model of the 3LB converter for DCM: (a) Output side of the 3LB converter DCM small signal model and (b) Output side current waveforms, $i_1(t)$: 0<D<0.5, $i_2(t)$: 0.5<D<1.



(a) (b)

Fig. 4. Boost converter and 3LB converter open-loop bode plot for DCM: (a) When D=0.3 and (b) When D=0.7.

Publication(s):

[1] Y.-W. Tan, C.-S. Lam, S.-W. Sin, M.-C. Wong, S.-P. U, and R. P. Martins, "DCM Operation Analysis of 3-level Boost Converters," IET Electron. Lett., vol. 53, no. 4, pp. 270–272, Feb. 2017.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

LIST OF PATENTS

1. Pui-In Mak, Seng-Pan U, R. P. Martins, "DC-Offset Canceled Programmable Gain Array for Low-Voltage Wireless LAN System and Method Using the Same", US Patent, Granted Number: 7,948,309, May 2011.

2. Man-Chung Wong, Chi-Seng Lam, Ning-Yi Dai, "Capacitive-coupling STATCOM and its control", Chinese Patent for Invention, Granted No. 200710196710.6, May 2011.

3. Pui-In Mak, Seng-Pan U, R. P. Martins, "Two-Step Channel Selection for Wireless Transmitter Front-Ends", US Patent, Granted Number: 8,019,290, Sep. 2011.

4. Pui-In Mak, Seng-Pan U, R. P. Martins, "Switched Current-Resistor Programmable Gain Array for Low-Voltage Wireless LAN System and Method Using the Same", US Patent, Granted Number: 8,229,382, Jul. 2012.

5. Ning-Yi Dai, Man-Chung Wong, Ying-Duo Han, "Generalized PWM methods and PW modulator for multi-level three-phase four-wire voltage source converter", Chinese Patent, Publication number: 200710102959.6, May 2012.

6. Man-Chung Wong, Ning-Yi Dai, Keng-Weng Lao, Chi-Kong Wong, "Single-phase power quality conditioner for power supply system in electrified Railway", Chinese Patent, Publication number: No. 201210051065.X, Feb. 2012.

7. Man-Chung Wong, Ning-Yi Dai, Wen-Chen Zhang, Chi-Kong Wong, "A single-phase grid-connected inverter with power quality conditioning capability", Chinese Patent, Application number: No. 2012120400404770, Nov. 2012.

8. Man-Chung Wong, Ning-Yi Dai, Keng-Weng Lao, Chi-Kong Wong, "Railway power conditioner for co-phase traction supply system", US Patent, Application Number:13/709,236, Dec. 2012.

9. Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins, Franco Maloberti, "N-Bits Successive Approximation Register Analog-to-Digital Converting System", US Patent, Granted Number: 8,344,931, Jan. 2013.

10. Sai-Weng Sin, He-Gong Wei, Li Ding, Yan Zhu, Chi-Hang Chan, U-Fat Chio, Seng-Pan U, R. P. Martins, Franco Maloberti, "A Time-Inteleaved Piplined-SAR Analog to Digital Converter with Low Power Consumption", US Patent, Granted Number: 8,427,355, Apr. 2013.

11. He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins, "Delay Generator", US Patent, Granted Number: 8,441,295, May 2013.

12. U-Fat Chio, He-Gong Wei, Yan Zhu, Sai-Weng Sin, Seng-Pan U, R. P. Martins, Franco Maloberti, "Cascade Analog to Digital Converting System", US Patent, Granted Number: 8,466,823, Jun. 2013.

13. Sai-Weng Sin, Li Ding, Yan Zhu, He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Seng-Pan U, R. P. Martins, Franco Maloberti, "Analog to Digital Converter Circuit", Taiwan Patent, Granted Number: 201242261, Mar. 2014.

14. He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins, "Delay Generator", Taiwan Patent, Granted Number: 201246793, Mar. 2014.

15. Man-Chung Wong, Chi-Seng Lam, Wai-Hei Choi, "Control strategy of adaptive dc-link voltage controlled LC-VSI device for reactive power compensation", Chinese Patent for Invention, Granted, No. 201210051133.2, May 2014.

16. Zushu Yan, Pui-In Mak, Man-Kay Law, R. P. Martins, "Frequency Compensation Techniques for Low-Power and Small-Area Multistage Amplifiers", US Patent, Granted Number: 8,963,639, Feb. 2015.

17. Ka-Fai Un, Pui-In Mak, R. P. Martins, "Wireless Transmitter", US Patent, Granted Number: 9,037,100, May 2015.

18. Ka-Fai Un, Pui-In Mak, R. P. Martins, "Wideband Driver Amplifier", US Patent, Granted Number: 9,172,337, Oct. 2015.

LIST OF PATENTS

19. Ka-Fai Un, Pui-In Mak, R. P. Martins, "Poly-Phase Local Oscillator", US Patent, Granted number: 9,093,951, Jul. 2015.

20. Yan Zhu, Chi-Hang Chan, Seng-Pan U, R. P. Martins, "Sampling front-end for analog to digital converter", US patent, Granted Number: 8,947,283, Feb. 2015.

21. Chi-Seng Lam, Man-Chung Wong, Wai-Hei Choi, Ying-Duo Han, "Adaptive dc-link voltage controlled LC coupling hybrid active power filters for reactive power compensation", US Patent, Granted Number: 9,122,296, Sept. 2015.

22. Zhicheng Lin, Pui-In Mak, R. P. Martins, "ZigBee Receiver Exploiting an RF-to-BB Current-Reuse Blixer and Hybrid Filter Topology", US Patent, Application Number: 14/254,318, Granted Number: 9,237,055, Jan. 2016.

23. Pui-In Mak, Fujian Lin, R. P. Martins, "RF-to-BB-Current-Reuse Wideband Receiver with a Single-MOS Pole-Zero LPF", US Patent, Granted Number: 9,270,314, Feb. 2016.

24. Wei-Han Yu, Chak-Fong Cheang, Ka-Fai Un, Pui-In Mak, R. P. Martins, "Non-recursive digital calibration for joint-elimination of transmitter and receiver I/Q imbalances with minimized add-on hardware", US Patent, Granted Number: 9,276,798, Mar. 2016.

25. Zhicheng Lin, Pui-In Mak, R. P. Martins, "IF-Noise-Shaping Transistorized Current-Mode Lowpass Filter Utilizing Cross-Coupled Transistors", US Patent, Granted Number: 9,306,540, Apr. 2016.

26. Pui-In Mak, Fujian Lin, R. P. Martins, "An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers", US Patent, Granted Number: 9,356,636, May. 2016.

27. Pui-In Mak, Zhicheng Lin, R. P. Martins, "Gain-Boosted N-Path Bandpass Filter", US Patent, Granted Number: 9,374,063, Jun. 2016.

28. Pui-In Mak, Zhicheng Lin, R. P. Martins, "Ultra-Low-Voltage Current-Reuse Voltage-Controlled Oscillator and Transconductance-Capacitor Filter", US Patent, Granted Number: 9,444,431, Sept. 2016.

29. Zhicheng Lin, Pui-In Mak, R. P. Martins, "Complex-Pole Load Offering Concurrent Image Rejection and Channel Selection", US Patent, Granted Number: 9,479,140, Oct. 2016.

OUR TEAM

SKL-AMSV Leadership Team

Rui Paulo da Silva Martins, Director
Seng-Pan U, Deputy Director
Pui-In Mak, Associate Director (Research) & Wireless Research Line Coordinator
Sai-Weng Sin, Teaching Coordinator & Data Conversion Research Line Coordinator
Mang-I Vai, Biomedical Research Line Coordinator
Man-Chung Wong, Integrated Power Research Line Coordinator

SKL-AMSV Faculty

Man-Kay Law, Assistant Professor
Sio-Hang Pun, Assistant Professor
Yan Zhu, Assistant Professor
Chi-Seng Lam, Assistant Professor
Yan Lu, Assistant Professor
Jun Yin, Assistant Professor
Chi-Hang Chan, Assistant Professor
Yanwei Jia, Assistant Professor
Yong Chen, Assistant Professor
Ka-Fai Un, Macao Fellow
Ka-Meng Lei, Macao Fellow

SKL-AMSV Administrative and Technical Staff

Weng-Keong Che, Technology Transfer Officer
Fan Ng, Functional Head of Administration
Un-Pang Lei, Administrative Officer
Chi-Wai Tang, Senior Administrative Assistant
Yuen-Ki Chan, Senior Administrative Assistant
Pui-Wan Sou, Administrative Assistant
Sut Wai Ieong, Administrative Assistant

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Behzad Razavi, University of California, Los Angeles, USA
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Ming-Dou Ker, National Chiao-Tung University, Taiwan
Hoi-Jun Yoo, Korea Advanced Institute of Science and Technology, Korea
Akira Matsuzawa, Tokyo Institute of Technology, Japan
Michiel Steyaert, Katholieke Universiteit Leuven, Begium
Bram Nauta, University of Twente, Netherlands
Chris Mangelsdorf, Analog Devices
Bang-Sup Song, University of California, San Diego, USA
Jacob Baker, University of Nevada, Las Vegas, USA

Rui Paulo da Silva Martins

Vice-Rector (Research), U. of Macau
Chair Professor ECE, IEEE Fellow
Academician, Academy of Sciences of Lisbon, Portugal
Director, State Key Laboratory of AMS-VLSI

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RESEARCH INTERESTS

Data Conversion and Signal Processing
Wireless IC
Biomedical IC
Integrated Power Electronics
Multidisciplinary Area of Microfluidics, Lab-on-a-Chip

PROFESSIONAL SERVICES

- Chairman, IEEE CAS Society Fellow Evaluation Committee, Class of 2018
- General Chair, ACM/IEEE ASP-DAC 2016
- Nominations Committee Member, IEEE CAS Society 2016
- Division I (CASS, EDS, SSCS) – Director of IEEE, Nominating Committee, Representative of CASS, 2014
- IEEE CAS Society Fellow Evaluation Committee, Classes of 2013-2014
- Vice-President (World), Regional Activities and Membership of the IEEE CAS Society 2012-2013
- Associate Editor, IEEE TCAS-II 2010-2013
- Vice-President (Region 10/Asia, Australia, The Pacific) IEEE CAS Society 2009-2011
- General Chair, IEEE APCCAS 2008
- Founding Chairman, IEEE Macau Chapter CAS/COM, 2005-2008
- Founding Chairman, IEEE Macau Chapter, 2003-2005

AWARDS

- IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award 2016, Tokyo, Japan.
- Business Awards of Macau – Innovation Excellence Award, 2014 (attributed to the SKL-AMSV)
- Macao Science & Technology Invention Awards 2012, 2014, and 2016
- IEEE ISSCC Silk-Road Award 2011 and 2016 (as co-supervisor)
- IEEE Circuits and Systems Society "World-Chapter of the Year" 2009 (as Founding Chapter Chair)
- "Honorary Title of Value", Decoration attributed by the Macao Special Administrative Region Government (Chinese Administration), 2001
- "Medal of Merit (Class of Professional Merit)", Decoration attributed by the Macao Government (Portuguese Administration), 1999

THESIS SUPERVISED (OR CO-SUPERVISED)

19 Ph.D.
21 M.Sc.

SELECTED PUBLICATIONS

- K-M Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti, R. P. Martins, "A Handheld High-Sensitivity Micro-NMR CMOS Platform With B-Field Stabilization for Multi-Type Biological/Chemical Assays", IEEE Journal of Solid-State Circuits, pp. 284-297, vol. 52, No.1, Jan. 2017.

- J. G, X. Liu, T. Chen, P-I Mak, Y. Du, M-I Vai, B. Lin, R.P.Martins, "An intelligent digital microfluidic system with fuzzy-enhanced feedback for multi-droplet manipulation", Lab on a Chip, Royal Society of Chemistry, Vol.13, Issue 3, pp.443-451, 2013.

- Z. Yan, P.-I. Mak, M.-K. Law and R. P. Martins, "A 0.016-mm^2 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load with >0.95-MHz GBW," IEEE Journal of Solid-State Circuits, vol. 48, pp. 527-540, Feb. 2013.
  P.-I. Mak and R. P. Martins, "A 0.46-mm2 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS," IEEE Journal of Solid-State Circuits, pp. 1970-1984, vol. 46, Sep. 2011.

- Y. Zhu, C.-H. Chan, U-F. Chio, S.-W. Sin, S.-P. U, R.P. Martins, and F. Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90nm CMOS," IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1111 -1121, Jun 2010.

Seng-Pan U (Ben)

General Manager and Senior Analog Design Manager of Synopsys - Chipidea Microelectronics (Macau) Ltd.
Visiting Professor (Part-Time), IEEE Fellow
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RESEARCH INTERESTS

Data Conversion and Signal Processing
Analog and Power Management ICs
Analog Front-End Systems (Audio Video, Wireless)
Serdes Wireline ICs

PROFESSIONAL SERVICES

- Member, Sci&Tech Council of China Ministry of Edu., 2016-
- Member, Sci&Tech Council of Macau SAR, 2016 -
- President, IEEE Macau Section, 2016-2018
- President, Macau Industry-University-Research Institute Collaboration Association, 2016 - Present
- Founder & Honorary Chair, IEEE SSCS Chapter, 2009-
- Honorary Chairman, IEEE CAS/COM Chapter, 2010-
- ITPC Member (Data Converter Subcommittee) & China Country Representative, IEEE ISSCC, 2015-
- Chairman, Data Converters Subcommittee, IEEE Asian Solid-State Circuits Conf. (A-SSCC), 2017- (09-16 TPC)
- Chairman, Ana. Mixed-Signal & RF Design Subcom., The Int. Sym. VLSI Des. Auto. & Test (VLSI-DAT), 2012 -
- Editorial Board Member, Springer Journal of Analog Integrated Circuits and Signal Processing, 2012-
- IEEE SSCS Distinguished Lecturer, 2014-2015
- Local Organization Chair, IEEE A-SSCC, 2019
- Tech. Program Co-Chair, PRIME-ASIA, 2011
- Tech. Program Co-Chair, IEEE APCCAS 2008

AWARDS

- National State Sci. & Tech. Progress Award, 2011
- He Leung Ho Lee Fund. S&T. Innovation Award, 2010
- Scientific Chinese of the Year Award, 2012
- "Honorary Title of Value", Macau SAR Decoration, 2010
- Macau Sci. & Tech. Invention Awards 2012, 2014, 2016
- Macau Sci. & Tech. Progress Awards 2012, 2014, 2016
- Macau Business Awards - Research Achi. Award, 2013
- IEEE Solid-State Circuit Society "Outstanding Chapter Award" 2013 (as Founding Chapter Chairman)
- IEEE Circuits and Systems Society "World-Chapter of the Year" 2009 (as Chapter Secretary)
- IEEE ESSCIRC Best Paper Award, 2014 (as co-author)
- IEEE SSCS Pre-doc Achi. Award, 2015 (as supervisor)
- IEEE ISSCC Silk-Road Award, 2011 (as supervisor)
- IEEE A-SSCC SDC Winner Award, 2011 (as supervisor)

THESIS SUPERVISED (OR CO-SUPERVISED)

8 Ph.D., 26 M.Sc., 36 B.Sc. (Final Year Project)

SELECTED PUBLICATIONS

- M. Huang, Y. Lu, S-P U, R.P. Martins, "A Reconfigurable Bidirectional Wireless Power Transceiver with Max Current Charging Mode and 58.6% Battery-to-Battery Efficiency," IEEE ISSCC Dig. Tech. Papers, pp.376-377, Feb. 2017.

- M. Huang, Y. Lu, S-P. U, R.P. Martins, "An Output-Capacitor-Free Analog-Assisted Digital Low-Dropout Regulator with Tri-loop Control", IEEE ISSCC Dig. of Tech. Papers, pp.376-377, Feb. 2017.

- C-H. Chan, Y. Zhu, H-I. Meng, Z-W. Hong, S-P. U, R.P. Martins, "A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration", IEEE ISSCC Dig. of Tech. Papers, pp. 282-284, Feb. 2017.

- Y. Zhu, C-H. Chan, S-P. U, R.P. Martins, "An 11b 450MS/s 3-way TI Sub-ranging Pipelined-SAR ADC in 65nm CMOS", IEEE J. Solid-State Circuits, vol.51, pp.1223-34, May 2016.

- C-H Chan, Y.Zhu, S-W Sin, S-P. U, R.P.Martins. "A 6b 5GS/s 4 Interleaved 3b/Cycle SAR ADC", IEEE J. Solid-State Circuits, vol.51, Issue2, pp.365-377, Nov.2015. & IEEE ISSCC Dig. of Tech. Papers, pp.466-8, Feb. 2015. S-S Wong, U-F Chio, Y.Zhu, S-W Sin, S-P. U, R.P.Martins "A 2.3mW 10-bit 170MS/s Two-Step Binary-Search Assisted Time-Interleaved (TI) SAR ADC," IEEE J. Solid-State Circuits. vol. 48, Issue 8, pp.1783-1794, Aug. 2013 & Proc. of IEEE CICC, pp.1-4, Sep 2012.

Pui-In Mak (Elvis)

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RESEARCH INTERESTS

3G/4G/5G Transceivers (sub-6GHz, >28 GHz)
IoT Transceivers (Bluetooth LE, ZigBee, NB-IoT)
Analog Techniques (amplifier, filter, crystal oscillator)
Portable In-Vitro Diagnostic Devices (DNA, proteins)
Microfluidic Technologies (digital, channel, hybrid)
Biomedical Readout Interfaces (EEG, ECG)

PROFESSIONAL SERVICES

- Board of Governor, IEEE CASS 2009-2011
- Distinguished Lecturer, IEEE SSCS 2017-2018
- Distinguished Lecturer, IEEE CASS 2014-2015
- Editorial Board Member, IEEE Press 2014-2016
- Senior Editor, IEEE JETCAS 2014-2015
- Associate Editor, IEEE TCAS-I 2010-2011, 2014-2015
- Associate Editor, IEEE TCAS-II 2010-2013
- Guest Editor, IEEE JSSC 2018
- Guest Editor, IEEE RFIC Virtual Journal 2013
- TPC Vice-Chair, IEEE/ACM ASPDAC 2016
- TPC Member, IEEE ISSCC 2017-Present
- TPC Member, IEEE ESSCIRC 2016-Present
- TPC Member, IEEE A-SSCC 2014-2016

AWARDS

- National Scientific & Technological Progress Award'11
- Macao Science & Technology Invention Awards'12'14'16
- Honorable Title of Value, Macau Government'06
- University of Cambridge Visiting Fellowship'09
- Invited Distinguished Speaker, Qualcomm-USA'17
- Invited Keynote Speaker, IEEE PRIME/SMACD'16
- Invited Keynote Speaker, IEEE'RFID-TA'16
- IEEE ISSCC Silkroad Award'16
- IEEE A-SSCC Distinguished Design Award'15
- IEEE TCAS-II Best Associate Editor'12-'13
- IEEE CASS Outstanding Young Author Award'10
- IEEE SSCS Pre-Doctoral Achievement Awards 14'15'17 (as advisor)

CURRENT GROUP MEMBERS

Ph.D.

Tantan Zhang, 2010 (co-supervisor)
Cheng Dong, 2012 (co-supervisor)
Wei-Han Yu, 2012
Chak-Fong Cheang, 2012
Gengzhen Qi, 2013
Xingqiang Peng, 2014
Haidong Yi, 2015
Chao Fan, 2016

M.Sc.

Tongquan Jiang, 2014 (co-supervisor)

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Jie Gao, 2015
Liang Wan, 2015
Tianlan Chen, 2017

SELECTED PUBLICATIONS

- K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti and R. P. Martins, "A Handheld High-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays," IEEE Journal of Solid-State Circuits (JSSC), vol. 52, Jan. 2017. [Also in ISSCC 2016]

- F. Lin, P.-I. Mak and R. P. Martins, "An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/ Passive Mixers and a Single-MOS Pole-Zero LPF," IEEE Journal of Solid-State Circuits (JSSC), vol. 49, pp. 2547-2559, Nov. 2014. [Also in ISSCC'14]

- Z. Lin, P.-I. Mak and R. P. Martins, "A 2.4-GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65-nm CMOS," IEEE Journal of Solid-State Circuits (JSSC), vol. 49, pp. 1333-1344, Jun. 2014. [Also in ISSCC'13]

- Z. Yan, P.-I. Mak, M.-K. Law and R. P. Martins, "A 0.016-mm^2 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load with >0.95-MHz GBW," IEEE Journal of Solid-State Circuits (JSSC), vol. 48, pp. 527-540, Feb. 2013. [Also in ISSCC'12]

- P.-I. Mak and R. P. Martins, "A 0.46-mm^2 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS," IEEE Journal of Solid-State Circuits (JSSC), pp. 1970-1984, vol. 46, Sept. 2011. [Also in ISSCC'11]

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RESEARCH INTERESTS

High-Performance Data Converters
- Pipelined, SAR, Flash, Binary Search, etc…
- Oversampling Data Converters

Power Management Integrated Circuits
Analog and Mixed-Signal Integrated Circuits
Low Voltage Switched-Capacitor Circuits
Integrated Analog Front-Ends

PROFESSIONAL SERVICES

- TPC and SDC Member, A-SSCC 2013-Present
- Publication Chair, ASPDAC 2016
- TPC Member, VLSI-SoC 2015
- TPC Member, The International Wireless Symposium
- Secretary, IEEE Solid-State Circuit Society (SSCS) Macau Chapter, 2009-2016
- Treasurer/Secretary, IEEE Macau CAS/COM Joint Chapter, 2009-2016

AWARDS

- Co-recipient of Third Class, Macau Scientific and Technological Invention Award, 2016
- Co-recipient of Second Class, Macau Scientific and Technological Invention Award, 2012, 2014
- Co-recipient of Second Class, State Scientific and Technological Progress Award, China, 2011
- PRIME Silver Leaf Certificate 2015 (as advisor)
- Best Master Thesis Award in Tsinghua University 2012 (as co-advisor)
- Student Design Contest Award, A-SSCC 2011 (as co-advisor)
- Silk Road Award, ISSCC 2011(as co-advisor)

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Jianwei Liu, 2012
Da Feng, 2010
Mingqiang Quo, 2014
Biao Wang, 2013
Dezhi Xing, 2012

M.Sc.

Song Cui, 2016
Hubert Liang, 2014
Jiaji Mao, 2013
Hanyu Wang, 2016
Jixuan Li, 2014

POST-DOCTORAL FELLOW

U-Fat Chio, 2012

R.A.

Luis Brochado Reis, 2016

SELECTED PUBLICATIONS

- Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, R. P. Martins, "A 5.5mW 6b 5GS/s 4-times Interleaved 3b/cycle SAR ADC in 65nm CMOS," in IEEE International Solid-State Circuit Conference (ISSCC), 2015.

- He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins and F. Maloberti, "A 0.024mm^2 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65 nm CMOS," in IEEE International Solid-State Circuit Conference (ISSCC), vol. 54, pp.188-189, Feb 2011.

- Si-Seng Wong, U-Fat Chio, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, "A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC", in IEEE Journal of Solid-State Circuits. vol. 48, Issue 8, pp. 1783-1794, Aug 2013.

- Arshad Hussain, Sai-Weng Sin, Chi-Hang Chan, Seng-Pan U, Franco Maloberti, Rui Paulo Martins, "Active-Passive ΔΣ Modulator for High-Resolution and Low-Power Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 1, pp. 364 – 374, Jan 2017.

- Yuan Ren, Sai-Weng Sin, Chi-Seng Lam, Man-Chung Wong, Seng-Pan, U, R.P.Martins, " A High DR Multi-Channel Stage-Shared Hybrid Front-End for Integrated Power Electronics Controller", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 1-4, Nov 2016.

Vai Mang I

Associate Professor, IEEE Senior Member
President, Macau Society of Biomed. Eng.
Exec. Board Member, CSBME

Room 3013, 3/F, N21, University of Macau, Taipa, Macau, China
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RESEARCH INTERESTS

Embedded Systems
Biomedical Electronics
Biomedical Signal Processing
Intra-Body Communication

PROFESSIONAL SERVICES

- General Chair, The Optoelectronics Global Conference (OGC) 2015, 2015
- Member of The IEEE Industrial Electronics Society (IES) Technical Committee on Cloud and Wireless Systems for Industrial Applications, since 2015
- Executive Board Member of the EEE EMBS Hong Kong - Macau Joint Chapter, since 2012
- Chair of IEEE Macau Section (2008-2009)
- Committee Member of Biomedical Electronics Society, the Chinese Institute of Electronics, since 2004
- Executive Board Member, Chinese Society of Biomedical Engineering (CSBME)
- Committee Member of Medical Neural Engineering Section, the Chinese Society of Biomedical Engineering, since 2010

CURRENT GROUP MEMBERS

Ph.D.

Chen Changhao, 2010
Yu Yuanyu, 2011
Zhang Shuang, 2011
Dong Cheng, 2012
Wang Jiujiang, 2012
Wang Panke, 2015
Sun Peng, 2015

M.Sc.

Cui Xutong, 2014
Wang Zhi Jiong, 2014
Liu Xin, 2014
Chen Zhimin, 2015
Han Yibo, 2015

R.A.

Huang Huajuan, 2016
Che U Kin, 2016

SELECTED PUBLICATIONS

- Xi Mei Chen, Shovan Barma, Sio Hang Pun, Mang I Vai, Peng Un Mak, "Direct Measurement of Elbow Joint Angle Using Galvanic Couple System," IEEE Transactions on Instrumentation and Measurement, 66(4), pp. 757-766, April, 2017

- Chang Hao Chen, Elizabeth A McCullagh, Sio Hang Pun, Peng Un Mak, Mang I Vai, Pui In Mak, Achim Klug, Tim C Lei, "An Integrated Circuit for Simultaneous Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation," IEEE Transactions on Biomedical Engineering, 64(3), pp.557-568, March, 2017

- Jiujiang Wang, Sio Hang Pun, Peng Un Mak, Ching-Hsiang Cheng, Yuanyu Yu, Pui-In Mak, Mang I Vai, "Improved Analytical Modeling of Membrane Large Deflection With Lateral Force for the Underwater CMUT Based on Von Kármán Equations," IEEE Sensors Journal, 16(17), pp. 6633-6640, 2016

- Wenya Nan, João Pedro Rodrigues, Jiali Ma, Xiaoting Qu, Feng Wan, Pui-In Mak, Peng Un Mak, Mang I Vai, Agostinho Rosa, "Individual Alpha Neurofeedback Training Effect on Short Term Memory," International journal of psychophysiology, 86(1), pp. 83-87, October, 2012

- Sio Hang Pun, Yue Ming Gao, Peng Un Mak, Mang I Vai, Min Du, "Quasi-static Modeling of Human Limb for Intra-body Communications With Experiments," IEEE Transactions on Information Technology in Biomedicine, 15(6), pp. 870-876, November, 2011

Man Chung Wong
Associate Professor
IEEE Senior Member

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RESEARCH INTERESTS

Integrated Power Electronics Controllers
Integrated DC-DC Converters
Power Quality Compensators
Renewable Energy
Smart Grid Technology

PROFESSIONAL SERVICES

- IEEE Region 10 Power and Energy Society North Representative (China, Macao, Hong Kong, Taiwan, Japan and South Korea)
- Chair, IEEE Macau Power & Energy and Power Electronics Joined Chapter, 2013~up to now.
- Chair, IEEE Macau Section, 2014~2015
- Vice Chair, IEEE Macau Section, 2010~2013
- General Chair of IEEE Region 10 Asia Pacific (TENCON) 2015 Conference
- Chair of Power Electronics Section and Organizing Committee Member in IEEE Asia-Pacific Conference on Circuits and Systems – APCCAS'2008
- Organizing Committee Member for IEEE/IEE
- Regional Inter-University Post-Graduate
- Electrical and Electronics Engineering Conference. – RIUPEEEC'2006
- Organizing Committee Member for Ninth International Symposium on Consumer Electronics (ISCE2005) at 2005

AWARDS

- Third-Class Award in Technology Invention Award given by FDCT (Macao Science and Technology Fund), "Design, Control and Application of Low-Loss Low-Cost Capacitive Coupling Current Quality Compensator (CCQC)", 2014.
- Third-Class Award in Technology Invention Award given by FDCT (Macao Science and Technology Fund), "Three-Dimensional Pulse Width Modulation Techniques and its Applications in Three-Phase Four-Wire Active Filters", 2012.
- Second Prize of Year 2003 Tsinghua University Excellent Ph. D. Thesis Award
- Young Scholar Award by University of Macau at Year 2001
- Macau Young Scientific Award by Macau International Research Institute at Year 2000

CURRENT GROUP MEMBERS

Ph.D.

Ya-Jie Wu, 2012
Wen-Liang Zeng, 2016

M.Sc.

Yi-Wei Tan, 2014
Wen-Ming Zheng, 2014
Xia Du, 2015
Jian-Yang Deng, 2015
Zi-Yang Lin, 2015

R.A.

Yuan Ren, 2017

POST - DOCTORAL FELLOW

U-Fat Chio, 2017
Lei Wang, 2017

SELECTED PUBLICATIONS

- M.-C. Wong, Y.-Z. Yang, C.-S. Lam, W.-H. Choi, N.-Y. Dai, Y.-j. Wu, C.-K. Wong, S.-W. Sin, U-F. Chio, S.-P. U, R.P. Martins, "Self-reconfiguration property of a mixed signal controller for improving power quality compensator during light loading," IEEE Transactions on Power Electronics, Oct. 2015.

- W.-L. Zeng, C.-S. Lam, W.-M. Zheng, S.-W. Sin, N.-Y. Dai, M.-C. Wong, S.-P. U, and R.P. Martins, "DCM operation analysis of KY converter," IET Electronics Letters, Nov. 2015.

- L. Wang, C.-S. Lam, M.-C. Wong, "Unbalanced control strategy for a thyristor controlled LC-coupling hybrid active power filter in three-phase three-wire systems", IEEE Transactions on Power Electronics, Feb. 2017.

- Y.-W. Tan, C.-S. Lam, S.-W. Sin, M.-C. Wong, S.-P. U, and R.P. Martins, "DCM operation analysis of 3-level boost converters," IET Electronics Letters, Feb. 2017.
  L. Wang, C.-S. Lam, M.-C. Wong, "Modeling and parameter design of thyristor controlled LC-coupled hybrid active power filter (TCLC-HAPF) for unbalanced compensation," IEEE Transactions on Industrial Electronics, Mar. 2017.

- L. Wang, C.-S. Lam, M.-C. Wong, "Selective compensation of distortion, unbalanced and reactive power of a thyristor controlled LC-coupling hybrid active power filter (TCLC-HAPF)," IEEE Transactions on Power Electronics, early access.

Man-Kay Law (Matthew)

Assistant Professor
IEEE Senior Member

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RESEARCH INTERESTS

CMOS Image Sensor
CMOS Temperature Sensor
Analog Techniques/Sensor Interface Circuits
Voltage/Current References
Energy Harvesting Circuits and Systems
Switched-Capacitor DC-DC Converters

PROFESSIONAL SERVICES

- TPC Member, ISSCC 2018-Present
- OC/TPC Member, ASP-DAC 2016
- TC Member, IEEE CASS Sensory Systems Technical Committee, 2012-Present
- TC Member, IEEE CASS Biomedical Circuits and Systems Technical Committee, 2012-Present
- RC Member, IEEE Symposium on Circuits and Systems, 2012-Present
- RC Member, IEEE Biomedical Circuits and Systems Conference, 2012-Present

AWARDS

- ISSCC Silkroad Award, IEEE International Solid-State Circuits Conference, 2016 (as co-supervisor)
- ISSCC Student Travel Grant Award, IEEE Solid-State Society, 2015, 2016, 2017 (as supervisor/co-supervisor)
- Best Design Award, Asia and South Pacific Design Automation Conference, 2016 (as co-supervisor)
- A-SSCC Distinguished Design Award, IEEE Asian Solid-State Circuits Conference, 2015 (as co-supervisor)
- Student Paper Award, IEEE International Society for Quality Electronic Design, 2013 (as advisor)

CURRENT GROUP MEMBERS

Ph.D.

Tantan Zhang, 2010
Yang Jiang, 2012
Zhiyuan Chen, 2013
Mingzhong Li, 2015
Jiangchao Wu, 2016
Xin Lu, 2016

M.Sc.

Dapeng Sun, 2015
Ruping Xiao, 2015
Baoyi Cen, 2015
Yukun Xu, 2016

R.A.

Chenyan Cai, 2017

POST - DOCTORAL FELLOW

Kwan-Ting, 2015

SELECTED PUBLICATIONS

- Z. Chen, M.-K. Law, P.-I. Mak, W.-H. Ki and R. P. Martins, "A 1.7mm^2 Inductor-less Fully-Integrated Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting with 483% Power Extraction Enhancement," in IEEE International Solid-State Circuit Conference (ISSCC), pp. 372-373, Feb. 2017.

- Z. Chen, M.-K. Law, P.-I. Mak and R. P. Martins, "A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes with a 67% Charge Pump Maximum Efficiency," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 1, pp. 44-53, Feb. 2017.

- B. Wang, M.-K. Law and A. Bermak, "A Precision CMOS Voltage Reference Exploiting Silicon Bandgap Narrowing Effect," IEEE Transactions on Electron Device, vol. 62, no. 7, pp. 2128-2135, Jul. 2015.

- D. G. Chen, F. Tang, M.-K. Law and A. Bermak, "A 12 pJ/pixel Analog-to-Information Converter based 816 x 640 Pixel CMOS Image Sensor," IEEE Journal of Solid-State Circuits, vol. 49, no. 5, pp. 1210-1222, May 2014.

- Z. Yan, P.-I. Mak, M.-K. Law and R. P. Martins, "A 0.016-mm^2 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With > 0.95-MHz GBW," IEEE Journal of Solid-State Circuits, vol. 48, no. 2, pp. 527-540, Feb. 2013.

Sio Hang Pun
Assistant Professor

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RESEARCH INTERESTS

Biomedical Electronics
Neuroscience Applications
Capacitive Micro-machined Ultrasonic Transducers
Bio-electromagnetism
Intra-body Communication

PROFESSIONAL SERVICES

- Chair, IEEE Engineering on Biology and Medicine Engineering Society (EMBS) Hong Kong and Macau Joint Chapter, 2013
- Executive Committee Member, IEEE Engineering on Biology and Medicine Engineering Society (EMBS) Hong Kong and Macau Joint Chapter, 2012-2017
- Reviewer, IEEE Transaction on Biomedical Engineering
- Reviewer, IEEE Transactions on Ultrasonic, Ferroelectric, and Frequency Control
- Reviewer, IEEE Journal on Biomedical and Health Informatics
- Reviewer, IEEE Engineering on Biology and Medicine Engineering Conference (EMBC), 2009-2017

AWARDS

- 2016 IEEE International Conference on Consumer Electronics- China (ICCE-China 2016) (ICCE-China)
- Best Session Paper Award 2015 (as advisor)

CURRENT GROUP MEMBERS

Ph.D.

Changhao Chen, 2011
Yuanyu Yu, 2011
Jiujiang Wang, 2012
Panke Wang, 2015

M.Sc.

XuiTong Cui, 2015
Xin Lu, 2015

R.A.

U Kin Che, 2012

SELECTED PUBLICATIONS

- X. M. Chen, S. Barma, S. H. Pun, M. I. Vai and P. U. Mak, "Direct Measurement of Elbow Joint Angle Using Galvanic Couple System," IEEE Transactions on Instrumentation and Measurement, vol. 66, no. 4, pp. 757-766, April 2017.

- C. H. Chen, Elizabeth A. McCullagh, S. H. Pun, et al., "An Integrated Circuit for Simultaneous Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation," IEEE Transactions on Biomedical Engineering, vol. 64, no. 3, pp. 557-568, March 2017.

- J. J. Wang, S. H. Pun, et al., "Improved Analytical Modeling of Membrane Large Deflection With Lateral Force for the Underwater CMUT Based on Von Kármán Equations," IEEE Sensors Journal, vol. 16, no. 17, pp. 6633-6640, Sept.1, 2016.

- Y.Y. Yu, S. H. Pun, et al., "Design of a Collapse-Mode CMUT With an Embossed Membrane for Improving Output Pressure," IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 63, no. 6, pp. 854-863, June 2016.

- Gao, Yue-Ming; Wei, Jian-Chong; Mak, Peng-Un; Vai, Mang-I; Du, Min; Pun, Sio-Hang; "Development of a Calibration Strip for Immunochromatographic Assay Detection Systems", Sensors, vol. 16, No. 7, pp.1007-2016

Yan Zhu (Julia)
Assistant Professor

Room 3003e, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4418 I Email: yanzhu@umac.mo

RESEARCH INTERESTS

RF direct-sampled ADC
Pipeline SAR ADC
SAR ADC
SAR Type Reference Voltage
Multi-channels Interleaving Architectures
Stage Gain Calibration
Phase Domain ADC
Clock and PLL for ADC

PROFESSIONAL SERVICES

- Data Converter TPC Member, A-SSCC 2017
- Review of Journal Solid State Circuit
- Review of Transaction of Circuits and Systems I
- Review of Transaction Very Large Scale Integration

AWARDS

- Best Paper Award from IEEE European Solid-State Circuits Conference 2014
- Best Design Award in IEEE A-SSCC 2011 Student Design Contest
- Macau Scientific and Technological R&D Award in 2016
- Macau Scientific and Technological R&D Award in 2014
- Macau Scientific and Technological R&D for Postgraduates Award in 2012
- Chipidea Microelectronic Prize 2011

CURRENT GROUP MEMBERS

Ph.D.

Wang Wei, 2014
Thomas Li, 2015
Wenning Jiang, 2015
Dezhi Xi, 2012

M.Sc.

Wei Lai 2016
Linc Zheng 2016
Zara Zhang, 2016
Victoria Lei, 2016
Luke Wang, 2014
City Li, 2014
Wai-Hong Zhang 2015

POST - DOCTORAL FELLOW

Jankey Zhong, 2017

SELECTED PUBLICATIONS

- Yan Zhu, Chi-Hang Chan, Seng-Pan U, R.P. Martins, "An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1223-1234, May 2016.

- Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, Franco Maloberti, "A 35fJ 10b 160 MS/s Pipelined-SAR ADC with Self-Embedded Offset Cancellation" in IEEE Journal of Solid-State Circuits. Vol. 47, no. 11, pp. 2614 -2626, Nov. 2012.

- Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1111 -1121, Jun 2010.

- Yan Zhu, Chi-Hang Chan, Seng-Pan U, and R.P. Martins, "An 11b 900 MS/s time-interleaved sub-ranging pipelined-SAR ADC," in IEEE European Solid State Circuits Conference (ESSCIRC), pp.211-214, Sept. 2014 (Best Paper Award).

- Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, R.P. Martins, "A 34fJ 10b 500MS/s Partial Interleaving Pipelined-SAR ADC," in IEEE Symposia on VLSI Technology and Circuit (VLSI), pp. 90-91, Jun. 2012.

Chi-Seng Lam (Terence)

Assistant Professor
IEEE Senior Member
IFMA FMP

Room 3012, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4417 I Email: cslam@umac.mo

RESEARCH INTERESTS

Integrated Power Electronics Controllers
Integrated DC-DC Converters
Voltage Reference Circuits
Power Quality Compensators
Renewable Energy
Smart Grid Technology

PROFESSIONAL SERVICES

- Vice-Chair, IEEE Macau Section, 2016 – Present
- Chair, IEEE Macau Section Circuits and Systems (CAS) & Communications (COM) Joint Chapter, 2017 – Present
- Secretary, IEEE Macau Section Power & Energy (PES) & Power Electronics (PELS) Joint Chapter, 2013 – Present
- Local Arrangement Co-Chairs, Asia and South Pacific Design Automation Conference (ASP-DAC 2016)
- Local Arrangement Chair, 2015 IEEE Region 10 Conference (TENCON 2015)
- Invited Speaker, Symposium on Sustainable Development of the Power Industry in Mainland China, Taiwan, Hong Kong and Macau, 2014
- Reviewer, TIE, TPEL, TPWD, TIAS, PEL, EL, GTD, etc.

AWARDS

- Macao Science and Technology Invention Award (Third-Class) 2014
- Macao Science and Technology R&D Award for Postgraduates (Ph.D.) 2012
- 5th National University Students Social Practice and Science Contest on Energy Saving and Emission Reduction (Second Prize) 2012 (as advisor)
- The 3rd Regional Inter-University Postgraduate Electrical and Electronic Engineering Conference Merit Paper Award 2005

CURRENT GROUP MEMBERS

Ph.D.

Ya-Jie Wu, 2012
Wen-Liang Zeng, 2016

M.Sc.

Yi-Wei Tan, 2014
Wen-Ming Zheng, 2014
Xia Du, 2015
Jian-Yang Deng, 2015
Zi-Yang Lin, 2015

R.A.

Yuan Ren, 2017

POST - DOCTORAL FELLOW

U-Fat Chio, 2017
Lei Wang, 2017

SELECTED PUBLICATIONS

- C.-S. Lam, W.-H. Choi, M.-C. Wong, and Y.-D. Han, "Adaptive dc-link voltage controlled hybrid active power filters for reactive power compensation," IEEE Transactions on Power Electronics, Apr. 2012.

- C.-S. Lam, M.-C. Wong, W.-H. Choi, X.-X. Cui, H.-M. Mei, and J.-Z. Liu, "Design and performance of an adaptive low dc voltage controlled LC-hybrid active power filter with a neutral inductor in three-phase four-wire power systems," IEEE Transactions on Industrial Electronics, Jun. 2014 .

- W.-L. Zeng, C.-S. Lam, W.-M. Zheng, S.-W. Sin, N.-Y. Dai, M.-C. Wong, S.-P. U, and R.P. Martins, "DCM operation analysis of KY converter," IET Electronics Letters, Nov. 2015.

- C.-S. Lam, M.-C. Wong, N.-Y. Dai, W.-H. Choi, X.-X. Cui, C.-Y. Chung, "Switching loss reduction technique in active power filters without auxiliary circuits", IET Power Electronics, Mar. 2016.

- Y. -W. Tan, C.-S. Lam, S.-W. Sin, M.-C. Wong, S.-P. U, and R.P. Martins, "DCM operation analysis of 3-level boost converters," IET Electronics Letters, Feb. 2017.

- C.-S. Lam, L. Wang, S.-I. Ho, and M.-C. Wong, "Adaptive thyristor controlled LC - hybrid active power filter for reactive power and current harmonics compensation with switching loss reduction," IEEE Transactions on Power Electronics, early access.

Jun Yin
Assistant Professor

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RESEARCH INTERESTS

Low-Power CMOS Wireless Transceivers for IoT Application
mm-Wave CMOS Transceivers for Radar Application
Analog and Digital PLLs
Integrated Oscillators

PROFESSIONAL SERVICES

- Secretary, IEEE CAS Macau Chapter, 2017

CURRENT GROUP MEMBERS

Ph.D.

Xingqiang Peng, 2014
Haidong Yi, 2015
Shiheng Yang, 2015

M.Sc.

Tongquan Jiang, 2014
Iat Fai Sun, 2015
Jinan Luo, 2017

POST–DOCTORAL FELLOW

Yatao Peng, 2016

R.A.

Chee Cheow Lim, 2017

SELECTED PUBLICATIONS

- J.Yin, P. -I. Mak, F. Maloberti and R. P. Martins, "A 0.003mm^2 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f^3 Phase-Noise Corner," in IEEE International Solid- State Circuit Conference (ISSCC), Feb, 2016.

- J.Yin, P. -I. Mak, F. Maloberti and R. P. Martins, " A Time-Interleaved Ring-VCO with Reduced 1/f^3 Phase Noise Corner, Extended Tuning Range and Inherent Divided Output," in IEEE Journal of Solid-State Circuits (JSSC), Dec. 2016.

- W. -H.Yu, H.Yi, P. -I. Mak, J.Yin and R. P. Martins, "A 0.18V 382μW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS," in IEEE International Solid- State Circuit Conference (ISSCC), Feb, 2017.

- X. Peng, J.Yin, P. -I. Mak, W. -H.Yu and R. P. Martins, "A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) Pout," in IEEE Journal of Solid-State Circuits (JSSC), 2017.

- H.Yi, J.Yin, P. -I. Mak, R. P. Martins, "A 0.032-mm^2 0.15-V 3-Stage Charge-Pump Scheme Using a Differential Bootstrapped Ring-VCO for Energy-Harvesting Applications," IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II), 2017.

Yan Lu
Assistant Professor

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RESEARCH INTERESTS

Wireless Power Transfer Circuits and Systems
Analog and Digital Low-Dropout Regulators
Fully-Integrated DC-DC Converters
RF Energy Harvesting
Voltage and Current References

PROFESSIONAL SERVICES

- Review Committee Member, IEEE ISCAS 2016, 2017
- TPC Member, IEEE VLSI-DAT 2017
- Special Session Chair of IEEE APCCAS 2016
- UDC Committee Co-Chair of IEEE ASP-DAC 2016
- Technical Program Sub-Committee Co-Chair of IEEE International Wireless Symposium 2015 & 2016
- Reviewer of IEEE JSSC, TCAS-I, TCAS-II, TPEL, TBioCAS, TVLSI, EDL, etc.

AWARDS

- IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award 2013-14
- IEEE TENCON Professional Award 2015 (as advisor)
- HKUST School of Engineering PhD Fellowship 2013
- HKUST School of Eng. Overseas Research Award 2012
- Outstanding Postgraduate Student of Guangdong (Canton) Province 2008

CURRENT GROUP MEMBERS

Ph.D.

Fangyu Mao, 2015
Xiaofei Li, 2016
Jie Lin, 2016

M.Sc.

Ziyang Luo, 2014
Yuanqing Huang, 2015
Yulun Wu, 2016

R.A.

Xiaofei Ma, 2016
Hesheng Lin, 2016

SELECTED PUBLICATIONS

- Y. Lu, X. Li, W.-H. Ki, C.-Y. Tsui, and C. P. Yue, "A 13.56MHz Fully Integrated 1X/2X Active Rectifier with Compensated Bias Current for Inductively Powered Devices," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2013.

- Y. Lu, W.-H. Ki, and C. P. Yue, "A 0.65ns-Response-Time 3.01ps FOM Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power-Supply-Rejection for Wideband Communication Systems," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2014.

- Y. Lu, J. Jiang, W.-H. Ki, C. P. Yue, S.-W. Sin, S.-P. U, and R. Martins, "A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2015.

- M. Huang, Y. Lu, S.-P. U, and R. P. Martins, "A Reconfigurable Bidirectional Wireless Power Transceiver with Maximum Current Charging Mode and 58.6% Battery-to-Battery Efficiency," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2017.

- M. Huang, Y. Lu, S.-P. U, and R. P. Martins, "An Output-Capacitor-Free Analog-Assisted Digital Low-Dropout Regulator with Tri-loop Control," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2017.

Yanwei Jia
Assistant Professor

Room 3001, 3/F, N21, University of Macau, Taipa, Macau, China
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RESEARCH INTERESTS

Digital Microfluidics Development
Microfluidics for Disease Diagnostics
Digital Microfluidics for Point-of-Care Testing
Digital Microfluidics for Biological Applications

AWARDS

- Innovation Prize, International Organization for Biological Crystallization, 2008
- Outstanding Mentor Award, Ministry of Education of Singapore, 2004

CURRENT GROUP MEMBERS

R.A.

Wan Liang, 2016

Ph.D.

Cheng Dong, 2012 (co-supervisor)

M.Sc.

Haoran Li, 2016

POST - DOCTORAL FELLOW

Jie Gao, 2016
Tianlan Chen, 2017

SELECTED PUBLICATIONS

- Cheng Dong, Yanwei Jia, Jie Gao, Tianlan Chen, Pui In Mak, Mang I Vai, R. P. Martins, "A 3D microblade structure for precise and parallel droplet splitting on digital microfluidic chips", Lab on a Chip, Feb-2017.

- Tianlan Chen, Yanwei Jia, Cheng Dong, Jie Gao, Pui In Mak, R. P. Martins, "Sub-7-second genotyping of single-nucleotide polymorphism by high-resolution melting curve analysis on a thermal digital microfluidic device", Lab on a Chip, Jan-2016.

- Yanwei Jia, J. A. Sanchez, L. J. Wangh, "Kinetic Hairpin Oligonucleotide Blockers for Selective Amplification of Rare Mutations", Scientific Reports, Jan-2014.

- Yanwei Jia, Pui In Mak, C. Massey, R. P. Martins, L. J. Wangh, "Construction of a microfluidic chip, using dried-down reagents, for LATE-PCR amplification and detection of single-stranded DNA", Lab on a Chip, Jan-2013.

- Yanwei Jia, A. Osborne, J. E. Rice, L. J. Wangh, "Dilute-'N'-Go Dideoxy Sequencing of All DNA Strands Generated in Multiplexed LATE-PCR Assays", Nucleic Acids Research, Jan-2010.

Yong Chen
Assistant Professor

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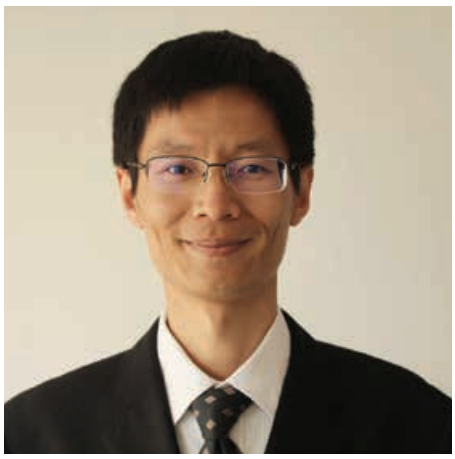


RESEARCH INTERESTS

Filter and Amplifier
VCO and Its Phase Noise Theory
RF/mm-wave System and Circuit
On-Chip and Chip-to-Chip Electrical/Optical Interconnects
Ultra-High-Speed Wireline
Data and Clock Jitter Analysis

PROFESSIONAL SERVICES

- Reviewer of the conferences and journals (ISCAS, APCCAS, IEEE TMTT, TCAS-I, TCAS-II, TVLSI, IET EL, etc.)

CURRENT GROUP MEMBERS

Ph.D.

Chao Fan, 2016

M.Sc.

Lei Zhao, 2016
Xi Meng, 2016
Xinyi Ge, 2016
Shaocan Fan, 2016

R.A.

Wei Zhu, 2017

SELECTED PUBLICATIONS

- Y. Chen, P.-I. Mak, L. Zhang, H. Qian, Y. Wang, "A Fifth-Order 20-MHz Transistorized-Ladder LPF With 58.2-dB SFDR, 68-μW/Pole/MHz Efficiency, and 0.13-mm2 Die Size in 90-nm CMOS", IEEE Transactions on Circuits and Systems – II, Jan-2013.

- Y. Chen, P.-I. Mak, L. Zhang, H. Qian, Y. Wang, "Pre-Emphasis Transmitter (0.007mm^2, 8Gbit/s, 0-14dB) with Improved Data Zero-Crossing Accuracy in 65nm CMOS", IET Electronics Letters, Jul-2013.
  Y. Chen, P.-I. Mak, S. D'Amico, L. Zhang, H. Qian, Y. Wang, "A Single-Branch Third-Order Pole–Zero Low-Pass Filter With 0.014-mm2 Die Size and 0.8-kHz (1.25-nW) to 0.94-GHz (3.99-mW) Bandwidth–Power Scalability", IEEE Transactions on Circuits and Systems – II, Nov-2013.

- Y. Chen, P.-I. Mak, L. Zhang, Y. Wang, "A 0.002-mm^2 6.4-mW 10-Gb/s Full-Rate Direct DFE Receiver with 59.6% Horizontal Eye Opening at 10-12 BER under 23.3-dB Channel Loss at Nyquist", IEEE Transactions on Microwave Theory and Techniques, Dec-2014.

- Y. Chen, P.-I. Mak, Y. Wang, "A Highly-Scalable Analog Equalizer Using a Tunable and Current-Reusable Active Inductor for 10-Gb/s I/O Links", IEEE Transactions on Very Large Scale Integration Systems, May-2015.

Chi-Hang Chan (Ivor)
Assistant Professor

Room 3003d, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4402 I Email: ivorchan@umac.mo

RESEARCH INTERESTS

Multibit SAR ADC
Flash ADC
Time domain-assisted ADC
SAR Reference Error Calibration
Comparator
Comparator Offset Calibration
Time-Interleaved ADC
CT/DT DSMs

PROFESSIONAL SERVICES

- Review of Journal Solid State Circuit
- Review of Transaction of Circuits and Systems I
- Review of Transaction of Circuits and Systems II
- Review of Transaction Very Large Scale Integration

AWARDS

- IEEE Solid-State-Circuit Society Pre-doctoral Achievement Award 2015
- Best Paper Award from IEEE European Solid-State Circuits Conference 2014 (2nd Author)
- Best Design Award in IEEE A-SSCC 2011 Student Design Contest (2nd Author)
- Macau Scientific and Technological R&D Award in 2016
- Macau Scientific and Technological R&D Award in 2014
- Macau Scientific and Technological R&D for Postgraduates Award in 2014

CURRENT GROUP MEMBERS

M.Sc.

Zara Zhang, 2016
Victoria Lei, 2016
Luke Wang, 2014
City Li, 2014
Wai-Hong Zhang 2015
Wei Lai 2016
Linc Zheng 2016

POST - DOCTORAL FELLOW

Wang Wei, 2014
Thomas Li, 2015
Wenning Jiang, 2015
JainWei Liu, 2012

SELECTED PUBLICATIONS

- Chi-Hang Chan, Yan Zhu, Iok-Meng Ho, Wai-Hong Zhang, Seng-Pan, U., Martins, R.P., "A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with background offset calibration," in IEEE International Solid-State Circuits Conference (ISSCC), pp. 282-283, Feb 2017

- Chi-Hang Chan; Yan Zhu; Sai-Weng Sin; Seng-Pan, U.; Martins, R.P., "A 5.5mW 6b 5GS/S 4×-interleaved 3b/cycle SAR ADC in 65nm CMOS," in IEEE International Solid-State Circuits Conference - (ISSCC), pp.1-3, Feb 2015.

- Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U and R.P. Martins, "A 5.5mW 6-b 5GS/s 4-Interleaved 3b/cycle SAR ADC in 65nm CMOS," in IEEE Journal of Solid-State Circuits, Vol. 51, no. 2, pp. 365-377, Feb. 2016.

- Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, "A 5b 1.25GS/s 4X Capacitive Folding Flash ADC in 65nm CMOS," in IEEE Journal of Solid-State Circuits , Vol. 48, no. 9, pp. 2154 -2169, Sep. 2013.

- Chi-Hang Chan, Yan Zhu, Iok-Meng Ho, Wai-Hong Zhang, Chon-Lam Lio, Seng-Pan, U., Martins, R.P., "A 0.011mm^2 60dB SNDR 100MS/s reference error calibrated SAR ADC with 3pF decoupling capacitance for reference voltages," in IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 145-148, Nov. 2016. (Highlighted Paper).

Ka-Fai Un

UM Macao Fellow (Lecturer)
Visiting Researcher, UCD, Dublin, Ireland

Room 3006, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4450 I Email: kafaiun@umac.mo

RESEARCH INTERESTS

Radio frequency integrated circuits
Wideband transmitters
Harmonic rejection mixers
Switched capacitor filters
Radio frequency digital-to-analog converters

PROFESSIONAL SERVICES

- Reviewer, IEEE Transactions on Circuits and Systems I: Regular Papers
- Reviewer, IEEE Transactions on Circuits and Systems II: Express Briefs
- Reviewer, IEEE International Symposium on Circuits and Systems – ISCAS

AWARDS

- Scientific and Technological R&D Award (PhD Student), Macau Science and Technology Award 2012
- Certificate of Merit, IEEE Asia-Pacific Conference on Circuits and Systems – APCCAS'2008, Macao, China.

CURRENT GROUP MEMBERS

Ph.D.

Wei-Han Yu, 2012
Chak-Fong Cheang, 2012
Gengzhen Qi, 2013

SELECTED PUBLICATIONS

- Ka-Fai Un, Wei-Han Yu, Chak Fong Cheang, Gengzhen Qi, Pui In Mak, R. P. Martins, "A Sub-GHz Wireless Transmitter Utilizing a Multi-Class-Linearized PA and Time-Domain Wideband-Auto I/Q-LOFT Calibration for IEEE 802.11af WLAN", IEEE Transactions on Microwave Theory and Techniques, Oct-2015.

- Chak Fong Cheang, Ka-Fai Un, Wei-Han Yu, Pui In Mak, R. P. Martins, "A Combinatorial Impairment-Compensation Digital Predistorter for a Sub-GHz IEEE 802.11af-WLAN CMOS Transmitter Covering a 10x-Wide RF Bandwidth", IEEE Transactions on Circuits and Systems – I, Apr-2015.

- Ka-Fai Un, Pui In Mak, R. P. Martins, "A 53-to-75 mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS", IEEE Journal of Solid-State Circuits, Aug-2013.

- Wei-Han Yu, Chak-Fong Cheang, Pui In Mak, Weng-Fai Cheng, Ka-Fai Un, U-Wai Lok, R. P. Martins, "A Nonrecursive Digital Calibration Technique for Joint Elimination of Transmitter and Receiver I/Q Imbalances With Minimized Add-On Hardware", IEEE Transactions on Circuits and Systems – II, Aug-2013.

Ka Meng Lei

UM Macao Fellow (Lecturer)

Visiting Researcher, Harvard U, Cambridge, MA, USA

Room 3006, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4432 I Email: kamenglei@umac.mo

EDUCATION

PhD, ECE, University of Macau, 2016
BS, EEE, University of Macau, 2012

EXPERIENCES

- Visiting scholar, Harvard University, Cambridge, MA, Jun. 2017 (2 years)
- Lecturer (UM Macao Fellow), University of Macau, Macau, Dec. 2016 - now
- Research assistant, University of Macau, Macau, Sept. 2012 – Nov. 2016
- Trainee, Evatronix SA, Poland, Jun. 2012 – Jul. 2012

RESEARCH INTERESTS

Analog and RF circuit techniques for micro-NMR
Sensors and analog front-end interfaces
System planning and integration for biomedical devices
Low-power and low-voltage oscillator design

PROFESSIONAL SERVICES

- Reviewer of Analytical Methods
- Reviewer of International Journal of Circuit Theory and Applications
- Reviewer of International Symposium of Circuits and Systems

AWARDS

- IEEE Solid-State Circuits Society - Pre-Doctoral Achievement Award 2017
- FDCT Macao Science and Technology Award for Postgraduates 2016 (Ph.D. level)
- IEEE international Solid-State Circuits Conference - Silkroad Award 2016
- IEEE Asian Solid-State Circuits Conference - Distinguished Design Award 2015
- Chemical and Biological Microsystems Society - Student/Young Researcher Grant 2015
- Asia Symposium on Quality Electronic Design - Best Paper Award 2013

SELECTED PUBLICATIONS

- K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti, and R. P. Martins, "A handheld high-sensitivity micro-NMR CMOS platform with B-field stabilization for multi-type biological/chemical assays," IEEE J. Solid-State Circuits, vol. 52, no. 1, pp. 284-297, Jan. 2017.

- K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A μNMR CMOS transceiver using a Butterfly-coil input for integration with a digital microfluidic device inside a portable magnet," IEEE J. Solid-State Circuits, vol. 51, no. 10, pp. 2274-2286, Oct. 2016.

- K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "CMOS biosensors for in vitro diagnosis - transducing mechanisms and applications," Lab Chip, vol. 16, no. 19, pp. 3664-3681, Oct. 2016.

- K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti, and R. P. Martins, "A handheld 50pM-sensitivity micro-NMR CMOS platform with B-field stabilization for multi-type biological/chemical assays," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), 2016, pp. 474–475.

- K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A palm-size μNMR relaxometer using a digital microfluidic device and a semiconductor transceiver for chemical/biological diagnosis," Analyst, vol. 140, no.15, pp. 5129-5137, Aug. 2015.

SKL-AMSV Main Research Lines

Wireless IC

Prof. Pui-In Mak, Research Line Coordinator

This research line focuses on RF and mmWave ICs for a wide variety of applications, including but not limited to, 3G/4G/5G multi-standard cellular radios, ultra-low-cost ultra-low-power IoT radios, and tens-of-MHz radios for micro-nuclear magnetic resonance (μNMR) applications. The key research interests are:

- Sub-6GHz 2G/3G/4G wireless transceiver front-ends, and >28GHz 5G transceiver front-ends. SAW-less RF-flexible receivers and transmitters using our proposed gain-boosted N-path filter techniques are investigated.
- Ultra-low-power IoT transceiver front-ends from sub-GHz to 2.4GHz, conforming to Bluetooth Low Energy (BLE), ZigBee and NB-IoT. Ultra-low-cost and ultra-low-power RF and baseband (BB) techniques using our proposed function-reuse gain-boosted N-path receiver, RF-to-BB-current-reuse receiver, function-reuse VCO-PA, and ultra-low-voltage receiver, transmitter and frequency synthesizer using a local micro-power manager are investigated.
- Analog baseband circuits such as micro-power amplifiers with high capacitive load drivability, continuous-time/discrete-time filters with a very compact chip area, energy-harvesting units with high efficiency, sensor readout interfaces with low noise effective factor, and crystal oscillators with low startup energy are investigated.
- RF/mmWave circuits such as active-inductor-enhanced wideband amplifiers, multi-harmonic-peaking wave-shaping VCOs, time-interleaved ring oscillators with a wide tuning range, and type-I phased-locked loops with ultra-low-voltage operation are investigated.
- Digital baseband correction techniques for I/Q mismatch, LO feedthrough and strong-memory-effect distortion in wideband transmitters are investigated.
- Tens-of-MHz (e.g., 20MHz) transceivers with a sensing coil (on/off-chip spiral inductor) to allow electronic-automated biological and chemical assays in a small form factor.

The invented techniques are expected to advance the state-of-the-art knowledge in the fields, and should be potentially transferrable to the industry for practical applications.

Data Conversion and Signal Processing

Prof. Sai-Weng Sin, Research Line Coordinator

The main objective of the research line is focus on innovations on high-performance data conversion and signal processing analog ICs, including those covering the most emerging applications e.g. 4G LTE, LTE-A, Ultra Low Power IoT devices, wideband (wirelined- or optical communication), etc. The following lists the key research interests:

- Power efficient data converters for portable and autonomous IoT system. The projects are based on the dynamic based circuits, like inverters, comparators, successive approximation register (SAR), binary search ADC etc. to achieve very low power consumption data converter implementation.
- Digitally-assisted / calibrated high resolution CMOS data converters for high quality video, cellular and data acquisition front-ends. This projects study the innovation that relies on the advanced scaling nanometer CMOS technology that bring the strong processing power of digital circuits, to assist the detection and calibration of the various analog circuit non-idealities like offset/gain errors, nonlinearity, various mismatch among different channels, etc.
- Oversampling noise-shaped sigma-delta converter for wireless applications. This project concentrates on the innovation techniques improving the noise-shaping performance in the discrete-time and continuous-time sigma-modulator modulator.
- Ultra wide bandwidth data converters for optical communications. This project investigates different techniques to extend the bandwidth physical limits in the data converter. The possible direction includes the interleaving with calibration or compensation of various mismatches, and utilize the time-based converters to take advantages of technology scaling.
- Application of data converters in various electronics application including sensors, power converters and navigation systems. This project focused more on the application aspect of the data converters. Current projects include the design of sensing interface for power electronics converters, and an accelerometer/velocity meter/position meter sensing analog sigma-delta front-end interface for navigation systems.

SKL-AMSV Associate Research Lines

Biomedical IC

Prof. Mang-I Vai, Research Line Co-Coordinator
Prof. Pui-In Mak, Research Line Co-Coordinator

The research line focuses on advanced micro/hybrid systems that can be applicable to human beings, biological and chemistry researches. The key research interests are:

- Advanced electronics platform for small animal behavioral study. Miniaturized circuit/SoC for simultaneous extracellular electrophysiology recording and optogenetic neural manipulation is studied.
- Micro ultrasound transducer for biological imaging and measurement. New membrane structure CMUT is designed and fabricated based on MEMS technology to enhance the output ultrasonic pressure. Multi-frequency CMUT is investigated to extend the imaging capability of photoacoustic imaging.
- Intra-body Communication with study in physical layer and MAC layer and their IC implementation.
- Microprocessor with built in multi-tasking ability for biomedical engineering applications. This can be used as a platform for ASIC development for related applications.
- Ultra-low-power energy harvesting CMOS biomedical implantable sensing chip. Single-chip energy harvesting solution with various ambient sources for low voltage operation, high efficiency and ultra-compact form factor are investigated.
- Ultra-low power biopotential interfacing circuit. Nanowatt analog signal processing and filtering is studied, focusing on nanowatt circuit design, subthreshold operation, linearity improvement and gain compensation.
- Digital microfluidic chips with software-defined intelligence. On-chip 3D structures for precise droplet splitting, fuzzy-logic and real-time feedback for precise droplet positioning, and non-DC driving voltage waveforms for higher droplet moving speed are investigated.

The invented techniques are expected to advance the state-of-the-art in terms of performances and understanding, and should be transferrable to the industry for practical applications.

Integrated Power

Prof. Man-Chung Wong, Research Line Co-Coordinator
Prof. Sai-Weng Sin, Research Line Co-Coordinator

The research directions are:

- Integrated power electronics controller design

  The integrated power electronics controller can significantly improve the power electronics system performances and is easy to be implemented by others (without knowledge and save programming time) compared with conventional DSP controller. Moreover, the integrated power electronics controller is possible to replace the digital controller in the power compensator products. This research work focuses on programmable gain signal conditioning circuit, analog-to-digital (A/D) conversion, and pulse-width-modulation (PWM) generator. Up to now, there is no such three-phase power electronics controller IC in the market.

- Power management IC design

  Fully-integrated high efficiency, wide input range, wide load current range, small output ripple, and fast transient response power management circuits, including inductor-based and switched-capacitor DC-DC converters, low dropout regulators, etc. are of great interest.

- Wireless power transfer

  Wireless power transfer (WPT) has a wide range of applications including (arranged from low to high power levels) radio frequency identification (RFID), internet-of-things (IoT), implantable medical devices (IMDs), real-time wireless power for non-contact memory devices and wafer-level testing, and also wireless chargers for portable/wearable devices and electric vehicles (EVs). It is evident that the utilization of WPT technologies is on the critical point of exponential growth.

The research line aimed at the investigation of the advantages of using microelectronics through signal processing and intelligence in order to improve the performance of energy processing power electronics systems, which is related with software control and hardware IC implementation. Power management and wireless power transfer are our research focuses.

THESES AWARDED

Ph.D. (18)

Arshad Hussain

High-Resolution Passive and Active-Passive Switched-Capacitor Delta-Sigma Modulator Design Techniques in Nanoscale CMOS, 2017
Assistant Professor, Quaid-i-Azam University, Islamabad, Pakistan

Lei WANG

Design and Implementation of a Three-Phase Three-Wire Thyristor Controlled LC-Coupling Hybrid Active Power Filter with Low DC-link Voltage and Wide Compensation Range, 2017
Post-Doc, University of Macau, Macao

Tianlan CHEN

Thermal Digital Microfluidic Devices for Rapid DNA Analysis, 2016
Research Assistant, University of Macau, Macao

Ka-Meng LEI

Handheld CMOS-Based NMR Devices for Biological/Chemical Diagnosis, 2016
Macau-fellow, University of Macau, Macao

Chio-In IEONG

Low-Power CMOS Processors Design for ECG QRS Wave Detection and Data Compression, 2016
Senior Engineer, Hisilicon, China

Jianyu ZHONG

High-resolution Power-efficient SAR-Type ADCs, 2016
Post-Doc, University of Macau, Macao

Ximei CHEN

Channel Characteristics and Communication Performance of Galvanic Coupling Human Body Communication, 2016

Jie GAO

Electronic-Automated Intelligent Digital Microfluidic System and its Applications to DNA Amplification, 2015
Laboratory Technician, University of Macau, Macao

Tawfiq AMIN

Analysis and Design of Power-Efficient Voltage-Controlled Oscillators for Wireless Applications in Nanoscale CMOS, 2015
Assistant Professor, Military Institute of Science & Technology (MIST), Dhaka, Bangladesh

Yaohua ZHAO

Low-Power, High-Linearity and Area-Efficient Switched Capacitor Filters Design Techniques in Nanoscale CMOS, 2015
Senior Design Engineer, Mediatek, Singapore

Fujian LIN

Advanced Circuit Design Techniques for Low-Power Wideband Wireless Receivers in Nanoscale CMOS, 2014
Senior Design Engineer, Mediatek, Singapore

Zhicheng LIN

Ultra-Low-Power and Ultra-Low-Cost Short-Range Wireless Receivers in Nanoscale CMOS, 2014
Senior Design Engineer, Qualcomm, USA

Zushu YAN

Systematic Design and Implementation of Single-Stage and Multi-Stage CMOS Amplifiers, 2014
Senior Design Engineer, Qualcomm, USA

Ka-Fai UN

New Architectures and Circuit Design Techniques for TV-Band White-Space Wireless Transmitters, 2014
Macau-fellow, University of Macau, Macao

Chi-Hang CHAN

Design Techniques and Considerations in Moderate to Low Resolution Power efficient GHz Range ADCs, 2015
Research Assistant Professor, University of Macau, Macao

U-Fat CHIO

Design Techniques for Low-Power High-Speed Analog-to-Digital Converters using Binary-Search and Subranging Schemes, 2012 Post-Doc, University of Macau, Macao

Yan ZHU

Circuit Techniques for High-Performance SAR-Type ADCs, 2011
Assistant Professor, University of Macau, Macao

Hegong WEI

High Speed Power/Area Optimized Multi-Bit/Cycle SAR ADCs, 2011
Engineer, Silicon Lab, USA

THESES AWARDED

M.Sc. (51)

Yuan REN

On the study of High DR Multi-Channel Stage-Shared Hybrid Front-End for Integrated Power Electronics Controller, 2016
Research Assistant, University of Macau, Macao

Wei LI

On the study of Mixed Signal Interface Circuit for Inertial Navigation System, 2016

Wen-Liang ZENG

Design and control of an integrated ky dc-dc step-up converter under dcm operation, 2016
Ph.D., University of Macau, Macao

Sut-Ian HO

Study of a combined system of thyristor controlled LC filter and hybrid active power filter, 2016
Facilitator of Telecommunication Exhibition, Communications Museum of Macao, Macao

Sanfeng LU

High Accuracy Multi-Range Ultra-Low Power/Non-Calibrated CMOS Smart Temperature Sensor Design, 2016
Design Engineer, Jia Chi Microelectronics Technology, China

Haojuan DAI

A Wide Input Range CMOS Rectifier Design for RF Energy Harvesting, 2016
Design Engineer, Solomon Systech, China

Baoning ZHANG

Cross-Correlation Phase Counting Method Using FPGA Implementation for Digital Frequency Domain Fluorescence Lifetime Imaging Microscopy, 2016
IT Engineer, Macau Tai Fung Bank, Macao

Haodong YAO

Novel Enveloped-Morphology Heart Sound Feature Extraction for Intelligent Cardiovascular Disease Prognosis in e-Home Healthcare, 2016

Wai-Kei TOU

Improved Montion Control System on Elevator Landing and Re-leveling, 2016

Haiyang WANG

Diagnose CVDs through Detecting Heart Sounds, 2016

Fei YUAN

A 10b Pipelined ADC with Nonlinear Digital Background Calibration & 2.5b/stage Opamp Sharing Architecture, 2015
Design Engineer, Synopsys Macau, Macao

Suyan FAN

AA Wide-Input-Range Supply Voltage Tolerant Capacitive Sensor Readout Using On-Chip Solar Cell, 2015
Design Engineer, Allwinner Technology, China

Yue LI

Joint-Digital-Predistortion for Wireless Transmitter's I/Q Imbalance and PA Nonlinearities Using an Asymmetrical Complexity-Reduced Volterra Series Model, 2015
Ph.D., Ryerson University, Canada

Choi-Fong NGAI

Predicting Protein Docking Poses on a Solid Surface by Particle Swarm Optimization: a Case Study of Lysozyme on PTFE, 2015
Ph.D., University of Macau, Macao

Wang MENG

Towards Improving Performance of Galvanic Coupling Intra-Body Communication, 2015

Cao-Xue WEN

Acoustic Output Pressure Enhancement for CMUTs Using Helmholtz Resonance Principle, 2015

Huijuan HUANG

FPGA Implementation of Synthetic Aperture Algorithm for Ultrasound Imaging, 2015

Mubo CHEN

Disease-Oriented Hierarchical CVDs Diagnosis Hemodynamic, Symptomatic and Physiological Parameters, 2015

Chon-In LAO

Semi-MASH Sigma-Delta A-to-D Converter for High-Speed High-Resolution Applications, 2014
Design Engineer, Synopsys Macau, Macao

Jiangchao WU

An Ultra-Low Power Acquisition Front-End for Neural Recording, 2014
Ph.D., University of Macau, Macao

THESES AWARDED

M.Sc. (CONTINUED)

Xingqiang PENG

Advanced Circuit Techniques for Class-D Power Amplifiers in Nanoscale CMOS, 2014
Ph.D., University of Macau, Macao

Wei WANG

Systematic Analysis and Design of Area-Efficient Frequency Compensation Techniques for Micropower Two-Stage CMOS Amplifiers, 2014

Ming-Zhong LI

Sub-threshold Standard Cell Library Design for Ultra-Low Power Biomedical Applications, 2014
Ph.D., University of Macau, Macao

Yan-Zheng YANG

Design and implementation of a mixed signal controller for power quality compensator improvement, 2014
Project Manager, China National Water Resource & Electric Power Materials & Equipment Co, Ltd., China

Bo JIN

Law Detection and Localization in Steel Material by the EEMD-HSA Based Technique in Ultrasonic Nondestructive Testing, 2014

Du YUN

On the Study of Improving Noise Shaping Techniques in Wide Bandwidth Sigma Delta Modulators, 2013

Wenlan WU

Monotonic Multi-Switching Method for Ultra-Low-Voltage Energy Efficient SAR ADCs, 2013
Engineer, Alphacore Inc., USA

Cheok-Teng LEI

Applying the Novel High Speed Robust Level Converter to a 12-bit Successive Approximation Analog-to-Digital Converters with Dual Supply Domain, 2013
Design Engineer, Synopsys Macau, Macao

Chenyan CAI

On the Study of Excess-Loop-Delay Compensation Techniques in Continuous-Time Delta-Sigma Modulators, 2013
Research Assistant, University of Macau, Macao

Tao WU

An Ultra-Low Power CMOS Smart Temperature Sensor for Clinical Temperature Monitoring, 2013
Technical Consultant, Huada Empyrean, China

Gengzhen QI

Design and Optimization of Wideband Power Amplifier and its Driver Circuits, 2013
Ph.D., University of Macau, Macao

Tianlan CHEN

Design and Implementation of Intelligent Digital Microfluidics Systems, 2013
Ph.D., University of Macau, Macao

Zhiyuan CHEN

Single-Chip Solar Energy Harvesting IC with Integrated Solar Cells for Biomedical Application, 2013
Ph.D., University of Macau, Macao

Yanjie XIAO

Capacitance-to-Digital Convert for Lab-on-Chip Digital Microfluidics Systems and Ultra-Low-Power SAR ADC with Effective Calibration, 2012
Senior Engineer, Schaeffler, China

Weng-Fai CHENG

A Wideband Balun Low-Noise Amplifier and Digital Impairment Correction Techniques for Wireless Transmitters, 2012
Engineer, CTM, Macao

Wei-Han YU

Digital Predistortion and Calibration Techniques for Wireless Transmitters, 2012
Ph.D., University of Macau, Macao

Jiang YANG

On the Study of Clock-Jitter Insensitive Circuit Techniques in Continuous-Time Sigma-Delta Modulators, 2012
Ph.D., University of Macau, Macao

Zhijie CHEN

Ultra-Low Power Sigma-Delta ADC for Biomedical Readout Front-End, 2012
Assistant Professor, Beijing University of Posts and Telecommunications, China

THESES AWARDED

M.Sc. (CONTINUED)

Wang RUI

Digital Calibration Techniques for Cyclic Analog-to-Digital Converter, 2012
Ph.D., University of Idaho, US

Peng ZHANG

Calibration of Timing-Skew error in Analog-to-Digital Converter, 2012
Engineer, Marvell Semiconductor, China

Wai-Hei CHOI

Low Loss and Dynamic Reactive Power Compensation Control Algorithms for Three-Phase Four-Wire Hybrid Active Power Filters, 2012
Laboratory Technician, University of Macau, Macao

Xiao-Xi CUI

Control and Minimization of DC-Link Voltage for Three-Phase Four-Wire Hybrid Active Power Filters, 2012
Research Assistant, University of Macau, Macao

Chong-Yin FOK

Very Short Term Load Forecasting for Macau Power System, 2012

Dong CHENG

Electrocardiogram Parameter Extract and Analysis System, 2011
Ph.D., University of Macau, Macao

Mia LIU

High-Voltage-Enabled Operational Amplifier and Active-Decoupling Technique for Wideband Balun-LNA, 2011
Engineer, STMicroelectronics, China

Cheng-Man NG

Electroencephalogram Analysis Based on Empirical Mode Decomposition, 2011

Chin-Chong HO

From Vehicle Black Box System to Elevator Event Data Recorder, 2011

Guohe YIN

Ultra-Low Power SAR ADC for Biomedical Application, 2011
Chinese Academy of Sciences, China

Chi-Hang CHAN

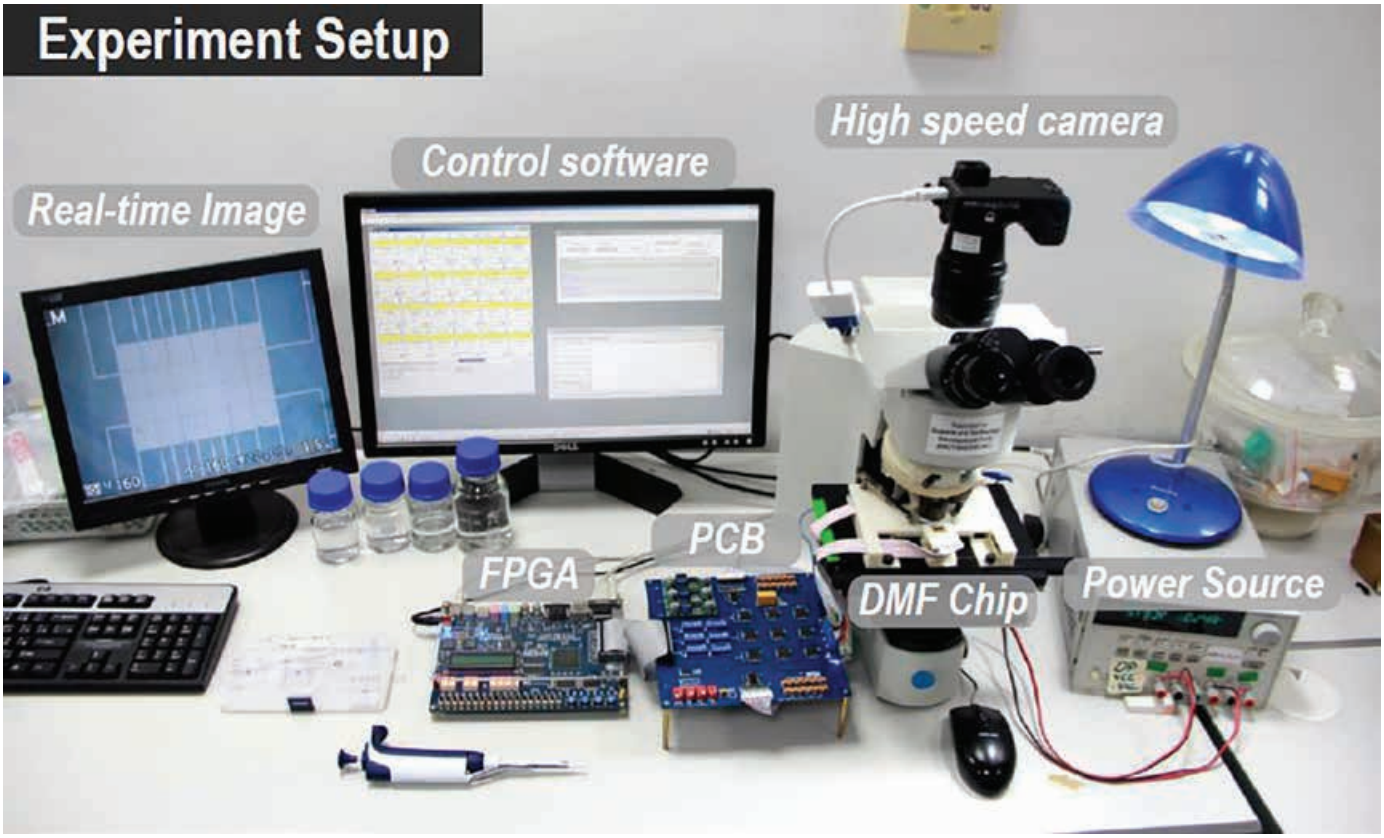
A Study on Comparator and Offset Calibration Techniques in High Speed Nyquist ADCs, 2011
Ph.D., University of Macau, Macao

Si-Seng WONG

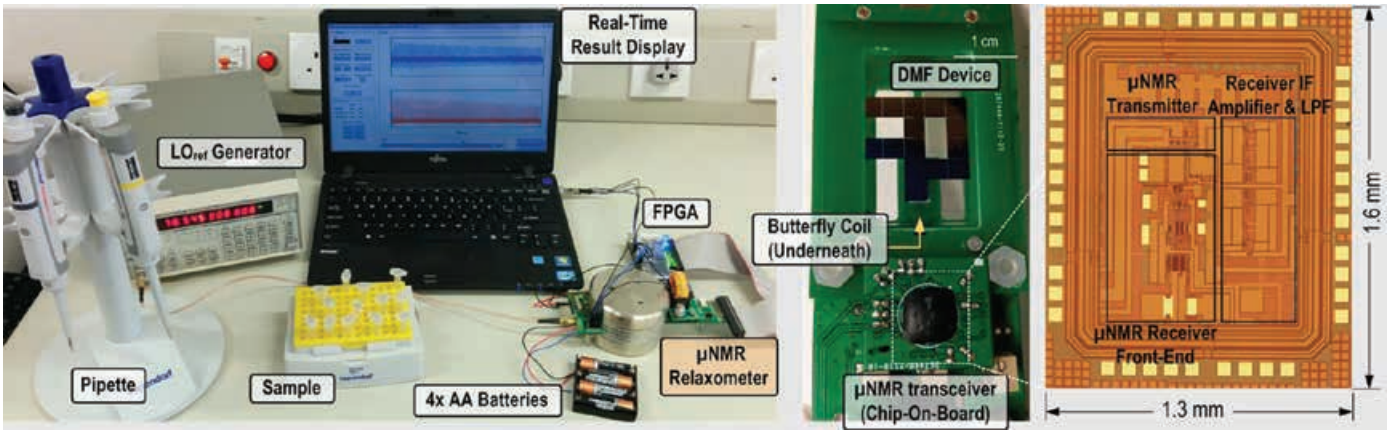
Design of Analog-to-Digital Converters with Binary Search Algorithm and Digital Calibration Techniques, 2011
Design Engineer, Synopsys Macau, Macao

Bo SUN

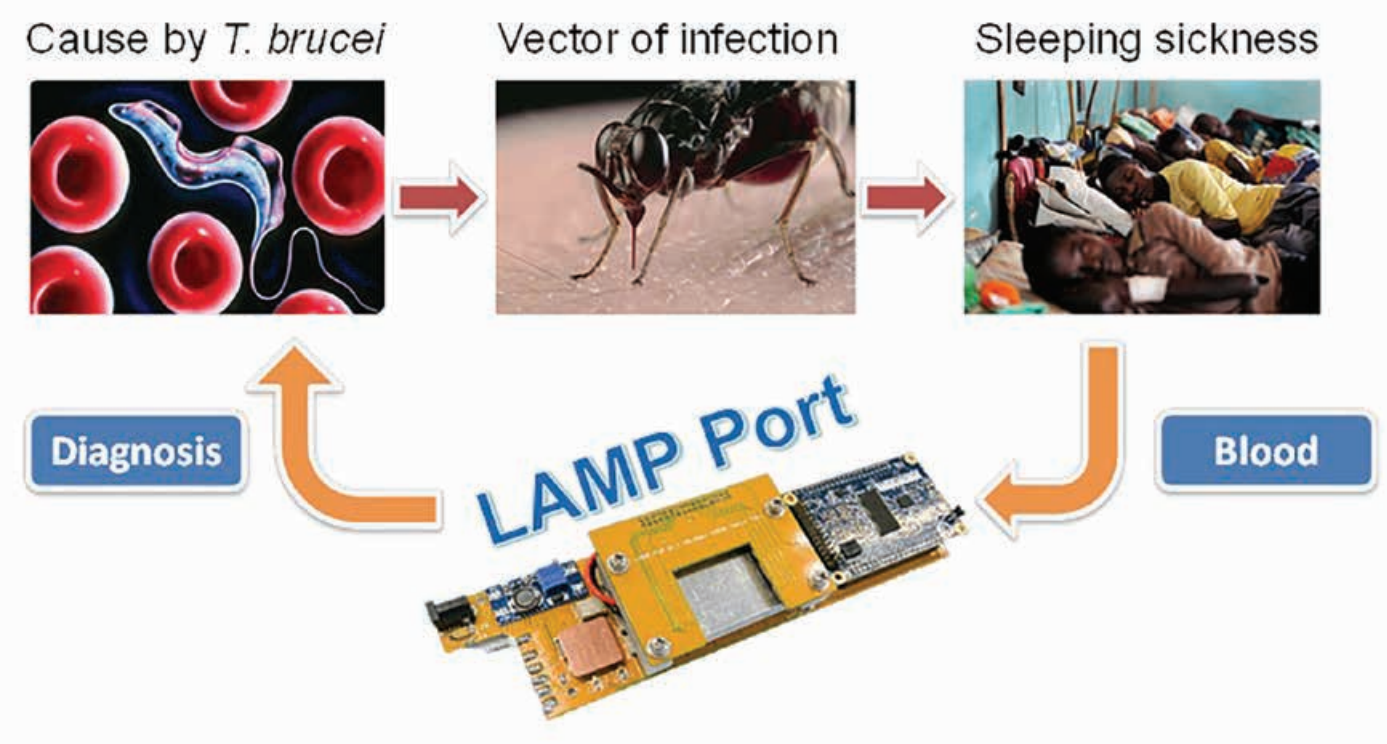
A FPGA-Based Power Electronics Controller for Three-phase Four-wire Hybrid Active Power Filters, 2011

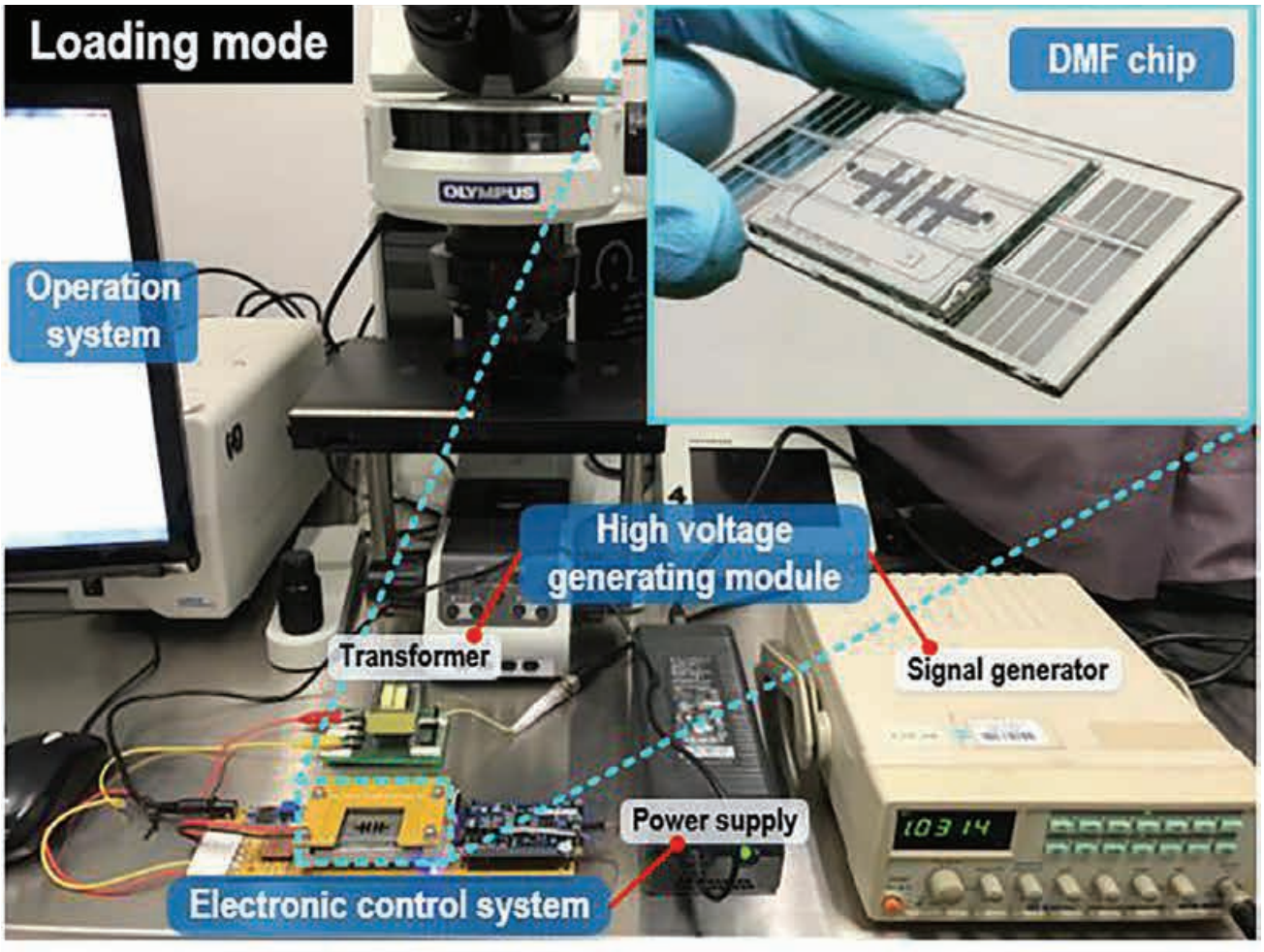


Experimental setup of an electronic-automated digital microfluidic system.



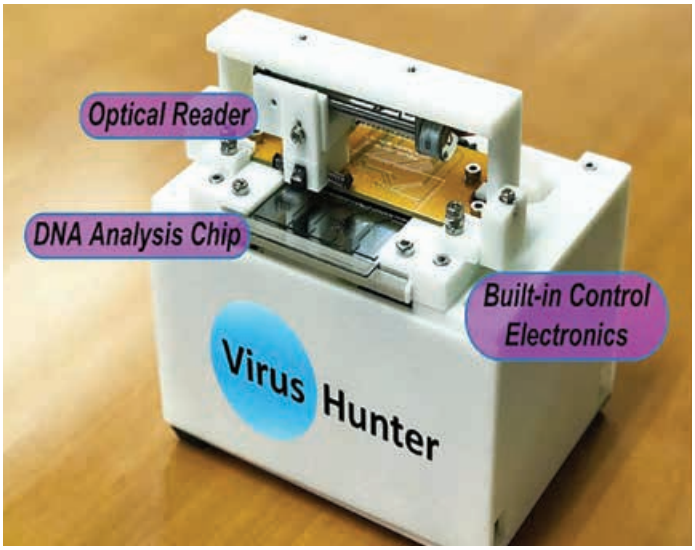
Experimental setup of a nuclear magnetic resonance (NMR)-digital microfluidic system.



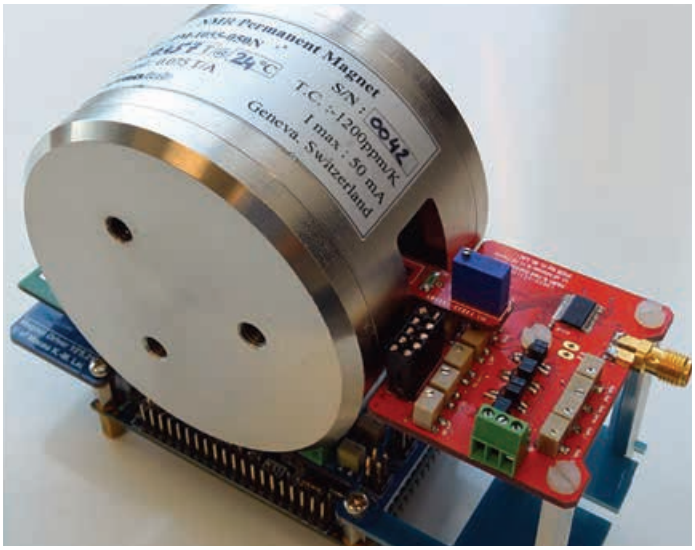


Application overview and experimental setup of a portable DNA analyzer (LAMP Port).

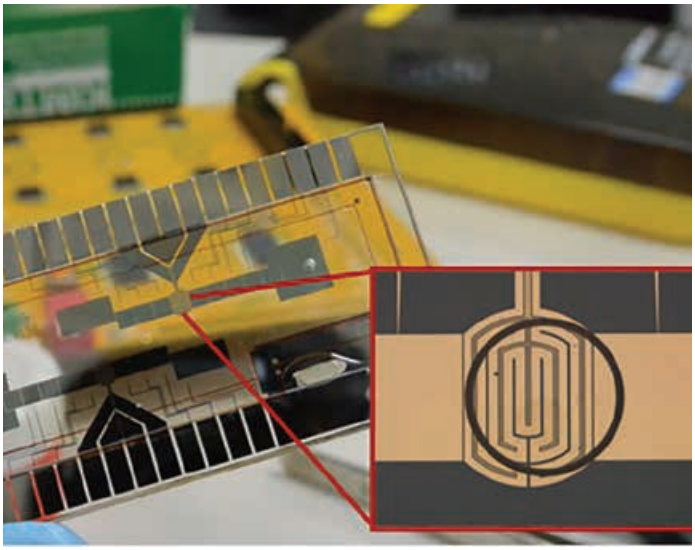
SAMPLE PROTOTYPES



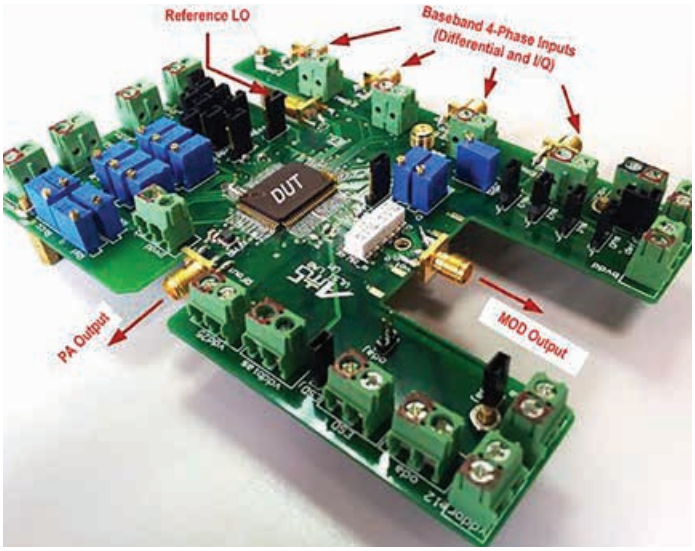
Portable real-time DNA analyzer (Virus Hunter).



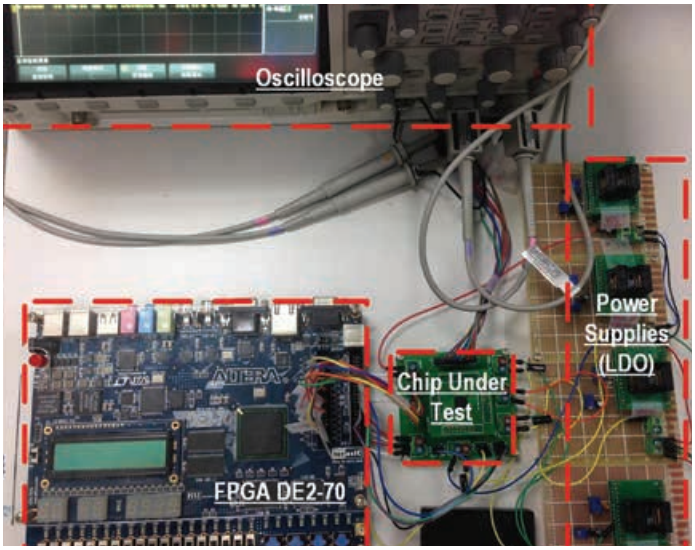
NMR CMOS platform with B-field stabliziation.



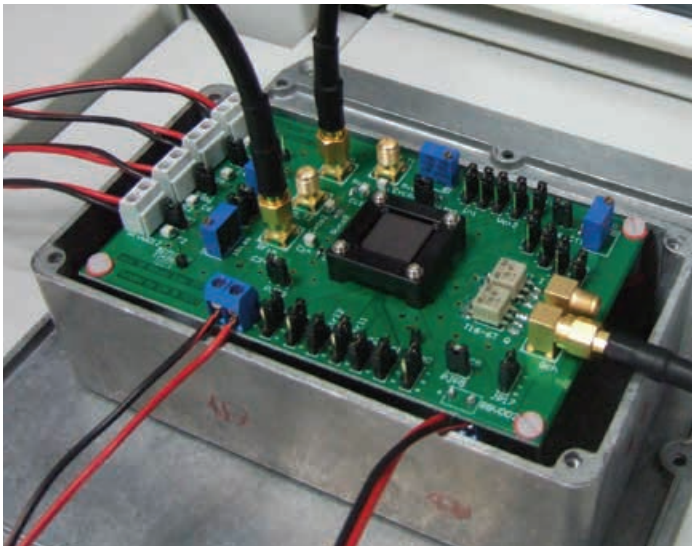
Thermal digital microfluidic chip.



Sub-GHz TV-band whitespace transmitter.

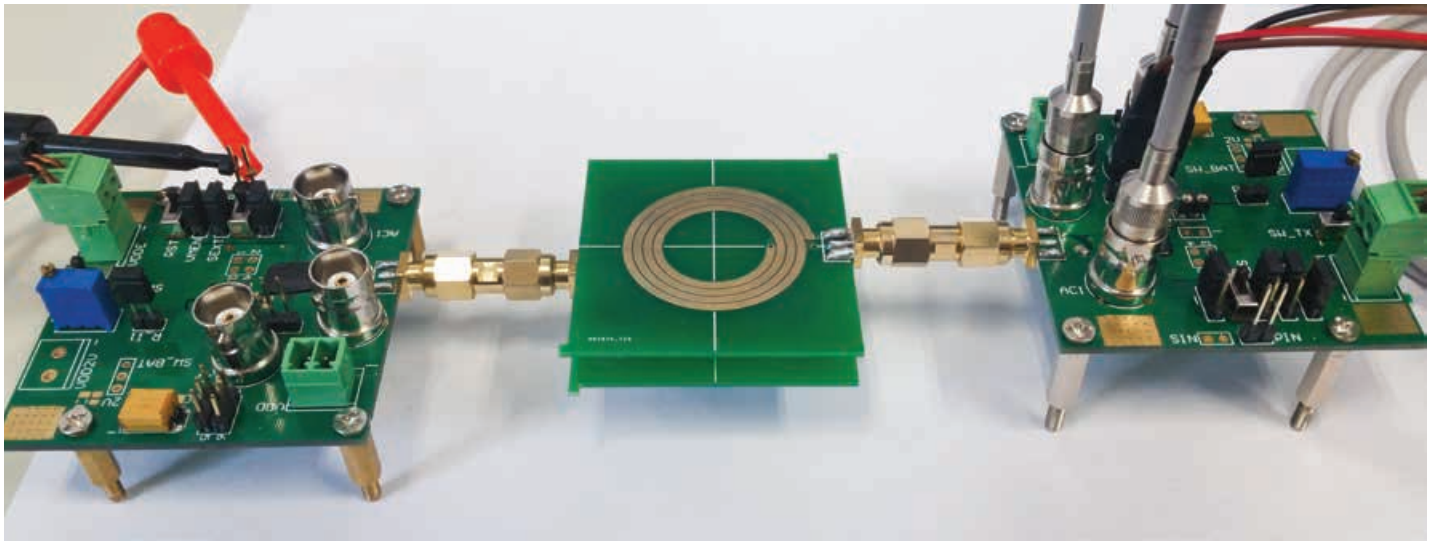


Measurement setup of the energy efficient subthreshold digital logic library prototype.

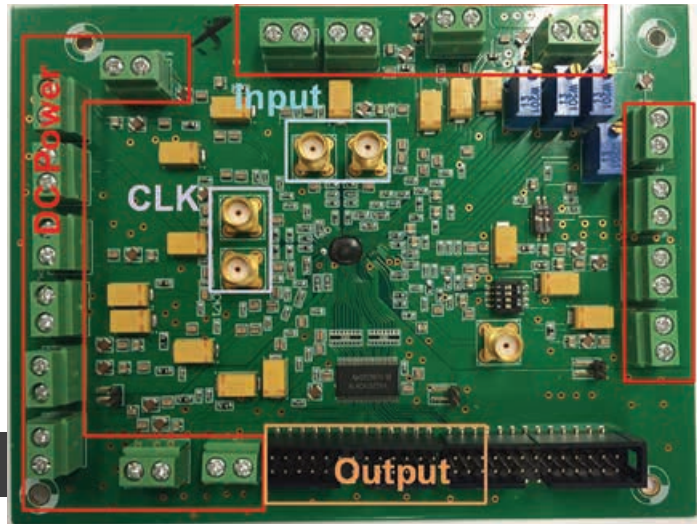


Full-band mobile-TV receiver.

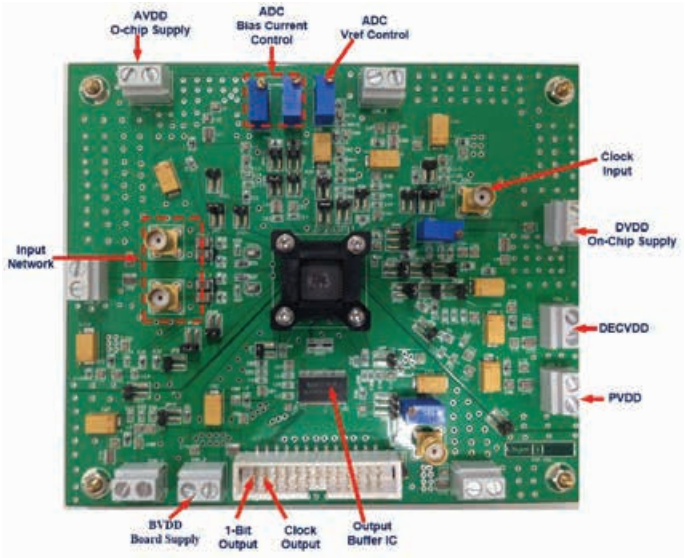
SAMPLE PROTOTYPES



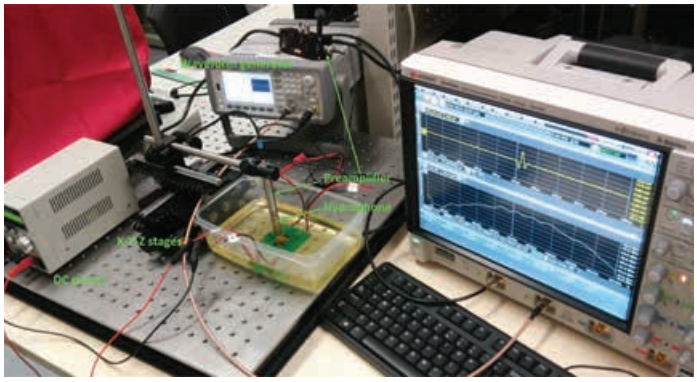
Measurement setup of a reconfigurable bidirectional wireless power transceiver system.



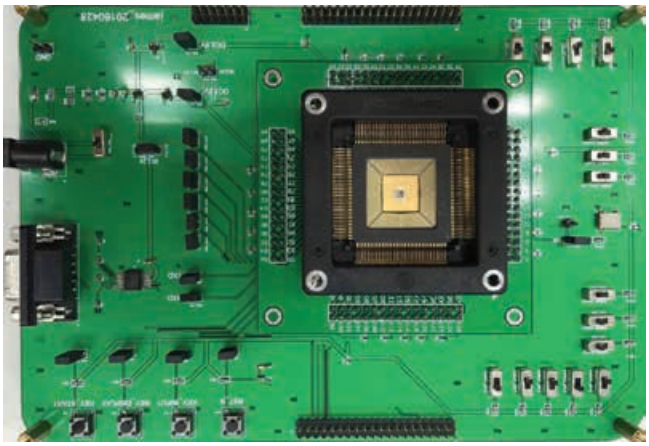
High speed high resolution ADC prototype.



Prototype test board for an Audio Sigma Delta ADC.



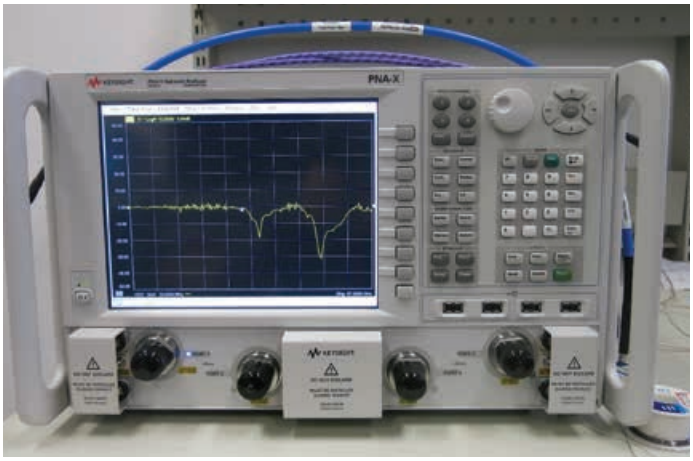
Experimental setup for measuring the output pressure of the CMUT.



Test board for the power electronics controller IC

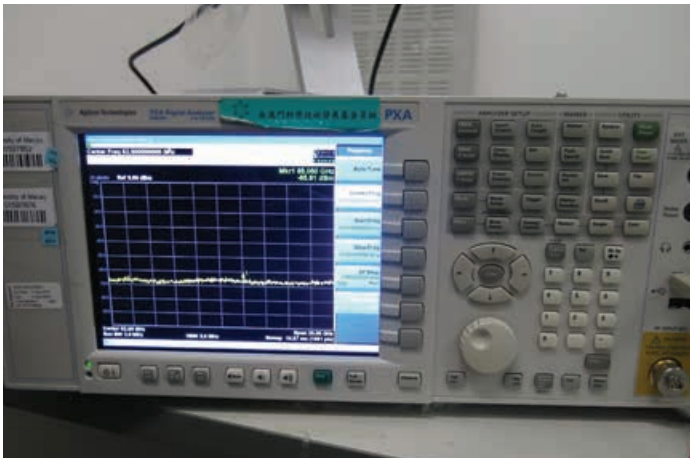
Measurement rooms with different testing equipment.

Keysight 16802A 68 channel, 4 GHz timing, 250 MHz state Logic Analyzer

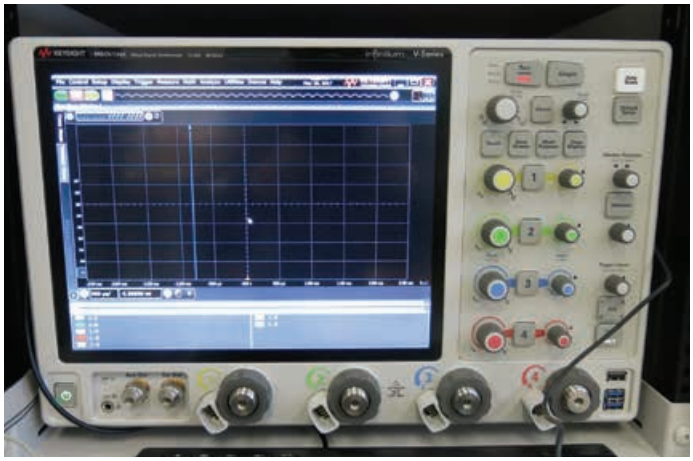


N5247A 67 GHz PNA-X 4 ports, dual source Microwave Network Analyzer

N6705B DC Power Analyzer Mainframe with precision DC power module



Keysight N9030A 50GHz PXA High Performance Signal Analyzer



MSOV134A 13 GHz, 4 Analog Plus 16 Digital Channels Mixed Signal Oscilloscope

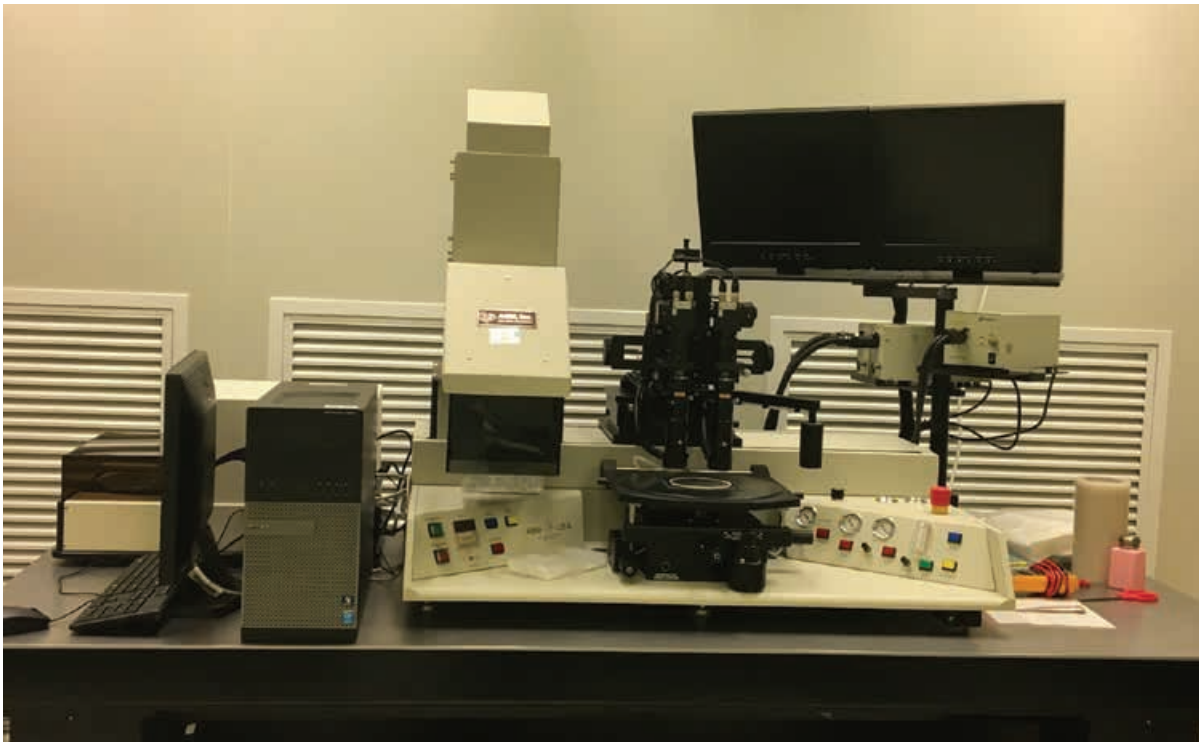
Keysight B1500A Semiconductor Device Parameter Analyzer/Semiconductor Characterization System Mainframe

Cascade PM5 Manual Analytical Probe Station/Base Machine and with SGS and SGSGS probes up to 65GHz

Cleanroom (Class 1000)

Wet Laboratory

Fluorescence Microscopes



ABM Manual High Resolution Mask Aligner and UV Exposure System

TESTING EQUIPMENT AND FACILITIES

CORE SWITCH:

- H3C 10508 x 2: Switching capacity 1.5Tbps

STORAGE: EMC ISILON: CAPACITY:

- 194TB, 7 nodes and 140Gbps parallel data connections

CLOUD COMPUTING SERVERS:

- Over 60 servers and 250 PC clients, 1256 CPU cores and 5TB RAM in total, can run 150 multi-core microelectronics imulations simultaneously

SOFTWARE AND EDA TOOLS:

- Cadence: Custom Integrated Circuits Bundle (80 licenses), Digital Integrated Circuits Bundle (20 licenses)
- Mentor Graphics: Nanometer design bundle (30 licenses)
- Synopsys: Front-end University Bundle (35 licenses)
- Sonnet Professional with Floating Network License with High-Performance Solver Engine
- Matlab and Simulink

ISSCC 2011

1. A 0.46mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65nm CMOS
2. A 0.024mm² 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65nm CMOS

ISSCC 2012

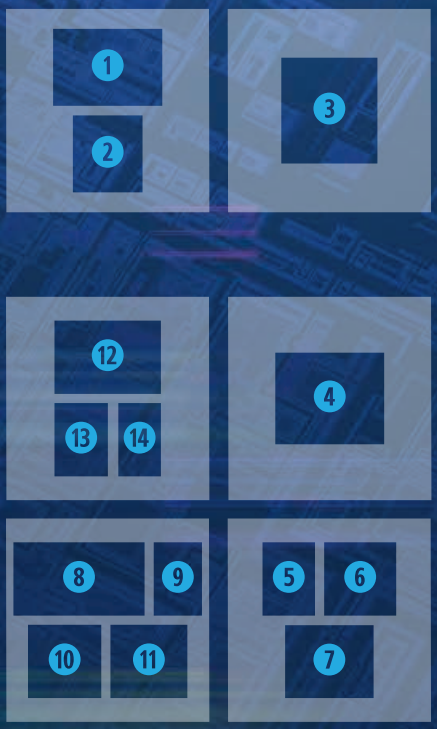
3. A 0.016mm² 144μW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load with >0.95MHz GBW

ISSCC 2013

4. A 1.7mW 0.22mm² 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer+Hybrid Filter Topology in 65nm CMOS

ISSCC 2014

5. A 0.0013mm² 3.6μW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Loads with >62° Phase Margin
6. An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF
7. A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components



ISSCC 2015

8. A 5.5mW 6b 5GS/s 4×-Interleaved 3b/cycle SAR ADC in 65nm CMOS
9. A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement
10. A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors
11. A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S_{11} Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF

ISSCC 2016

12. A 0.038mm² SAW-less Multi-Band Transceiver Using an N-Path SC Gain Loop
13. A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz $1/f^3$ Phase Noise Corner
14. A Handheld 50pM-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays

ISSCC: IEEE International Solid-State Circuits Conference

State Key Laboratory of Analog and Mixed-Signal VLSI

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UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

Research Report 2011-2016

State Key Laboratory of Analog and Mixed-Signal VLSI
University of Macau