RESEARCH ABSTRACTS
POWER MANAGEMENT AND CONDITIONING CIRCUITS

An Analog-Assisted Digital Low-Dropout Regulator with Tri-Loop Control

Mo Huang, Yan Lu, Seng-Pan U, and Rui P. Martins

FEATURES

Analog-assisted loop for instant transient response
Tri-loop control for reducing number of shift-registers
Output capacitor free
Freeze mode for low quiescent current, 3.2μA
Nonlinear coarse word control for glitch reduction
Silicon verified in TSMC 65nm GP CMOS

DESCRIPTION

Low-dropout regulators (LDOs) are widely distributed in SoC designs to supply individual voltage domains, and digital LDO (DLDO) is favorable for its low-voltage operation and process-scalability. However, as many SoCs generate a load current variation at sub-A/ns level, voltage regulators require a large area-consuming output capacitor (C_{OUT}) to maintain the output voltage (V_{OUT}) during fast transients. Conventional shift-register (SR) based DLDO suffers from a power and speed trade-off, thus requires a large C_{OUT}. Fig.1 shows the proposed AA technique in addition to the SR-based DLDO. The V_{SSB} nodes of the driving inverters of the power switches are not connected to Gnd as usual, but AC-coupled to V_{OUT} through a coupling capacitor C_C and DC-biased to Gnd with R_C. This forms an AA loop for bandwidth-extension and instant response.

Fig. 2 shows the overall architecture of the proposed AA-DLDO. A 9bit PMOS switch array is implemented for better V_{OUT} accuracy. This array is divided into 3 sub-sections (low, medium, and high) with carry-in/out between each other. These sub-sections are made of L, M, and H SR-bits respectively. A tri-loop control, including the 1) AA, 2) coarse- and 3) fine-tuning, is implemented. The driving inverters are sized proportionally to their corresponding switch strengths, and all the V_{SSB} nodes are AC-coupled to V_{OUT}. Besides, the coarse tuning is made by the medium and high SRs. The medium SR, triggered by a dead-zone comparator (DZ), outputs carry-in/out signals to drive the High SR. The fine tuning only composes of the low sub-section fed by a 1-bit quantization comparator (CMP). All these SRs are clock-gated for power loss reduction.

A nonlinear coarse word control for glitch reduction is also proposed, for details, please read the paper.

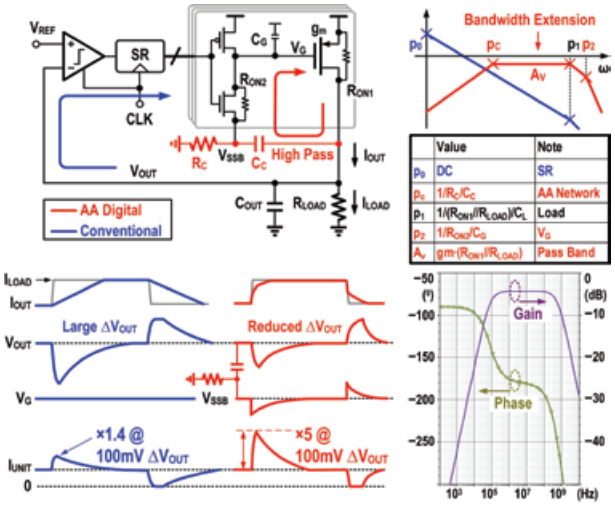


Fig. 1. AA-DLDO scheme and the poles of the AA loop; the transient waveforms of the AA and conventional schemes; and, the Bode plot of the AA loop.

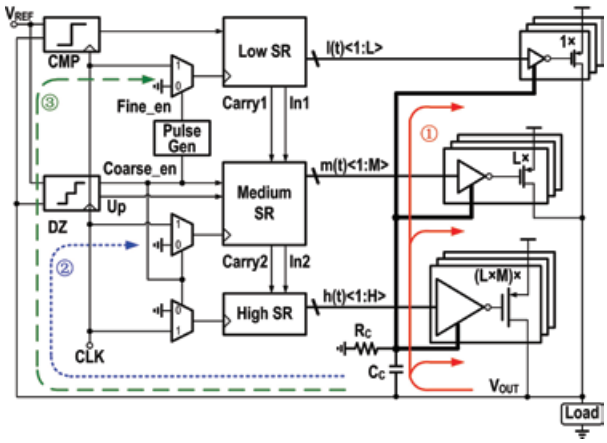


Fig. 2. Overall architecture of the proposed AA-DLDO, with the AA, coarse tuning, and fine tuning loops.

Publication(s):

[1] M. Huang, Y. Lu, S. P. U, and R. P. Martins, "An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control," in IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 342–343.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Dual-Symmetrical-Output Switched-Capacitor Converter with Dynamic Power Cells and Minimized Cross Regulation for Application Processors

Junmin Jiang, Yan Lu, Wing-Hung Ki, Seng-Pan U, and Rui P. Martins

FEATURES

Dual-symmetrical-output for reduced area overhead
Dynamic power cell reallocation for higher efficiency
Power density, 150mW/mm^2
Peak efficiency, 83.3%
Silicon verified in GF 28nm bulk CMOS

DESCRIPTION

Multi-core application processors in smart-phone/-watch require multiple voltages for each core. Highly-efficient fully integrated switched-capacitor (SC) converters that require zero external component, are promising candidates in these applications. Fig.1 shows the strategy of the shared power cells and dynamic allocation. The two outputs (V_{OUT1} and V_{OUT2}) are regulated by frequency modulation. So that the frequencies (f_1 and f_2) reflect the loading demands of each outputs. Assume the two channels start with the same no. of power cells, when the load of channel 1 (Ch1) is larger than that of channel 2 (Ch2), resulting $f_1 > f_2$, then more power cells will then be assigned to Ch1. That means the physical boundary of the two channels will go right, until f_1 and f_2 are close to each other. The dynamic allocation can balance the load demands by trying to operate at the optimized frequency with all the power cells, thus the switching and parasitic losses are reduced.

The number of power cells is designed to be 82 and work with interleaving-phase to reduce ripple. To enable the allocation with minimum the cross regulation, a dual-path VCO is proposed.

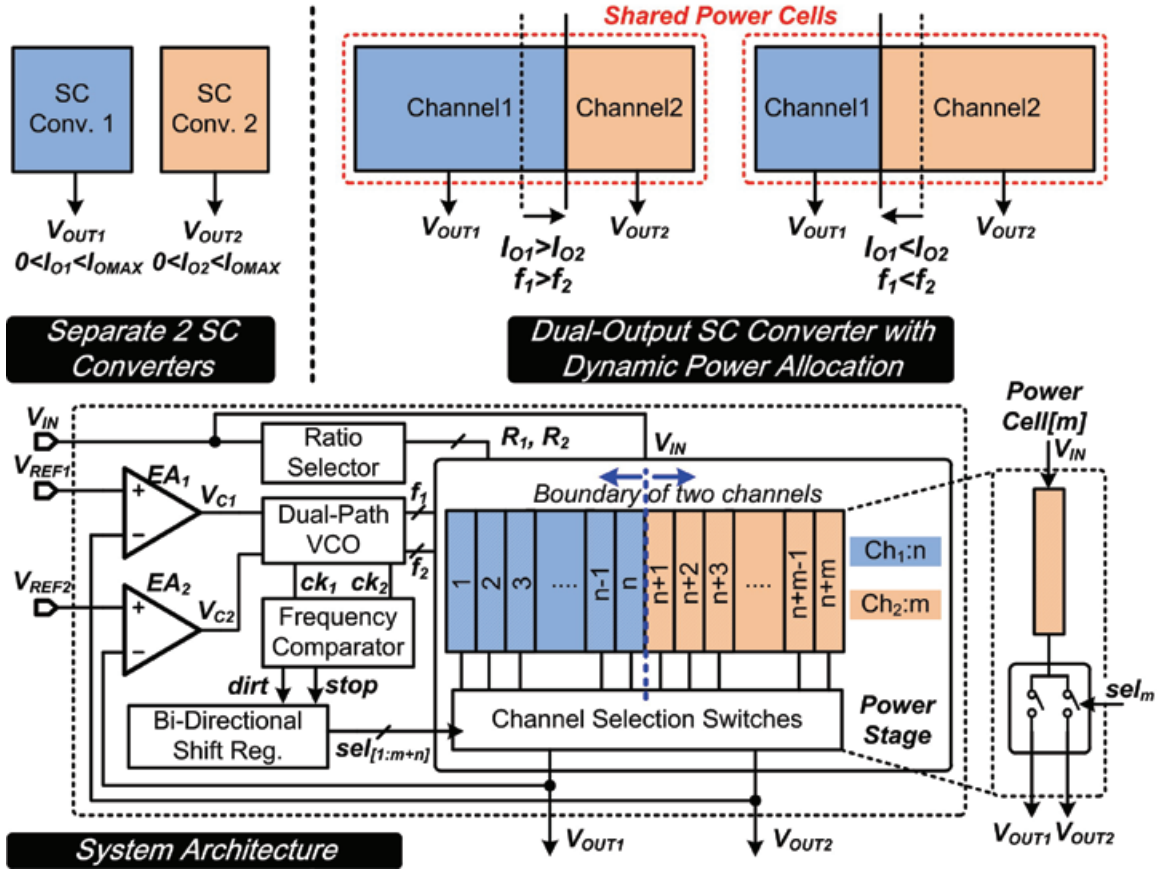


Fig. 1. Strategy of dynamic power-cell allocation and system architecture of proposed dual-output SC converter.

Publication(s):

[1] J. Jiang*, Y. Lu*, W. H. Ki, S. P. U*, and R. P. Martins*, "A dual-symmetrical-output switched-capacitor converter with dynamic power cells and minimized cross regulation for application processors in 28nm CMOS," in IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 344–345.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Research Grant Council of Hong Kong

A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors

Yan Lu, Junmin Jiang, Wing-Hung Ki, C. Patrick Yue, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Fast transient response, 3ns
Fast reference tracking, 2.5V/μs
75.8% efficiency at 0.13W/mm^2 power density
Silicon verified in UMC 65nm LL CMOS process

DESCRIPTION

Inspired by The Square of Vatican City, a fully-integrated step-down switched-capacitor DC-DC converter-ring with 100+ phases is designed with a fast-DVS (dynamic voltage scaling) feature for the microprocessor in portable/wearable devices. As shown in Fig. 1, this symmetrical ring-shaped converter surrounds its load in the square and supplies the on-chip power grid, such that a good quality power supply can be easily accessed at any point of the chip edges. There are 30 phases on the top edge and 31 phases on each of the other 3 edges, making 123 phases in total. The phase number and unit cell dimensions of this architecture can easily be adjusted to fit the floor plan of the load.

The pads of the converter-ring are placed at the corners, and will not affect the pads of the load. Moreover, by using the proposed V_{DD}-controlled oscillator (V_{DD}CO) the frequency of which is controlled by varying its supply voltage, a hitherto unexplored feature of the multiphase DC-DC architecture is exposed: the control-loop unity gain frequency (UGF) could be designed to be a few times higher than the switching frequency.

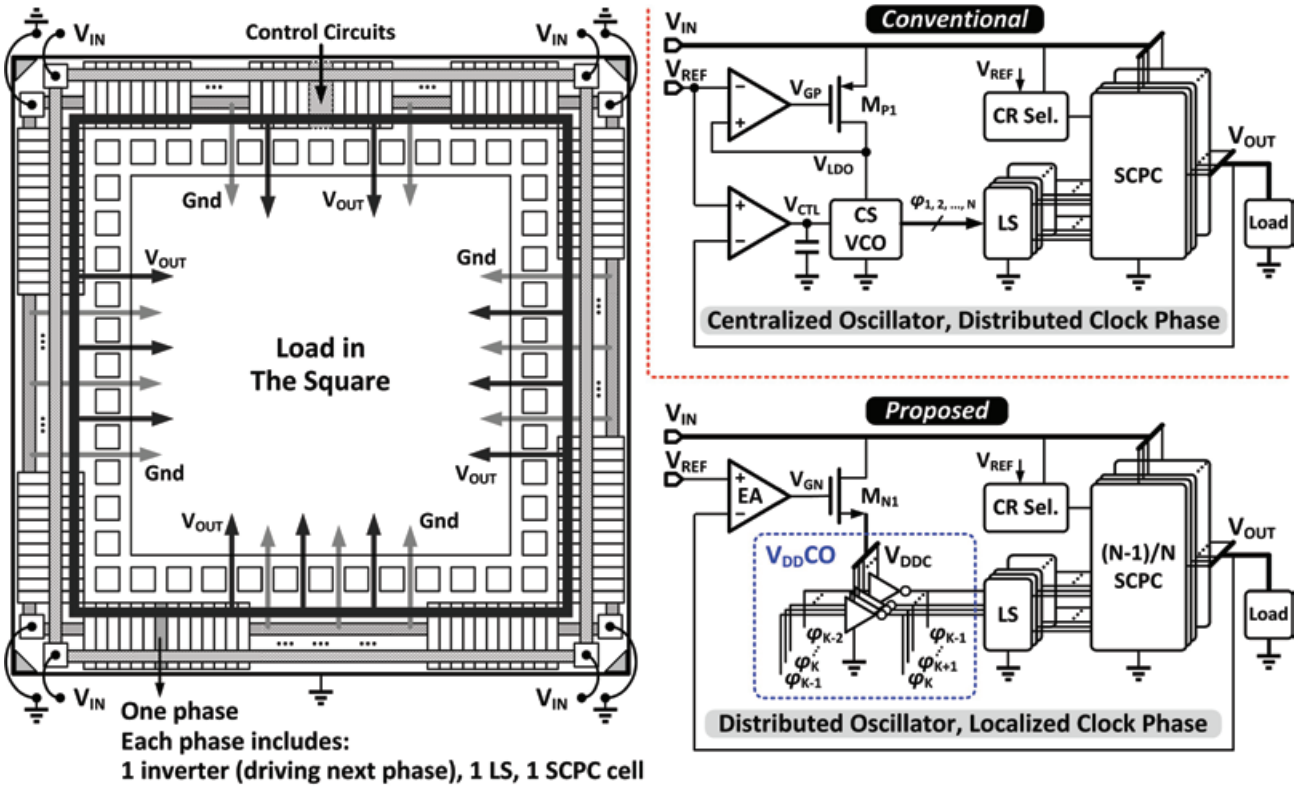


Fig. 1. Conceptual layout of the 100+ phases converter-ring for microprocessors; and the proposed system architecture with the V_{DD}CO and the (N-1)/N SCPC.

Publication(s):

[1] Y. Lu*, J. Jiang, W.-H. Ki, C. P. Yue, S.-W. Sin*, S.-P. U*, and R. Martins*, "A 123-phase DC-DC converter ring with fast-DVS for microprocessors," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2015, pp. 364–365.

[2] Y. Lu*, J. Jiang, and W. H. Ki, "A Multiphase Switched-Capacitor DC–DC Converter Ring With Fast Transient Response and Small Ripple," IEEE Journal of Solid-State Circuits, vol. 52, no. 2, pp. 579–591, Feb. 2017.

* Contributors with University of Macau

Sponsorship:

Research Grant Council of Hong Kong, Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Fully-Integrated Low-Dropout Regulator with Fast Transient Response and Full-Spectrum Power Supply Rejection

Yan Lu, Yipeng Wang, Quan Pan, Wing-Hung Ki, and C. Patrick Yue

FEATURES

Fully integrated voltage regulator
Full-spectrum power supply rejection
Fast transient response time, 1.15ns
Quiescent current, 50μA
43mV undershoot @ 0 to 10mA load step
Silicon Verified in TSMC 65nm CMOS

DESCRIPTION

A fully-integrated low-dropout regulator (LDO) with fast transient response and full spectrum power supply rejection (PSR) is proposed to provide a clean supply for noise-sensitive building blocks in wideband communication systems. With the proposed point-of-load LDO, chip-level high-frequency glitches are well attenuated, consequently the system performance is improved. A tri-loop LDO architecture is proposed and verified in a 65 nm CMOS process. In comparison to other fully-integrated designs, the output pole is set to be the dominant pole, and the internal poles are pushed to higher frequencies with only 50 μA of total quiescent current.

For a 1.2 V input voltage and 1 V output voltage, the measured undershoot and overshoot is only 43 mV and 82 mV, respectively, for load transient of 0 μA to 10 mA within edge times of 200 ps. It achieves a transient response time of 1.15 ns and the figure-of-merit (FOM) of 5.74 ps. PSR is measured to be better than -12 dB over the whole spectrum (DC to 20 GHz tested). The prototype chip measures 260 × 90 μm², including 140 pF of stacked on-chip capacitors.

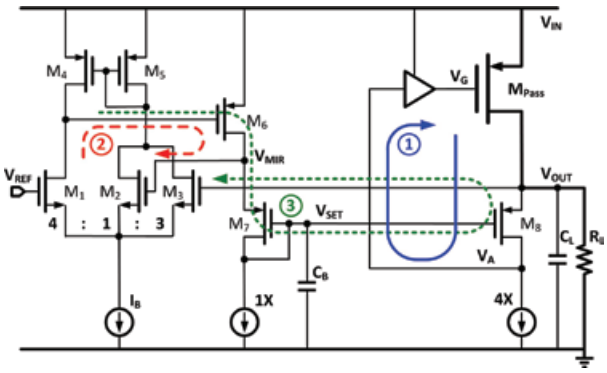


Fig. 1. Schematic of the proposed fully integrated tri-loop LDO.

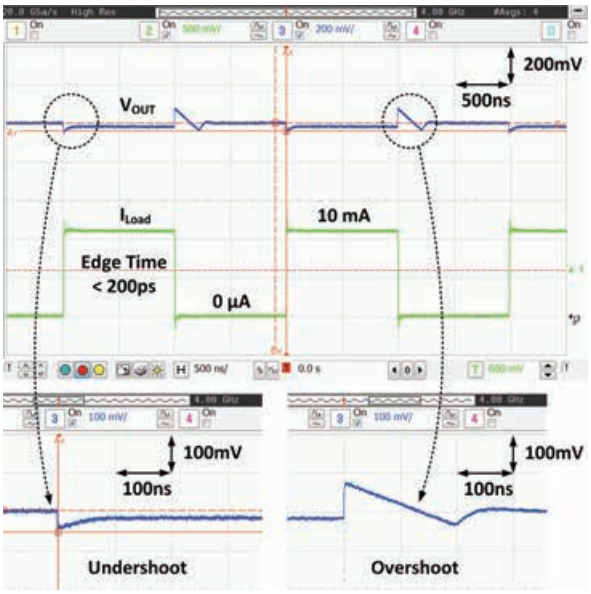


Fig. 2. Measured transient response with V_{IN} = 1.2 V, V_{OUT} = 1.0 V, and on-chip loading change from 0 μA to 10 mA within edge times of 200 ps.

Publication(s):

[1] Y. Lu*, Y. Wang, Q. Pan, W.-H. Ki, and C. P. Yue, "A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, pp. 707–716, Mar. 2015.

* Contributors with University of Macau

Sponsorship:

N/A

A Fully Integrated Digital LDO With Coarse–Fine-Tuning and Burst-Mode Operation

Mo Huang, Yan Lu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Fully integrated voltage regulator
Coarse-fine tuning and adaptive clock
55mV undershoot @ 2-to-100 mA load step
Quiescent current, 82μA
Silicon verified in ST 65nm CMOS process

DESCRIPTION

The digital low dropout regulator (D-LDO) has drawn significant attention recently for its low-voltage operation and process scalability. However, the tradeoff between current efficiency and transient response speed has limited its applications. In this work, a coarse–fine-tuning technique with burst-mode operation is proposed to the D-LDO. Once the voltage undershoot/overshoot is detected, the coarse tuning quickly finds out the coarse control word in which the load current should be located, with large power MOS strength and high sampling frequency for a fixed time.

Then, the fine-tuning, with reduced power MOS strength and sampling frequency, regulates the D-LDO to the desired output voltage and takes over the steady-state operation for high accuracy and current efficiency. The proposed D-LDO is verified in a 65-nm CMOS process with a 0.01-mm2 active area. The measured voltage undershoot and overshoot are 55 and 47 mV, respectively, with load steps of 2 to 100 mA with a 20-ns edge time. The quiescent current is 82 μA, with a 0.43-ps figure of merit achieved. Moreover, the reference tracking speed is 1.5 V/μs.

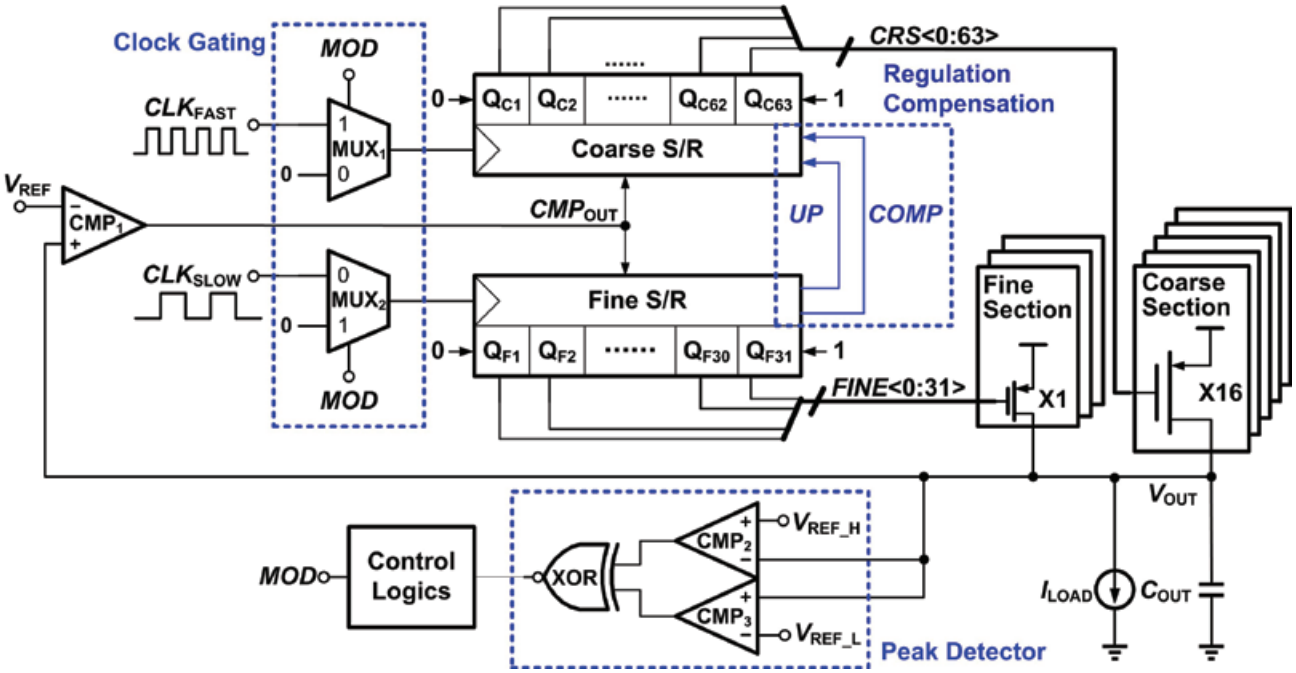


Fig. 1. Schematic of the proposed D-LDO.

Publication(s):

[1] M. Huang, Y. Lu, S. W. Sin, S. P. U, and R. P. Martins, "A Fully Integrated Digital LDO With Coarse–Fine-Tuning and Burst-Mode Operation," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 7, pp. 683–687, Jul. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators

Mo Huang, Yan Lu, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Wing-Hung Ki

FEATURES

Model analysis on the limit cycle oscillation (LCO)
Reduce the LCO mode of D-LDO to 1 with negligible area and power overhead
Simulated in ST 65nm CMOS

DESCRIPTION

The digital low-dropout regulator (D-LDO) has drawn significant attention recently for its low-voltage operation and process-scalability. However, the inherent quantization errors with this architecture will originate a steady-state limit cycle oscillation (LCO). As defined in literatures, the period of LCO is 2M times of the sampling period T_S, where M is the mode of LCO. In previous designs, LCO was reduced with a higher ADC resolution which increased circuit complexity, or using a dead-zone which sacrifices the output DC accuracy.

To address this issue, the modes and amplitudes of LCO are calculated in this work and verified by SPICE simulation in a 65-nm CMOS process. An LCO reduction technique for the D-LDO is then proposed, by adding two unit power transistors in parallel with the main power MOS array as a feedforward path, as shown in Fig. 1. This technique sets the LCO mode to 1 and effectively reduces the ripple amplitude for a wide (0.5–20 mA) load current range. When compared with the dead-zone scheme, this technique minimizes LCO with negligible circuit complexity and design difficulty.

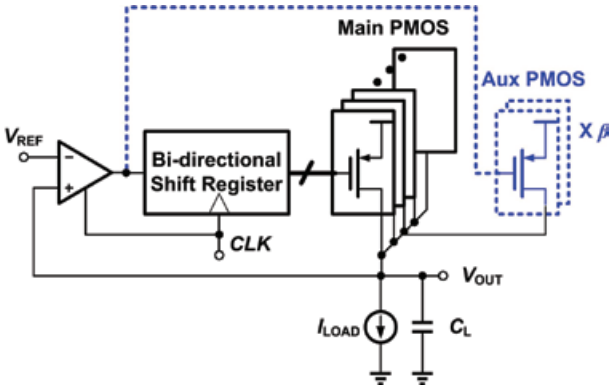


Fig. 1. Implementation of the modified D-LDO with LCO reduction.

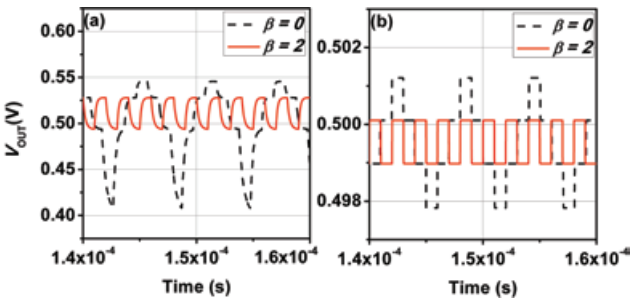


Fig. 2. Simulated results of the proposed D-LDO in β = 0 and 2 cases, with (a) 0.5- and (b) 20-mA load currents, at F_s = 1 MHz and V_{REF} = 0.5 V.

Publication(s):

1] M. Huang*, Y. Lu*, S. W. Sin*, S. P. U*, R. P. Martins*, and W. H. Ki, "Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 9, pp. 903–907, Sep. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

An NMOS-LDO Regulated Switched-Capacitor DC-DC Converter with Fast-Response Adaptive-Phase Digital Control

Yan Lu, Wing-Hung Ki, and C. Patrick Yue

FEATURES

Fully integrated voltage regulator
Cascaded switched-capacitor DC-DC with NMOS LDO
Adaptive-phase control for flatter efficiency curve
Peak DC-DC efficiency, 80.3%
Peak DC-DC + LDO efficiency, 76.2%
Output ripple, 2mV
Silicon Verified in TSMC 65nm CMOS

DESCRIPTION

A fully-integrated low-dropout regulated step-down multi-phase switched-capacitor DC-DC converter (a.k.a. charge pump, CP) with a fast-response adaptive-phase (Fast-RAP) digital controller is designed using a 65 nm CMOS process, as shown in Fig. 1 and Fig. 2.

Different from conventional designs, a low-dropout regulator (LDO) with an NMOS power stage is used without the need for an additional step-up charge pump for driving. A clock tripler and a pulse divider are proposed to enable the Fast-RAP control. As the Fast-RAP digital controller is designed to be able to respond faster than the cascaded linear regulator, transient response will not be affected by the adaptive scheme. Thus, light-load efficiency is improved without sacrificing the response time.

When the CP operates at 90 MHz with 80.3% CP efficiency, only small ripples would appear on the CP output with the 18-phase interleaving scheme, and be further attenuated at V_{OUT} by the 50-mV dropout regulator with only 4.1% efficiency overhead and 6.5% area overhead. The output ripple is less than 2 mV for a load current of 20 mA.

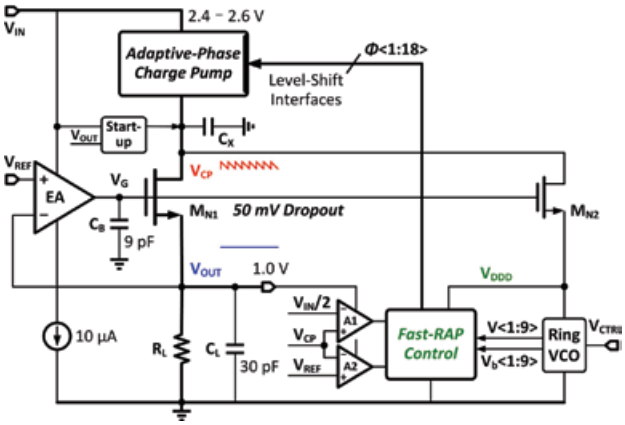


Fig. 1. Block diagram of the fully-integrated NMOS-LDO regulated switched-capacitor DC-DC converter with fast-response adaptive-phase (Fast-RAP) control.

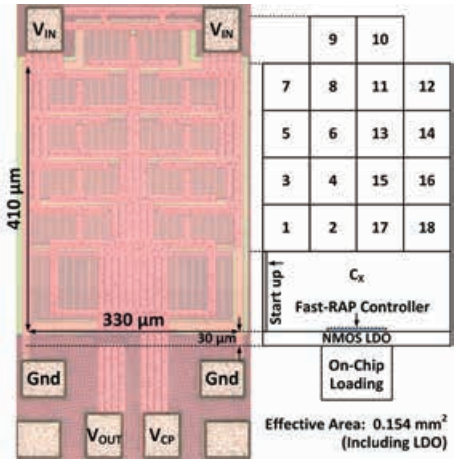


Fig. 2. Chip micrograph of the NMOS-LDO regulated charge pump.

Publication(s):

[1] Y. Lu*, W. Ki, and C. Patrick Yue, "An NMOS-LDO Regulated Switched-Capacitor DC–DC Converter With Fast-Response Adaptive-Phase Digital Control," IEEE Transactions on Power Electronics, vol. 31, no. 2, pp. 1294–1303, Feb. 2016.

* Contributors with University of Macau

Sponsorship:

N/A

A 312 ps Response-Time LDO with Enhanced Super Source Follower in 28 nm CMOS

Yan Lu, Cheng Li, Yan Zhu, Mo Huang, Seng-Pan U, and Rui P. Martins

FEATURES

Fully integrated voltage regulator
Enhanced super source follower
Fast transient response time, 312ps
Quiescent current, 100μA
26mV undershoot @ 0 to 10mA load step
Simulated in GF 28nm Bulk CMOS

DESCRIPTION

High quality fully integrated power supplies could notably improve the performances of the noise-sensitive building block in the ultra-wideband (UWB) communication systems.

The flipped-voltage-follower (FVF) based LDO is one of the most popular architectures, due to its simplicity and the potential for fast-transient-response. Since the FVF-based LDO is a single-ended topology, for a similar dynamic response, the FVF-based LDO only consumes 50% of the bias current compared a conventional LDO that using a differential error amplifier (EA). Although the FVF-based LDO also consists of an auxiliary differential EA, it is not in the main loop, and only serves as a bias voltage generator which consumes low current. Thus, the FVF-based LDO is more power-efficient

As shown in Fig. 1, double buffers are inserted into the cascode FVF topology to enable designing the dominant pole at the output node for better PSR and less voltage variation during load transient. An enhanced super source follower (E-SSF) is proposed in this work to further reduce the output impedance of the buffer that drives the power transistor. In the conventional SSF, only M_4 and M_6 are used, while in the proposed E-SSF, M_5 is inserted between M_4 and M_6, to provide an even lower output impedance.

The proposed idea is simulated in a 28 nm CMOS process, and consumes 100 μA quiescent current with 1.0 V input and 0.8 V output voltages. In total, 120 pF on-chip capacitors are used for filtering. The AC responses including the Bode plots and the PSR curves with the load current ranging from 0.1 to 10 mA are simulated. The loop UGF of the cascode FVF with the enhanced SSF is 1.28 GHz with 49° phase margin. Benefitting from the UHF bandwidth, full-spectrum PSR is achieved with the worst case of −18.9 dB happening at 1.55 GHz, while the low frequency PSR is around −27 dB. Meanwhile, a transient response time of 312 ps is achieved.

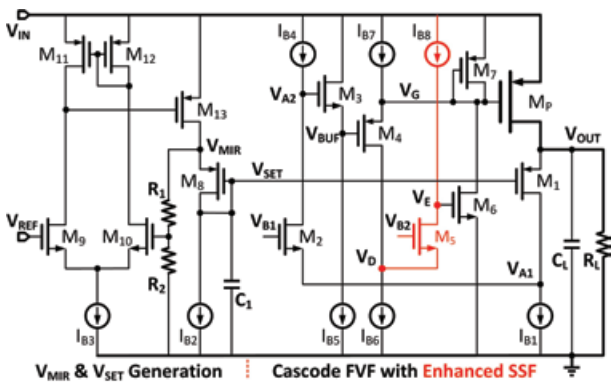


Fig. 1. Schematic of the proposed LDO with enhanced super source follower.

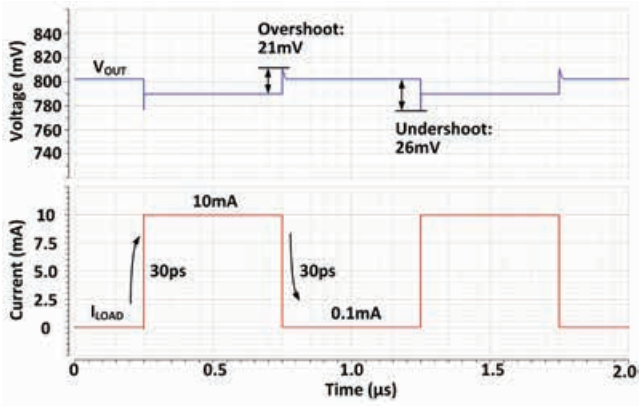


Fig. 2. Simulated load transient response of the LDO with 1.2 V input voltage and 1.0 V output voltage with voltage positioning.

Publication(s):

[1] Y. Lu, C. Li, Y. Zhu, M. Huang, S. P. U, and R. P. Martins, "A 312 ps response-time LDO with enhanced super source follower in 28 nm CMOS," Electronics Letters, vol. 52, no. 16, pp. 1368–1370, 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Self-Reconfiguration Property of A Mixed Signal Controller for Improving Power Quality Compensation during Light Loading

Man-Chung Wong, Yan-Zheng Yang, Chi-Seng Lam, Wai-Hei Choi, Ning-Yi Dai, Yajie Wu, Chi-Kong Wong, Sai-Weng Sin, U-Fat Chio, Seng-Pan U, and Rui P. Martins

FEATURES

Adaptive signal conditioning & programmability on-the-fly
Parallelism properties & higher redundancy
Higher accuracy, higher bandwidth, faster response time & low power
Algorithm complexity & simplicity of implementation

DESCRIPTION

When power quality compensator performance does not satisfy international standards, other PWMs can be selected, or the dc link voltage can be increased. However, it may be the case that neither of these methods will improve compensator performance during light loading due to the low resolution of the input signals compared with the error signal and the PWM error margin. The design of digital controllers is usually based on a full loading situation. The full analog-to-digital (A/D) conversion input signal range of a digital controller is therefore utilized, to avoid analog signal saturation. In a light load situation, the digital controller may suffer from the problem of low resolution, which significantly affects its compensation performance. There is presently no achievable control strategy to deal with power quality compensation issues during light loading.

A mixed signal controller for power quality compensator is proposed for enhancing the advanced performance that cannot be achieved by analog or digital controller alone and independently. The FPAA can be operated as an adaptive signal conditioning unit that pre-conditions and filters, according to the optimization of system performance. The modified signals then pass to the digital unit for further processing, assisted by the ADC. The digital system, FPGA/DSP, can work with a "backer" sub-program to optimize the system operation by reconfiguring the control system automatically, or to carry out self-testing and self-repairing tasks. When it is necessary to reconfigure the analog part, the re-programming data can be transferred directly through the digital path to the FPAA. Conversely, the FPAA can also send out control signals to the FPGA to modify the algorithm for protection, critical operations, etc.

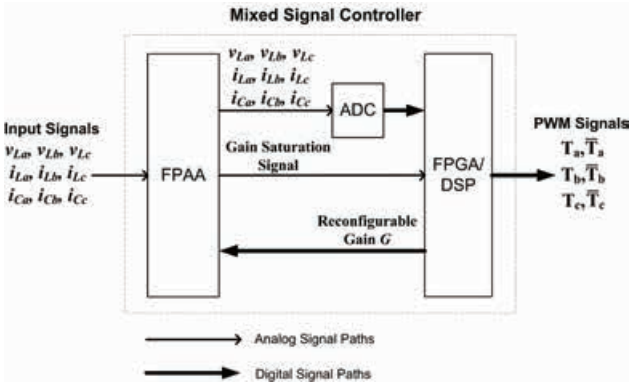


Fig. 1. Proposed mixed signal controller.

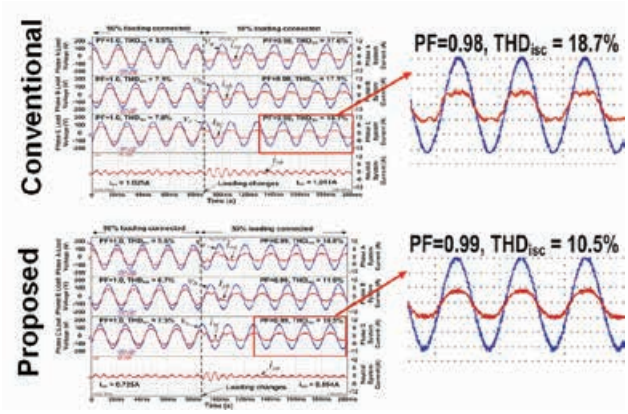


Fig. 2. Experimental compensation performance during loading changes by using conventional digital controller and proposed mixed signal controller.

Publication(s):

[1] M.-C. Wong, Y.-Z. Yang, C.-S. Lam, W.-H. Choi, N.-Y. Dai, Y.-j. Wu, C.-K. Wong, S.-W. Sin, U-F. Chio, S.-P. U, R.P. Martins, "Self-reconfiguration Property of A Mixed Signal Controller for Improving Power Quality Compensator during Light Loading," IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5938–5951, Oct. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

DCM Operation Analysis of KY Converter

Wen-Liang Zeng, Chi-Seng Lam, Wen-Ming Zheng, Sai-Weng Sin, Ning-Yi Dai, Man-Chung Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Deduce KY converter CCM/DCM operation boundary, DCM voltage gain & DCM small signal transfer function
Important for DCM closed-loop controller of KY converter IC design
MATLAB and 65 nm CMOS technology in Cadence confirm deduced DCM theory

DESCRIPTION

A KY converter has the characteristics of non-pulsating output current, low output voltage ripple and no right-half plane zero (RHPZ) in continuous conduction mode (CCM), which can overcome the drawbacks of the conventional boost and buck-boost converters. However, when the KY converter is implemented into an integrated circuit (IC), its discontinuous conduction mode (DCM) operation cannot be avoided due to a small inductor value.

The boundary for DCM operation region, DCM dc voltage and small signal transfer functions are proposed, which fill the gap of the DCM operation theory for the KY converter. Simulation results by using MATLAB and Cadence are provided to verify the deduced DCM operation theory of KY converter. Then, its DCM closed-loop controller design can be achievable in future.

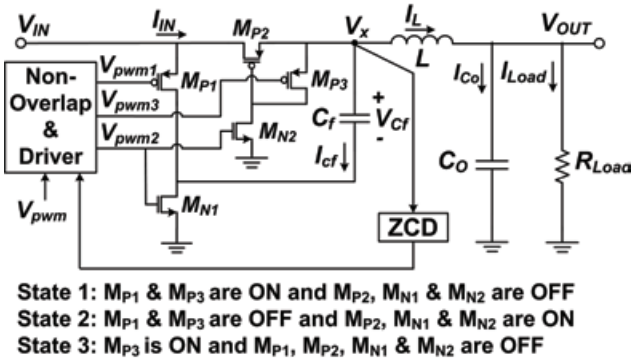


Fig. 1. Proposed KY converter IC topology for DCM.

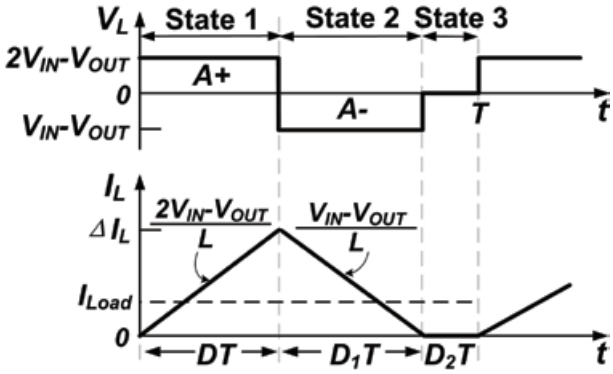


Fig. 2. KY converter idealized V_L and I_L waveforms for DCM.

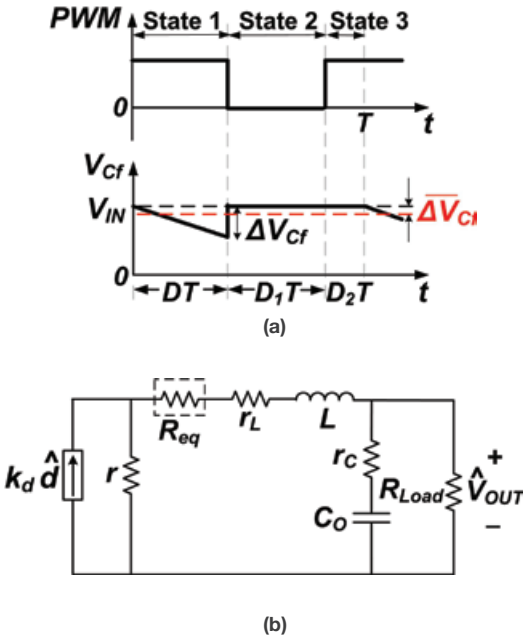


Fig. 3. Small signal model of KY converter for DCM: (a) Flying capacitor voltage V_{cf} deviation phenomenon and (b) Small signal model with V_{cf} deviation.

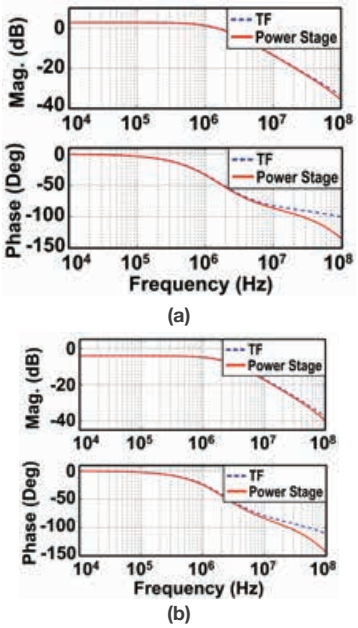


Fig. 4. KY converter open-loop bode plot for DCM: (a) When D=0.3 and (b) When D=0.5.

Publication(s):

[1] W.-L. Zeng, C.-S. Lam, W.-M. Zheng, S.-W. Sin, N.-Y. Dai, M.-C. Wong, S.-P. U, and R. P. Martins, "DCM Operation Analysis of KY Converter," IET Electron. Lett., vol. 51, no. 24, pp. 2037–2039, Nov. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

DCM Operation Analysis of 3-Level Boost Converters

Yi-Wei Tan, Chi-Seng Lam, Sai-Weng Sin, Man-Chung Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Deduce 3LB CCM/DCM operation boundary
DCM voltage gain & DCM small signal transfer function
Important for DCM closed-loop controller of
3LB converter IC design
MATLAB and 65 nm CMOS technology in Cadence
confirm deduced DCM theory

DESCRIPTION

The 3-level boost (3LB) converters have the characteristics of higher voltage conversion ratio and efficiency, lower inductor current ripples, output voltage ripples and voltage stresses on switches when compared with the conventional boost converters in continuous conduction mode (CCM). When implemented into an integrated circuit (IC) we cannot avoid the 3LB converter discontinuous conduction mode (DCM) operation due to a smaller inductance.

In this work, we deduce its DCM operation analysis, including CCM/DCM boundary, DCM voltage gain and DCM small signal transfer function, which are surprisingly different from the boost converter as they have the same CCM ones. We verify the deduced DCM operation theory using MATLAB and Cadence, to obtain a feasible DCM closed-loop controller design in future.

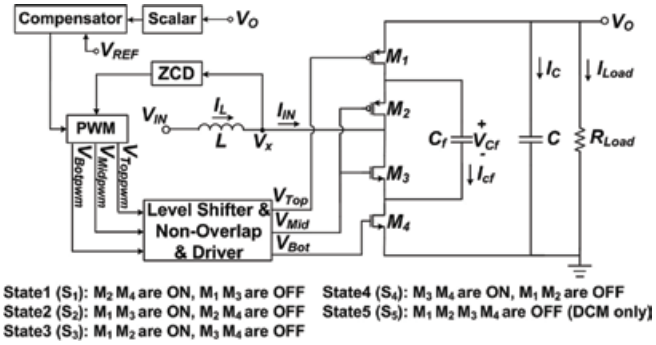
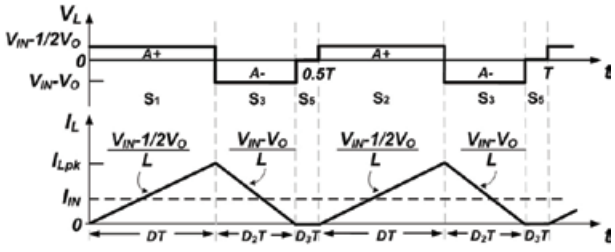
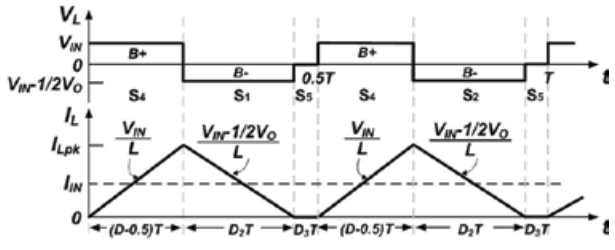


Fig. 1. Proposed 3LB converter IC topology for DCM.

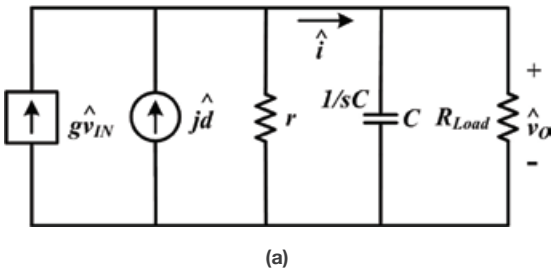


(a)

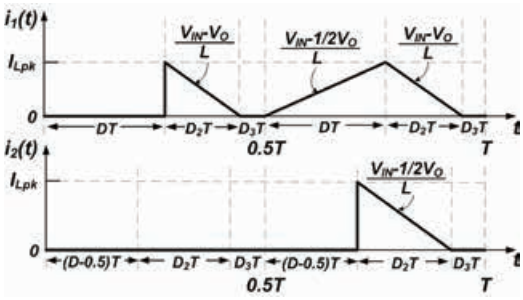


(b)

Fig. 2. 3LB converter idealized V_L and I_L waveforms for DCM: (a) when 0<D<0.5 and (b) when 0.5<D<1.

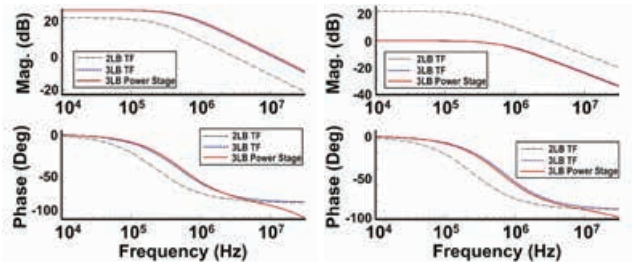


(a)



(b)

Fig. 3. Output side small signal model of the 3LB converter for DCM: (a) Output side of the 3LB converter DCM small signal model and (b) Output side current waveforms, $i_1(t)$: 0<D<0.5, $i_2(t)$: 0.5<D<1.



(a) (b)

Fig. 4. Boost converter and 3LB converter open-loop bode plot for DCM: (a) When D=0.3 and (b) When D=0.7.

Publication(s):

[1] Y.-W. Tan, C.-S. Lam, S.-W. Sin, M.-C. Wong, S.-P. U, and R. P. Martins, "DCM Operation Analysis of 3-level Boost Converters," IET Electron. Lett., vol. 53, no. 4, pp. 270–272, Feb. 2017.

Sponsorship:

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