RESEARCH ABSTRACTS
ENERGY HARVESTING AND SENSING CIRCUITS

A 12 pJ/pixel Analog-to-Information Converter based 816 x 640 Pixel CMOS Image Sensor

Denis Guangyin Chen, Fang Tang, Man-Kay Law, and Amine Bermak

FEATURES

Aanlog-to-Information conversion (AIC)
Pixel-level compression with bit-image processor
Area-efficient SAR-SS hybrid ADC
High energy efficiency, 12 pJ/pixel·frame
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

To achieve improved energy efficiency for image sensors, the most aggressive approach is to integrate image compression at or before the point of quantization. In this work, a column-parallel AIC based on visual pattern image coding (VPIC) is proposed. When compared with other algorithm classes, VPIC has the advantage of not requiring any matrix operations. The proposed AIC circuit is prototyped in a high-resolution image sensor. The charge-transfer-amplifier (CTA) integrates a charge-pump bit-image processor (BIP) with a successive approximation-register-single-slope (SAR-SS) hybrid ADC. The SAR-SS ADC's capacitor array is exploited to provide additional functionalities both as a load for the CTA and as a computational device to perform parts of the compression algorithm.

The basic algorithm is illustrated in Fig. 1(a). The mean u and gradient G is calculated for a 4x4 pixel block, and the bit-image B is quantized by comparing each pixel to u. If G is less than a threshold, then the pixel block is a uniform pattern (UP), otherwise, it is an edge pattern (EP). The entire column circuit is depicted in Fig. 1(b). A charge-transfer amplifier (CTA) is used to implement correlated double sampling (CDS). The chip prototype is fabricated in 0.18-μm CMOS, as shown in Fig. 1(c). Fig. 1(e) and (f) shows the captured image using the chip prototype in compression and raw mode respectively. This work achieves an energy consumption of 12 pJ/pixel, which is the most energy efficient CMOS image sensor to date.

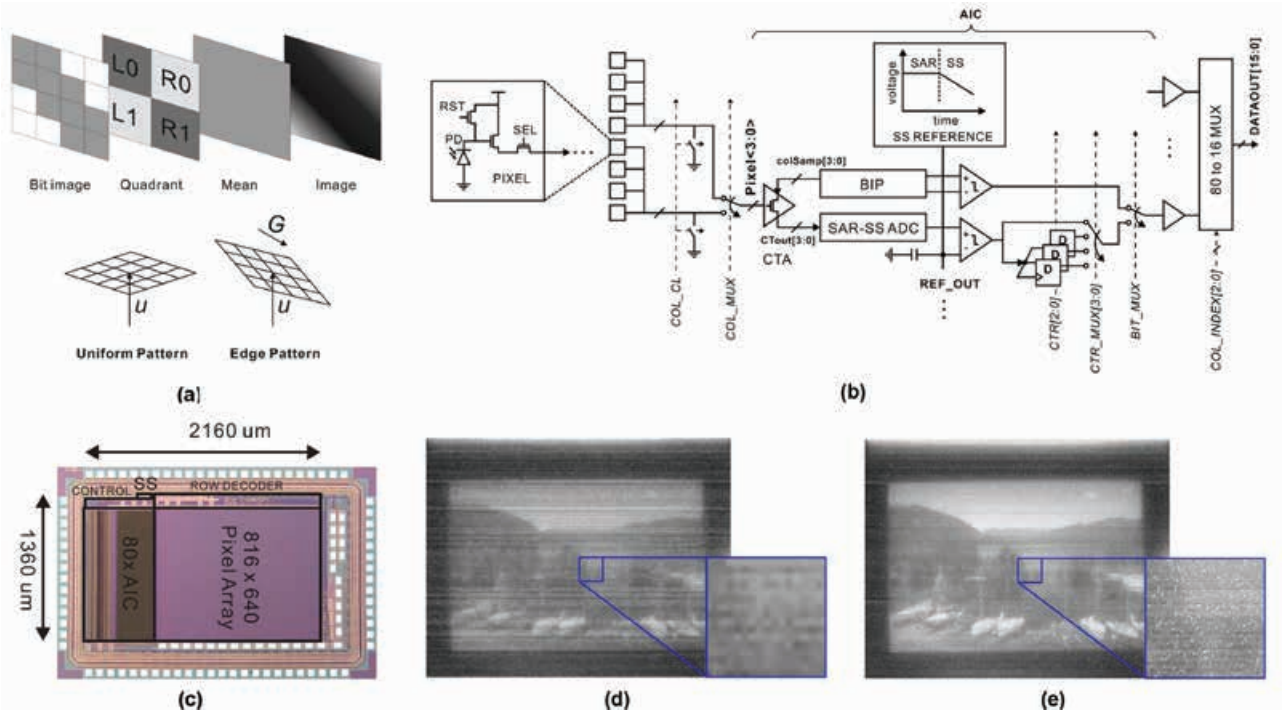

Fig. 1. (a) Components used in the image compression algorithm. (b) Column circuit: from pixel to AIC. (c) Chip micrograph. (d) Image captured from the chip prototype in compression mode. (e) Image captured in raw mode.

Publication(s):

[1] D. G. Chen, F. Tang, M.-K. Law* and A. Bermak, "A 12 pJ/pixel Analog-to-Information Converter based 816 x 640 Pixel CMOS Image Sensor," IEEE J. Solid-State Circuits, vol. 49, no. 5, pp. 1210-1222, May 2014.

* Contributors with University of Macau

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A 64 fJ/step 9-bit SAR ADC Array With Forward Error Correction and Mixed-Signal CDS for CMOS Image Sensors

Denis Guangyin Chen, Fang Tang, Man-Kay Law, Xiaopeng Zhong, and Amine Bermak

FEATURES

Pilot-Digital-to-Analog Converter (pDAC)
Forward error correction
Mixed-signal correlated-double-sampling
Figure-of-Merit of 64 fJ/step
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

The main challenge of column parallel SAR ADCs for image sensors lies in achieving adequate resolution in a very small capacitor array. The pDAC described introduces input independent Forward-Error-Correction (FEC), mixed-signal CDS, parasitic effect reduction, and energy efficient dynamic comparators.

The basic pDAC operation is illustrated in Fig. 1. The input signal is sampled onto the top-plate of the capacitor array during sampling. During MSB phase, the pDAC array is one quarter of the size of the MSB array with the exception of C_{92}. Once the 4 MSBs are determined, the rest of the MSB and LSB capacitors are connected on the fifth clock without any trial-and-error. In FEC phase, the missing code issue is addressed by introducing a redundant bit-trial. During the error correction clock, C_{N-k} is restored to GND, this creates a negative perturbation on V_{DAC}. Both positive and negative errors from earlier bit-trials can be recovered by the C_{N2} weight (C_{92} in this case) under the accuracy of the full-sized capacitor array. In LSB phase, the 5 LSBs in the SAR ADC are obtained using the conventional switching sequence.

The chip prototype is fabricated in a standard 0.18-µm CMOS process. As shown in Fig. 2, the large DNL error due to missing codes at 125th and 350th code entry in the conventional DAC is resolved by the reported FEC algorithm. The INL, on the other hand, is limited by the accuracy of the full capacitor-array. The work achieves one of the smallest and most energy efficient designs with the best FoM among ADCs found in state-of-the-art image sensors.

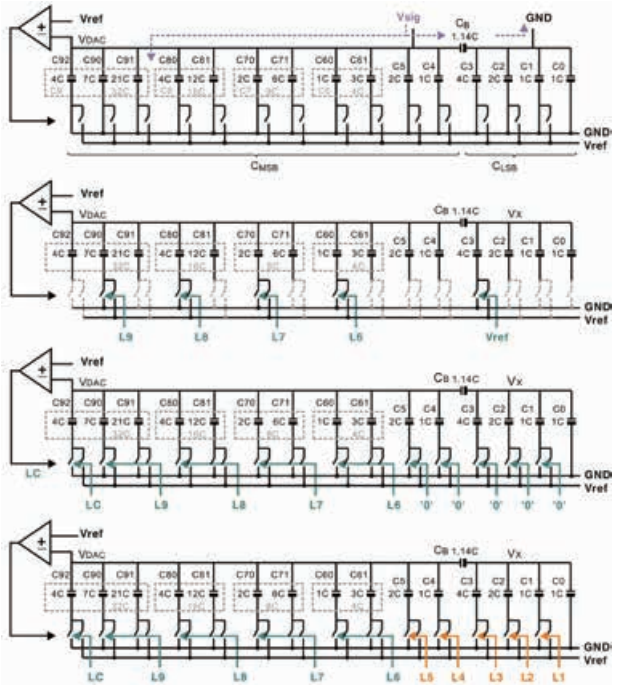

Fig. 1. (a) sampling; (b) MSB; (c) FEC; and (d)LSB.

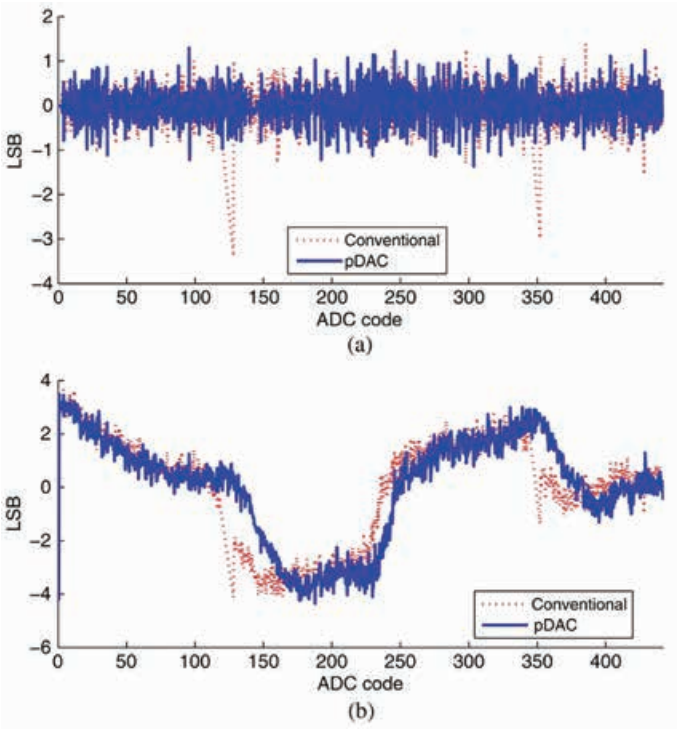

Fig. 2. (a) DNL and (b) INL of the 9 b SAR ADC.

Publication(s):

[1] D. G. Chen, F. Tang, M.-K. Law*, X. Zhong and A. Bermak, "A 64-fJ/step 9-bit SAR ADC Array with Forward Error Correction and mixed-signal CDS for CMOS Image Sensors," IEEE Trans. Circuits Syst.-I: Reg Papers, vol. 61, no. 11, pp. 3085-3093, Nov. 2014.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Passive RFID Tag Embedded Temperature Sensor With Improved Process Spreads Immunity for a -30°C to 60°C Sensing Range

Bo Wang, Man-Kay Law, Amine Bermak, and Howard C. Luong

FEATURES

Embedded CMOS temperature sensor in passive RFID tag system
Improved PVT spread immunity
High accuracy, ±0.15 °C (3σ) from -30 to 60 °C
Low power, 0.35 µA at 1-V supply
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

Embedding the temperature sensing function into passive RFID tag brings new challenges in terms of system design. Firstly, the embedded sensor should be ultra-low power (in the order of sub-µW) to prevent loss in the RFID tag's sensitivity; Secondly, the occupied sensor area and its calibration effort should be minimized to maintain low cost. Thirdly, for passive tags, as the sensor is supplied by the on-chip power management unit (PMU) and a good supply rejection is necessary to achieve accurate sensing.

This work targets at a -30 to 60 °C for cold chain food monitoring, medicines and health commodities storage range, as well as the general environment monitoring. A resistor, capacitor and on-chip clock frequency PVT variations compensation technique is embodied in a time-domain readout to improve the process spreads immunity. Fig. 1 shows the simplified circuit implementation of the embedded temperature sensor readout. It consists of three capacitor, C_{ref}, C_{pt} and C_{ct}, two comparator branches A_1 and A_2, and other digital blocks. Once the sensor is enabled by sen_EN, $M_{2\text{-}4}$ are turned on to steer the current signals from the sensor frontend. With all the capacitors initially reset, $I_{pt}(T)$ and $I_{ct}(T)$ charges C_{pt} and C_{ct}, respectively, while I_{ref} charges C_{ref}. At the end of integration, a temperature dependent pulse-width $t_{PW}(T)$ is generated, which is then digitized with a ripple counter. The calling edge of $t_{PW}(T)$ indicates the end of one sensing cycle.

Fig. 2 shows the chip prototype fabricated in a standard 180nm bulk CMOS process, with the temperature sensor is embedded in a passive RFID tag. Measurement results show that a sensing error of ±1.5 °C (3σ) is achieved from -30 to 60 °C. Our work achieves a good tradeoff among robustness, sensing power and sensing accuracy in the passive RFID platform. Moreover, this work requires only one-point calibration for its process immunity, which ensures the sensing tag to be low cost.

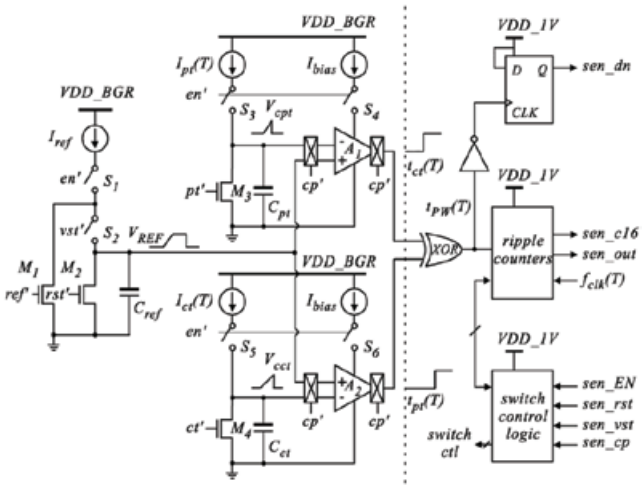

Fig. 1. Implementation of the proposed temperature sensor core.

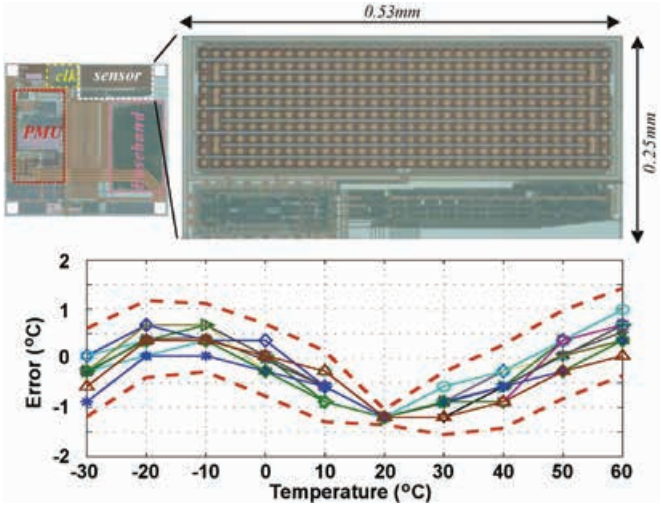

Fig. 2. Chip prototype in a RFID tag system (top) and measured inaccuracy of 12 sensor tag samples.

Publication(s):

[1] B. Wang, M.-K. Law*, A. Bermak and H. C. Luong, "A Passive RFID Tag Embedded Temperature Sensor With Improved Process Spreads Immunity for a -30 to 60 Sensing Range", IEEE Trans. Circuits Syst.-I: Reg. Papers, vol. 61, no. 2, pp. 337 – 346, Feb. 2014.

* Contributors with University of Macau

Sponsorship:

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Low-power CMOS Laser Doppler Imaging using Non-CDS Pixel Readout and 13.6-bit SAR ADC

Denis Guangyin Chen, Man-Kay Law, Yong Lian, and Amine Bermak

FEATURES

Fully customized laser doppler imager (LDI)
Non-CDS pixel readout scheme
Column 13.6b SAR ADC
State of the art Figure-of-Merit, 23 fJ/state
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

The laser Doppler (LD) effect describes the difference in frequency–the Doppler Shift–between the incident light and its scattered parts from moving particles. This work aims to provide a circuit-level analysis on how LDI imposes a distinctively different set of noise requirements compared to general purpose imaging. Quantitative conclusions will be drawn on how ADC resolution and correlated-double-sampling (CDS) can impact on LDI instrumentation precision. A compact body-biased PMOS reset pixel is proposed for reducing reset-noise without CDS. A compact time-domain noise-averaging comparator is also developed to satisfy the ADC resolution requirements of LDI while enjoying the energy efficiency of the SAR architecture.

The CMOS LDI sensor depicted in Fig. 1(a) is composed of a 128x128 pixel array and 13 column parallel high-resolution SAR ADCs. Each ADC is shared between 16 neighboring pixel columns via transfer-gate multiplexers. The output of the source follower is sampled by the 16b SAR ADC which generates 19 bits of datafor each sample.

The schematic of the 16b SAR ADC is shown in Fig. 1(b). Its sub-radix-2 digital-to-analog converter (DAC) with 19 weights is split into 3 sections. The unit capacitor is a 28 fF MIM capacitor. During the sampling phase, the bottom-plates of all capacitors in the negative DAC, DAC_n, except for the MSB capacitor is connected to while their top-plates sample the input signal, V_{sig}. Meanwhile, the top-plates of all capacitors in the positive DAC, DAC_p, except for the MSB capacitor is connected to GND while their bottom-plates sample V_{sig}. As a result, the DC bias of the comparator input is determined by K, simplifying the comparator design. V_{sig} can also have an inherent 2x voltage gain through the sampling process. The chip micrograph is shown in Fig. 1(c). It is measured using phantom serum with results matching the expected theoretical values. It has the lowest FoM amonst published works making it suitable for future mobile LDI applications.

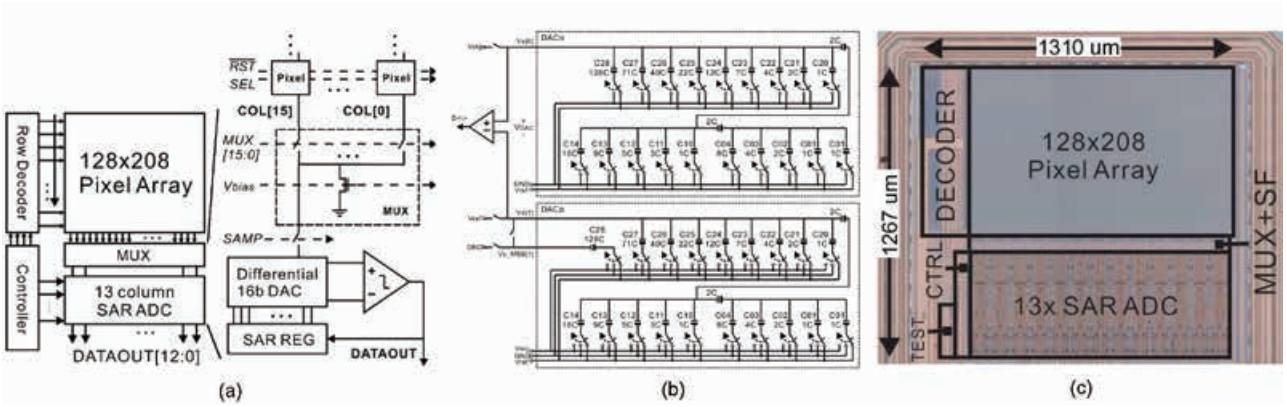

Fig. 1. (a) Block diagram of the LDI sensor chip and its column circuit from pixel to source follower to SAR ADC. (b) Schematic of the sub-radix-2 16b SAR ADC. (c) Prototype LDI sensor.

Publication(s):

[1] D. G. Chen, M.-K. Law*, Y. Lian and A. Bermak, "Low-power CMOS Laser Doppler Imaging using Non-CDS Pixel Readout and 13.6-bit SAR ADC," IEEE Trans. Biomed. Circuits Syst., vol. 10, no. 1, pp. 186-199, Feb. 2016.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong Research Grant Council

A 1.1 µW CMOS Smart Temperature Sensor with an Inaccuracy of ±0.2°C (3σ) for Clinical Temperature Monitoring

Man-Kay Law, Sanfeng Lu, Tao Wu, Amine Bermak, Pui-In Mak, and Rui P. Martins

FEATURES

Multi-ratio pre-gain stage
Block-based data weighted averaging (BDWA)
High accuracy, ±0.2°C(3σ) from 25 to 45 °C
Area-efficient SAR-SS hybrid ADC
Ultra-low power consumption
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

In this work, a CMOS temperature sensor is designed with high accuracy and ultra-low power consumption especially suitable for passively-powered clinical temperature monitoring applications where the human body temperature can be readily measured non-invasively. A multi-ratio pre-gain stage is proposed to relax the resolution requirement of the I-ADC by optimizing its input range utilization. BDWA is also proposed to alleviate the capacitor mismatch error while effectively relaxing the control overhead.

Fig. 1 (a,b) shows the block diagram of the conventional and proposed smart temperature sensor. We propose to integrate a multi-ratio pre-gain stage (k_{1-4}) to amplify the temperature signal while providing an offset to prevent integrator saturation under low voltage operation. This also relaxes the I-ADC requirement as only a moderate resolution is required (e.g. 12-bit for 0.1°C). The output bit-stream bs is then fedback for pre-gain update as well as processed by the off-chip digital filter to obtain the ratiometric output µ'.

BDWA is proposed to achieve multi-ratios with high accuracy while significantly reducing the routing cost. The key idea is to group a maximum number of unit capacitors into blocks while still providing the flexibility offered by the DWA. In this work, the number of control lines required is significantly reduced to 24, which is 4.8x less than that required for the conventional DWA.

This proposed smart temperature sensor is implemented in a standard 0.18µm CMOS process, occupying an active area of 0.198 mm². The sensor dissipates a measured power of 1.1 µW at 37°C with a conversion rate of 2 Sa/s. Measurement results show that an inaccuracy of ±0.1 °C (3 σ) is obtained from 37°C to 39°C (±0.2°C from 25°C to 45°C), demonstrating its suitability in human body temperature monitoring applications.

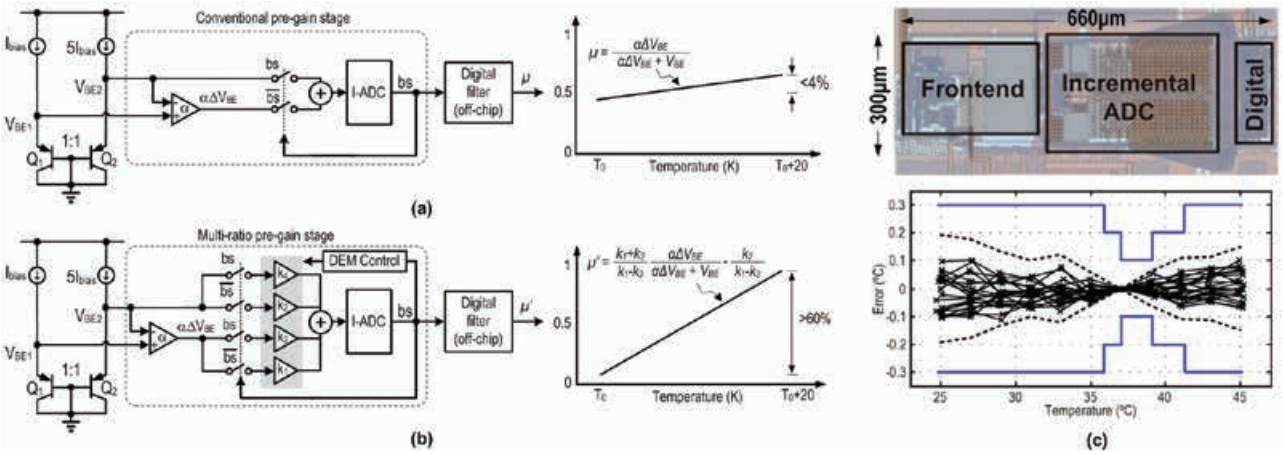

Fig. 1. (a) Block diagram of the conventional gain stage. (b) Block diagram of the proposed multi-ratio pre-gain stage. (c) Chip micro-graph (top) and measured inaccuracy from 20 chips samples after one-point calibration at 37°C, with bold dashed lines indicating the ±3σ values and blue solid lines showing the accuracy requirement.

Publication(s):

[1] M.-K. Law, S. Lu, T. Wu, A. Bermak, P.-I. Mak, and R. P. Martins, "A 1.1 µW CMOS Smart Temperature Sensor with an Inaccuracy of ±0.2oC (3σ) for Clinical Temperature Monitoring," IEEE Sensors J., vol. 16, no. 8, pp. 2272-2281, Feb. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Adaptive On/Off Delay-Compensated Active Rectifiers for Wireless Power Transfer Systems

Lin Cheng, Wing-Hung Ki, Yan Lu, and Tak-Sang Yim

FEATURES

Adaptive loops for reverse current control
ISM band frequency, 13.56MHz
Peak output power, 64.8mW
Peak efficiency, 91.4%
Silicon verified in AMS 0.35μm CMOS process

DESCRIPTION

An adaptive on/off delay-compensation technique is proposed to improve the performance of CMOS active rectifiers for wireless power transfer (WPT) systems. The effects of the on/off delays on the performance of the active rectifiers with either a parallel-resonant or a series-resonant circuit at the secondary coil are studied, which include power conversion efficiency (PCE), voltage conversion ratio (VCR) and output voltage ripple. By adding two feedback loops to the active diodes to generate the switched-offset currents for the comparators adaptively, both on- and off-delays are compensated for accurately against PVT variations and mismatches.

As a design example, a fully integrated active rectifier for biomedical applications with a parallel-resonant secondary was fabricated in a standard 0.35 μm CMOS process. With an AC input that ranges from 1.8 to 3.6 V, the measured VCR is higher than 90% and the measured PCE is higher than 89.1% for a load resistor of 500 Ω. In particular, the PCE is increased by 9% compared to the active rectifier without using the proposed technique.

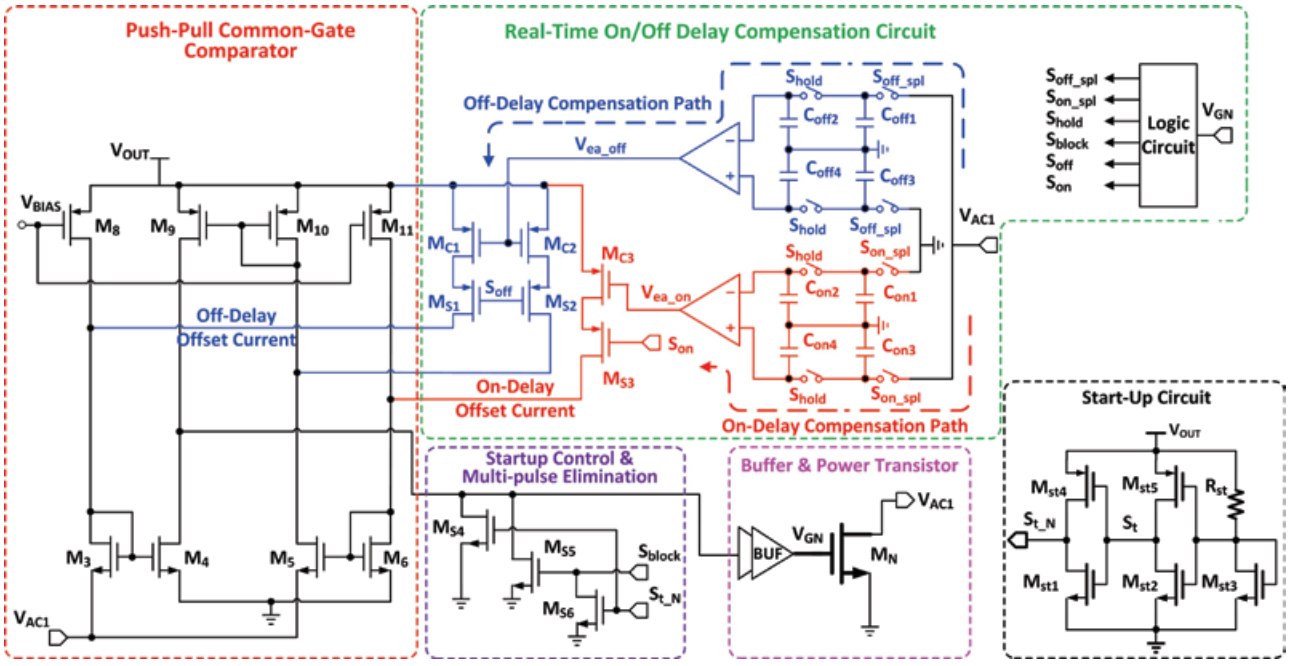

Fig. 1. Schematic of the active diode with the proposed adaptive on/off delay-compensation technique.

Publication(s):

[1] L. Cheng, W. H. Ki, Y. Lu*, and T. S. Yim, "Adaptive On/Off Delay-Compensated Active Rectifiers for Wireless Power Transfer Systems," IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 712–723, Mar. 2016.

* Contributors with University of Macau

Sponsorship:

N/A

A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes with a 67% Charge Pump Maximum Efficiency

Zhiyuan Chen, Man-Kay Law, Pui-In Mak, and Rui P. Martins

FEATURES

Solar energy harvesting IC with on-chip solar cell
Photodiode-assisted dual startup circuit (PDSC)
Auxiliary charge pump
Charge pump and solar cell area optimization
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

Solar energy harvesting has been recently demonstrated as a viable solution in applications including intraocular pressure monitoring and subdermal implant applications. Yet, the feasibility and co-optimization of a single-chip solar energy harvesting solution, that can boost the harvested voltage while achieving a high efficiency suitable for implantable applications, is yet to be demonstrated. We propose a single-chip solar energy harvesting system using a 3-stage integrated charge pump with on-chip photodiodes. An output power in the μW level is targeted for subdermal implant applications, where the key challenge is to achieve high energy efficiency at ultra-low power levels and in a small volume.

Fig. 1 shows the application scenario of a typical subdermal implant. This work focuses on the power management unit. The solar cell harvests the incoming solar energy and provides power to the other building blocks as well as to the load. To prevent noise coupling between modules, the solar cell is divided into three sub-blocks D_M, D_P and D_R to provide energy to the main/auxiliary charge pump, clock phase generator and voltage reference, respectively. The voltage reference generates a reference voltage V_{ref} for biasing the clock phase generator. PDSC is proposed to improve the voltage reference startup time while imposing minimum overhead. The clock phase generator provides a two-phase non-overlapping clock to the AQP and LCs using a 5-stage ring oscillator with body-biasing. An AQP is utilized to generate an auxiliary supply voltage V_{aux} to LC1 to ensure a low startup voltage while minimizing the reversion loss. High swing clock phases are utilized for improved conduction loss in the main charge pump.

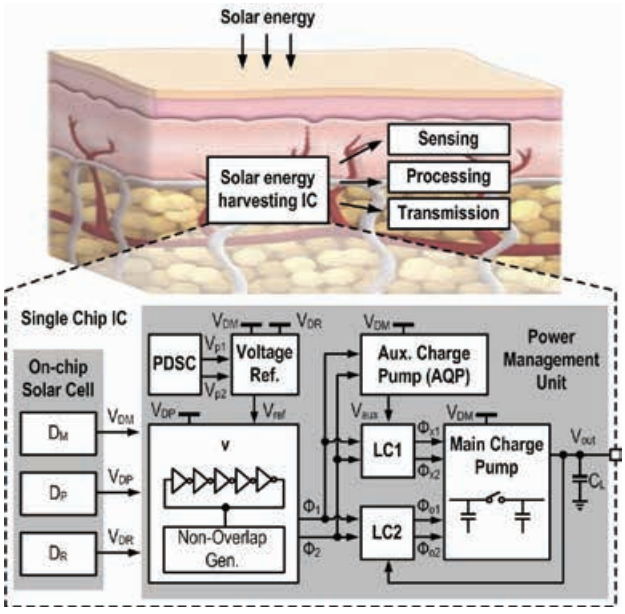

Fig. 1. Overview of the proposed single chip solar energy harvesting system.

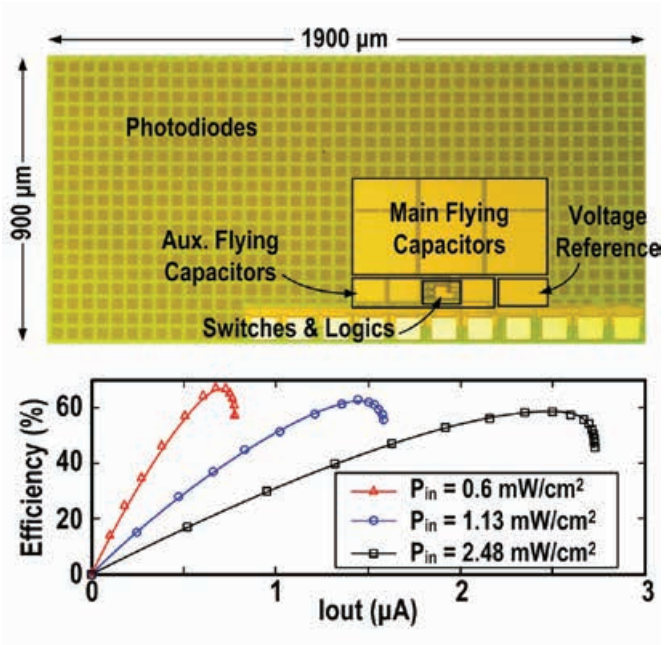

Fig. 2. Chip micrograph (top) and measured efficiency under different incident power levels (bottom).

Publication(s):

[1] Z. Chen, M.-K. Law, P.-I. Mak, and R. P. Martins, "A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes with a 67% Charge Pump Maximum Efficiency," IEEE Trans. Biomed. Circuits Syst., vol. 11, no. 1, pp. 44-53, Feb. 2017.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Reconfigurable Bidirectional Wireless Power Transceiver

Mo Huang, Yan Lu, Seng-Pan U, and Rui P. Martins

FEATURES

Reconfigurable without additional hardware
Maximum current charging mode
ISM frequency band, 6.78MHz
Battery-to-battery efficiency, 58.6%
Maximum charging power, 1.65W
Silicon verified in AMS 0.35μm 5V CMOS

DESCRIPTION

Wireless power transfer (WPT) is currently on the critical point of an explosive growth. Here, as projected in Fig. 1, we propose a future WPT eco-system of consumer electronics, which includes three layers: 1) wireless charging pads being the fundamental energy plants that can charge a wireless power bank and mobile devices; 2) wireless power banks that get energy from plants and feed mobile devices; 3) power hungry mobile devices that get energy from all the other sources.

Since the power transistors occupy a large silicon area, and the differential Class-D power amplifier (PA) and the full-wave (FW) active rectifier have very similar symmetrical architectures, to enable the mobile devices charging others without additional hardware, we propose a reconfigurable bidirectional 6.78 MHz WPT transceiver (TRX) that reuses the LC resonant tank and 4 area consuming power transistors for the differential Class-D PA and the full-wave rectifier. With such WPTTRX embedded, one can provide a first-aid to his/her smart watch or friend's device of which the battery is dying.

Fig. 2 shows the chip microphotograph and the measurement setup. The system was measured with two identical chips and two identical coils.

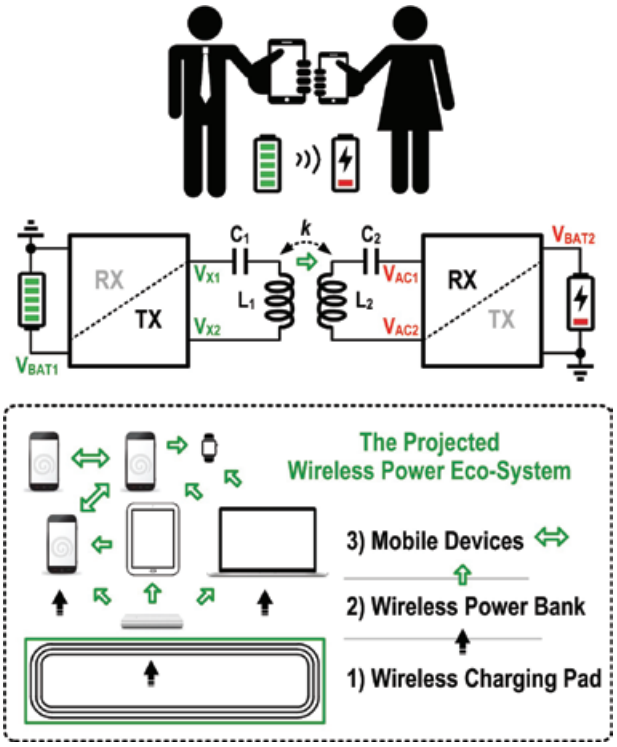

Fig. 1. The projected wireless power eco-system with mobile devices charging each other, enabled by the proposed reconfigurable bi-directional WPTTRX.

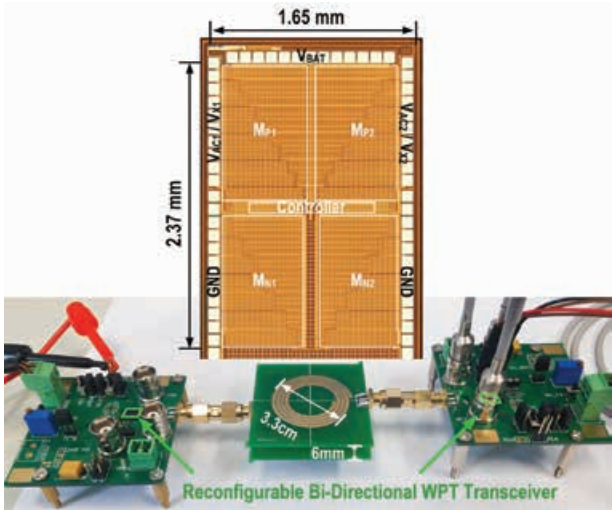

Fig. 2. Die micrograph and measurement setup of the reconfigurable bi-directional WPTTRX.

Publication(s):

[1] M. Huang, Y. Lu, S. P. U, and R. P. Martins, "A reconfigurable bidirectional wireless power transceiver with maximum-current charging mode and 58.6% battery-to-battery efficiency," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2017, pp. 376–377.

Sponsorship:

Research Committee of University of Macau, Macau Science and Technology Development Fund (FDCT)

A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting

Yan Lu, Haojuan Dai, Mo Huang, Man-Kay Law, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Dual-path RF energy harvesting
Wide input range, -16dBm to -5dBm
Silicon Verified in ST 65nm CMOS

DESCRIPTION

Energy harvesting has become increasingly important for a wide range of applications, including the wearable electronic devices, radio frequency identification (RFID), internet-of-things (IoT) and biomedical implanted devices. This work presents a dual-path CMOS rectifier with adaptive control for ultra-high frequency (UHF) RF energy harvesters. The input power range with high power convention efficiency (high-PCE) of the rectifier is extended by the proposed architecture which includes a low-power path and a high-power path.

The block diagram of the proposed rectifier is shown in Fig. 1. The dual-path rectifier consists of a low power path using LVTGP transistors for high-PCE at low input power and also for better input sensitivity, a high power path using LVTLP transistors designed for high-PCE at high input power, a reference path that generates a threshold voltage for the automatic path selection, and 3 switches S_1 through S_3 to enable/disable the low power path. Thus, the system can automatically choose the appropriate path according to the input power level to achieve a wider high-PCE range.

The dual-path rectifier with an adaptive control circuit is fabricated in a 65 nm CMOS process. Fig. 2 shows the chip micrograph of the proposed rectifier. The effective area excluding the pads is 250 × 190 μm². Operating at 900 MHz and driving a 147 kΩ load resistor, the measured PCE of this work can be maintained above 20% with an 11-dB input range from −16 dBm to −5 dBm, while only an 8 dB input range can be achieved with traditional single-path rectifiers. A sensitivity of −17.7 dBm is measured with 1 V output voltage across a capacitive load.

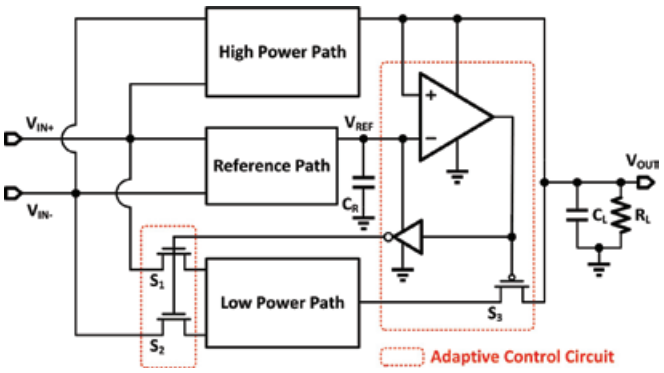

Fig. 1. System architecture of the dual-path rectifier.

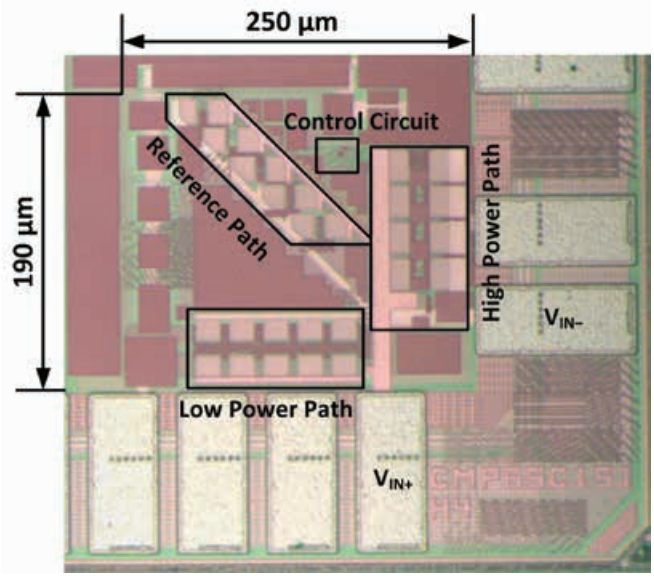

Fig. 2. Chip micrograph of the proposed dual-path rectifier.

Publication(s):

[1] Y. Lu et al., "A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 2, pp. 166-170, Feb. 2017.

Sponsorship:

Research Committee of University of Macau, Macau Science and Technology Development Fund (FDCT)

A Dual-Output Wireless Power Transfer System with Merged Active Rectifier and Three-Level Operation

Yan Lu, Mo Huang, Lin Cheng, Wing-Hung Ki, Seng-Pan U, and Rui P. Martins

FEATURES

Dual-output wireless power receiver
Three-level single-inductor dual-output operation
ISM frequency band, 6.78MHz
Maximum output power, 0.6W
Peak receiver efficiency, 80.5%
Silicon Verified in AMS 0.35μm 5V CMOS

DESCRIPTION

To cut the last wire of the electronic devices, this work presents a 6.78 MHz wireless power transfer (WPT) system for wirelessly powered flash drives that need multiple supplies with a total power of sub-1 W. A new architecture that merges an N-level single-inductor multiple-output switching converter with a multi-stage rectifier is proposed for the WPT receiver, and the regulated outputs attain small ripples. As shown in Fig. 1, the 3-level DC-DC and the SIMO techniques are merged with a 2X rectifier which readily has two DC supplies (3-level). When the V_{AC} amplitude is 3.2 V, V_{DC1} will be 2.7 V and V_{DC2} will be 5.5 V. The higher output voltage V_{O2} retrieves current from V_{DC2} and V_{DC1}, and can be programmed to range from 3.3 V to 5 V for I/O and memory circuits; and the lower output voltage V_{O1} retrieves current from V_{DC1} and Gnd, and can be ranged from 1.0 V to 1.8 V for core circuits. The SIMO converter switches at the WPT frequency of 6.78 MHz.

One benefit of operating the DC-DC converter at the WPT frequency is that, part of the discontinuous rectifier output currents will directly go to the DC-DC converter inputs in every half cycle, bypassing the rectifier load capacitors C_{DC1} and C_{DC2}, thus further reduces the output ripple.

The WPT system was fabricated in a 0.35 μm CMOS process using both 5 V and 3 V devices, and it was measured with the PCB coils shown in Fig. 2. A transmitter (TX) chip consists of a single-ended Class-D power amplifier driving a series LC resonant tank at 6.78 MHz was also fabricated for testing.

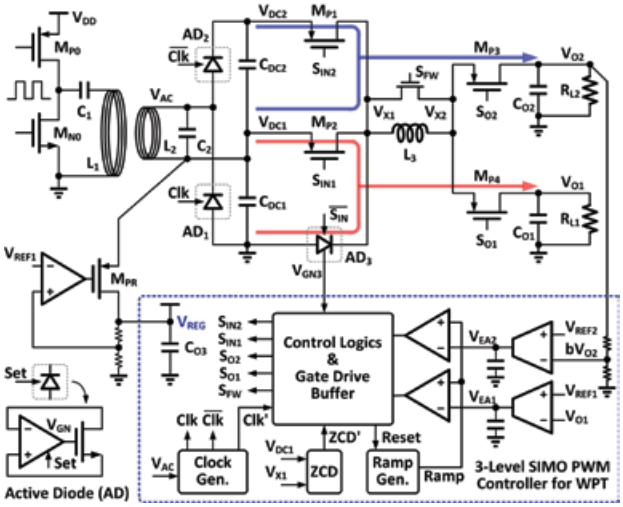

Fig. 1. WPT system with 2X rectifier and three-level SIMO converter.

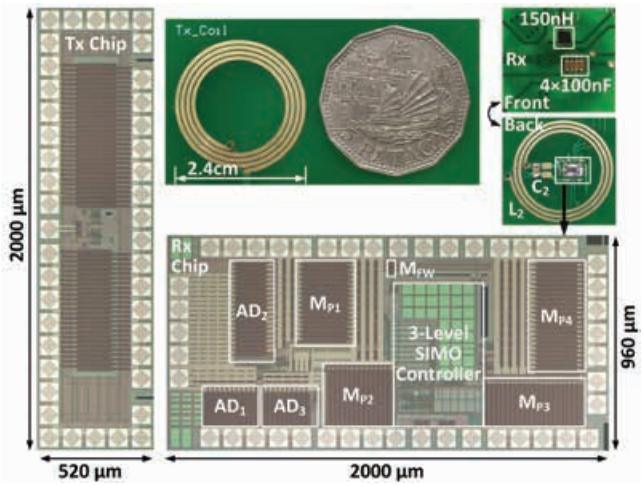

Fig. 2. Chip micrographs and off-chip components of the proposed system.

Publication(s):

[1] Y. Lu*, M. Huang*, L. Cheng, W. H. Ki, S. P. U*, and R. P. Martins*, "A Dual-Output Wireless Power Transfer System With Active Rectifier and Three-Level Operation," IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 927–930, Feb. 2017.

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