RESEARCH ABSTRACTS
ANALOG AND MIXED-SIGNAL CIRCUITS

A Reconfigurable Low-Noise Dynamic Comparator with Offset Calibration in 90nm CMOS

Chi-Hang Chan, Yan Zhu, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Low noise dynamic comparator
Resolution is reconfigurable
On-chip offset calibration
Silicon verified in UMC 90nm CMOS

DESCRIPTION

This paper presents a reconfigurable, low offset, low noise and high speed dynamic clocked-comparator for medium to high resolution Analog to Digital Converters (ADCs). The proposed comparator reduces the input referred noise by half and shows a better output driving capability when compared with the previous work on state-of-the-art.

The offset, noise and power consumption can be controlled by a clock delay which allows simple reconfiguration. Moreover, the proposed offset calibration technique improves the offset voltage from 11.6mV to 533μV at 1 sigma. A prototype of the comparator is implemented in 90nm 1P8M CMOS with experimental results showing 320μV input referred noise at 1.5GHz with 1.2V supply.

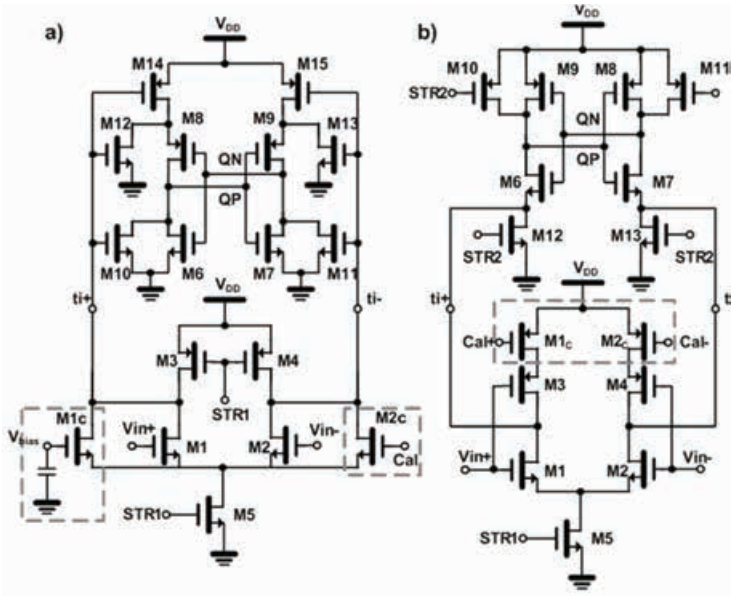

Fig. 1. Circuit schematic of two stage comparator with three times noise improved from conventional one (a) and the proposed comparators (b).

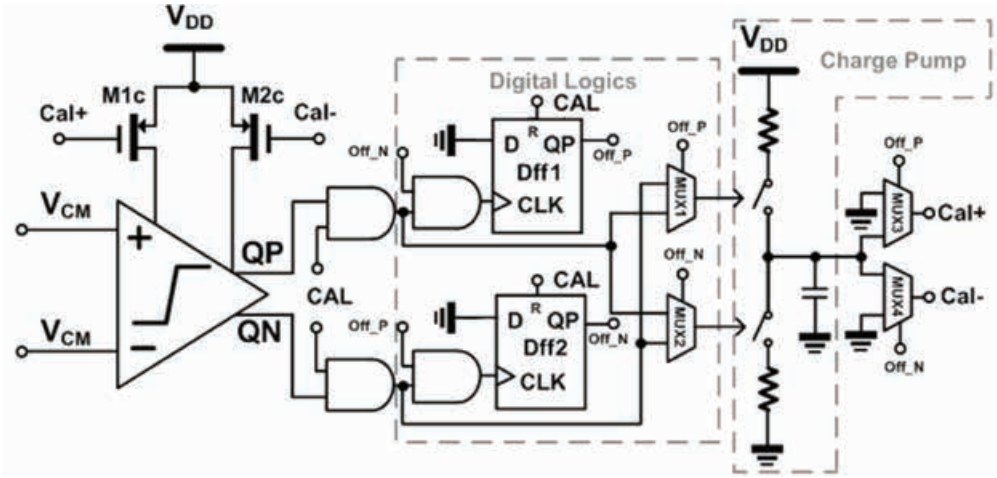

Fig. 2. Circuit schematic of the proposed offset calibration scheme.

Publication(s):

[1] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A reconfigurable low-noise dynamic comparator with offset calibration in 90nm CMOS" in IEEE Asia Solid-State-Circuit-Conference (A-SSCC), pp. 233-236, Nov.2011.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.016-mm² 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With > 0.95-MHz GBW

Zuzhu Yan, Pui-In Mak, Man-Kay Law, and Rui P. Martins

FEATURES

Wide loading range multi-stage amplifier
Current-buffer Miller compensation (CBMC) and parasitic-pole cancellation
Local feedback loop analysis
Silicon verified in standard 350nm bulk CMOS

DESCRIPTION

Most commercial buffer for LCD drivers require an external resistor (e.g., 20Ω for C_L=10 nF) in series with the output for ringing reduction. This regrettably penalizes the cost, settling time and high-frequency gain droop. This work describes a three-stage amplifier managed to afford particularly large and wide range of C_L with optimized power and die size. The control-centric Local Feedback Loop (LFL) Analysis enables effective analysis, comparison and design of three-stage amplifiers at the system level.

Fig. 1 shows the proposed scheme. The outer LFL is built upon CBMC, with the parasitic-pole cancelled by the LHP zero. The proposed active LHP zero circuit generates the desired LHP zero without introducing unwanted low-frequency poles. G_{mb2} offers V-to-I conversion for driving G_{mL} as well as isolation between V_2 and V_3 nodes. This resolve the problem of degraded owing to the passive LHP zero circuit.

Fig. 2 shows the schematic of the proposed three-stage amplifier. G_{m1} ($M_{1\text{-}10}$) is a folded cascode structure featuring a PMOS input differential pair ($M_{1\text{-}2}$). The active LHP zero circuit is embodied in G_{m2} ($M_{11\text{-}14}$) to enhance the power efficiency. G_{mL} (M_{15}) is combined with G_{mf} (M_{16}) to form a push-pull structure. The chip prototype is fabricated in standard 0.35-μm CMOS. Measured AC responses shows that C_L can be as large as 15 nF with 18.1-dB gain and 52.3° phase margins, and as small as 1 nF with 9.8-dB gain and 83.2° phase margins. The extrapolated DC gain is >100 dB. The GBW is 0.95 MHz at 15-nF C_L.

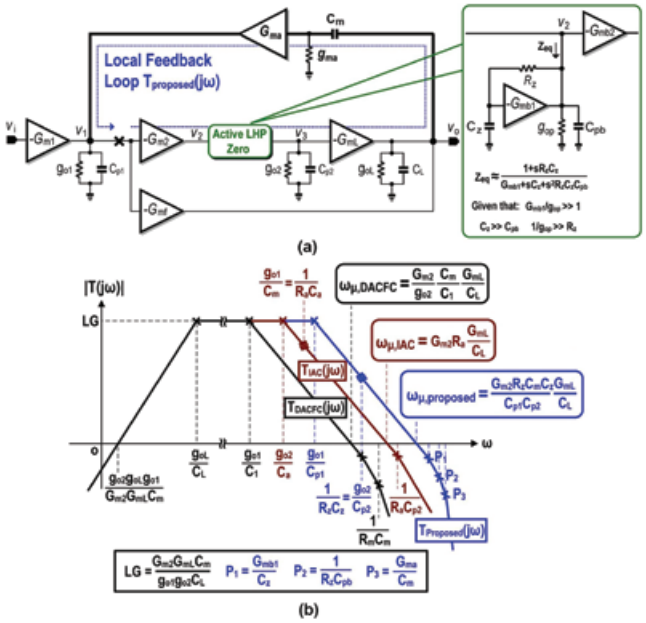

Fig. 1. Proposed scheme using CBMC plus parasitic-pole cancellation, and its (b) LFL bode plot.

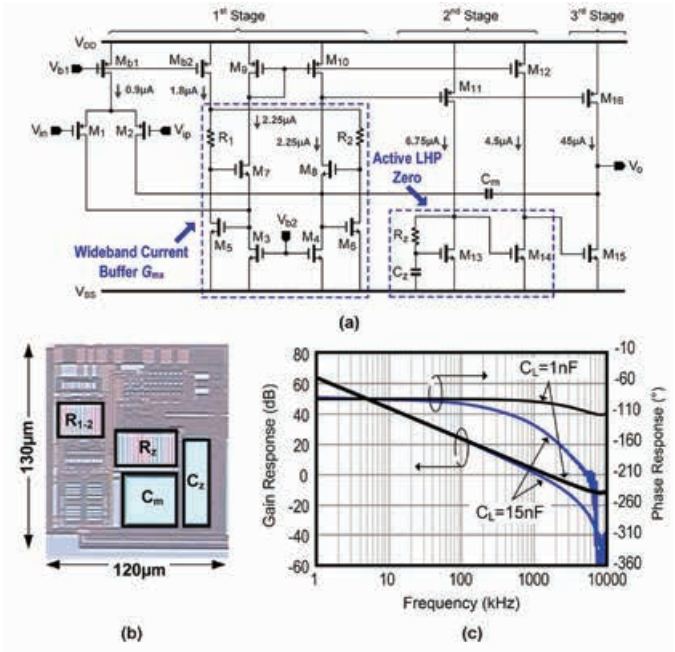

Fig. 2. Schematic of the proposed amplifier (top) and chip photo and measured AC response (bottom).

Publication(s):

[1] Z. Yan, P.-I. Mak, M.-K. Law and R. P. Martins, "A 0.016mm² 144μW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load With >0.95MHz GBW," IEEE Int. Solid-State Circuit Conference (ISSCC), pp. 366-367, Feb. 2012.

[2] Z. Yan, P.-I. Mak, M.-K. Law and R. P. Martins, "A 0.016-mm² 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With > 0.95-MHz GBW," IEEE Journal of Solid-State Circuits, vol. 48, no. 2, pp. 527-540, Feb. 2013.

Sponsorship:

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Nested-Current-Mirror Rail-to-Rail-Output Single-Stage Amplifier With Enhancements of DC Gain, GBW and Slew Rate

Zushu Yan, Pui-In Mak, Man-Kay Law, Rui P. Martins, and Franco Maloberti

FEATURES

Nested-current-mirror (NCM) single-stage amplifier
Improved area and power efficiencies
Improved DC gain, gain-bandwidth product (GBW) and slew rate (SR)
Rail-to-rail output
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

Column drivers for display applications exhibit extremely tight area and power budgets to meet the market pressure on cost and display quality. Plus, due to the fabrication spread and scale alternative of the panels, the buffer amplifiers should master a wide range of capacitive load (C_L) up to tens of nF, while securing adequately large DC gain (e.g., >66 dB for 10 bit resolution) and output swing.

This paper introduces a nested-current-mirror (NCM) single-stage amplifier that can alleviate the tight performance trade-offs in conventional single-stage amplifier topologies, including the fundamental DP amplifier. The prototyped 3-step and 4-step NCM amplifiers achieve favorable performances with respect to the standard DP amplifier, and are comparable with the state-of-the-art of three-stage amplifiers.

The description of the NCM technique consists of two steps (Fig. 1). The first step is to split the DP transistor of the current-mirror amplifier into N sub-transistors M_1 to M_N, and alternately connect their inputs with V_n and V_p. Next, the outputs of M_1 to M_N are combined in sequence via the NCM formed by subdividing a current mirror into pieces with different ratios, which concurrently increases the effective transconductance and output resistance beyond those of the DP, and other single-stage amplifiers. The schematic of a 3-step NCM amplifier is also shown in Fig. 1. The DP transistors are split into M_1-M_3. Their outputs are summed via the NCM mirrors realized by M_4-M_9. M_{10} collects the output of the left, to form the single-ended output together with M_9.

Fig. 2 shows the chip micrograph of the 3-step (top) and 4-step NCM (bottom) and their measured AC responses at C_L=0.15 and 15 nF, showing much improved performance when compared with DP amplifiers, while preserving a rail-to-rail output swing, and wide drivability without entailing any compensation capacitor or resistor.

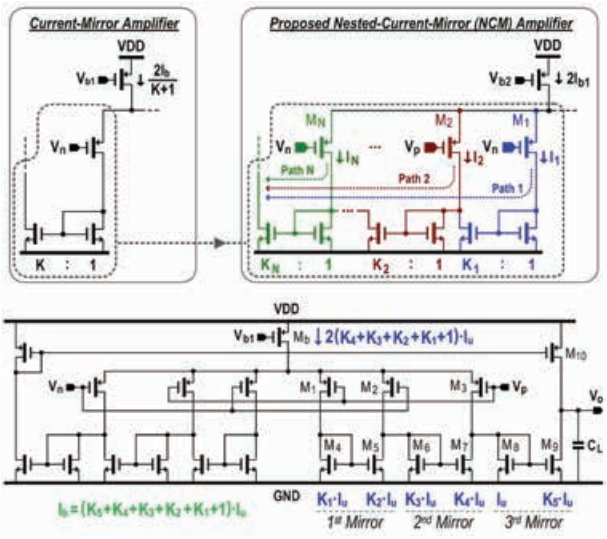

Fig. 1. Development of the NCM amplifier (top) and schematic of the 3-step NCM amplifier (bottom).

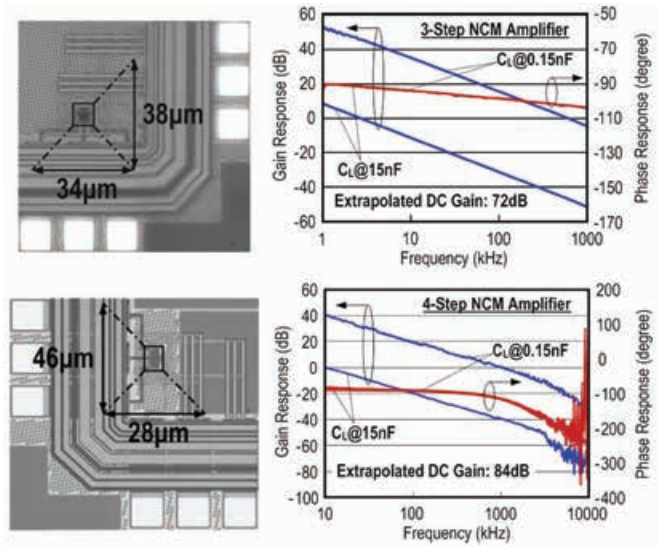

Fig. 2. Chip photo and the measured AC responses for 3-step NCM (top) and 4-step NCM (bottom).

Publication(s):

[1] Z. Yan, P.-I. Mak, M.-K. Law, R. P. Martins, and F. Maloberti, "Nested-Current-Mirror Rail-to-Rail-Output Single-Stage Amplifier with Enhancements of DC Gain, GBW and Slew Rate," IEEE J. of Solid-State Circuits, vol. 50, no. 10, pp. 2353-2366, Oct. 2015.

[2] Z. Yan, P.-I. Mak, M.-K. Law, R. P. Martins, and F. Maloberti, "A 0.0013mm² 3.6μW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Loads with >62° Phase Margin", IEEE Int. Solid-State Circuit Conference (ISSCC), pp. 288 - 289, Feb. 2014.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Precision CMOS Voltage Reference Exploiting Silicon Bandgap Narrowing Effect

Bo Wang, Man-Kay Law, and Amine Bermak

FEATURES

Silicon bandgap narrowing effect for BJT curvature reduction and residual curvature correction
Reduced temperature coefficient after batch trimming
Micropower consumption, 4.3 µA at 25 °C
Excellent Line sensitivity, 0.03%/V
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

To avoid dissipating power driving the curvature correction circuits, this work presents a BGR that only exploits the temperature characteristics of the BJT itself to reduce the $V_{be}(T)$ curvature and to perform residual curvature correction. As the silicon impurity doping concentration becomes particularly high (>10^{18} cm^{-3}), the silicon bandgap narrowing (BGN) occurs. For BJT, due to the BGN induced by the silicon lattice deformation in the heavily doped emitter, its forward current gain becomes strongly temperature dependent. This characteristic is utilized to achieve high precision voltage reference.

The proposed BGR topology with curvature reduction is shown in Fig. 1. A shunt-feedback loop, consisting of an amplifier A_1 and a pass transistor M_{p0}, regulates the voltage across R_{pt}. The input pair of A_1 consists of two matched vertical transistors $Q_{1,2}$ having an emitter ratio of 1:p under the same collector bias. Therefore, A_1 has a PTAT offset voltage $V_{pt}(T)$. $I_{pt}(T)$ mainly serves as Q_0's base bias and the results in curvature in $V_{be0}(T)$.$R_{c1,2}$ are used to amplify $V_{pt}(T)$, thereby compensating the first-order TC of $V_{be0}(T)$. After curvature reduction, the residual can still be large and further correction is preferred. In this work, three X_{TB}-related nonlinear signals can be used to linearize $V_{be0}(T)$, including Q_0's collector current I_{c0}, and the base currents $I_{b1,2}$ of $Q_{1,2}$, if their collector currents are PTAT.

Fig. 2 shows the micrograph of the prototype BGR, which occupies an area of 0.05 mm^2. The 3σ spread of the untrimmed V_{REF} is ±1.06% from −55 to 125 °C with an averaged TC of 36.5 ppm/°C. After batch trimming of R_{c1} at 25 °C for all 12 samples, the resultant spread is reduced to ±0.22%.

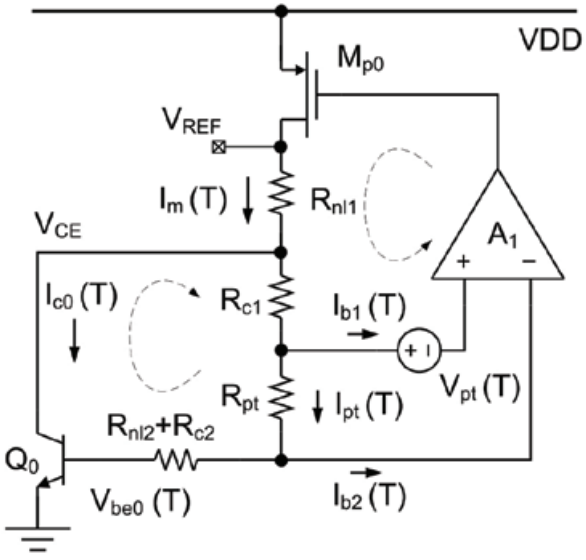

Fig. 1. Proposed BGR topology with curvature reduction and residual curvature correction utilizing the temperature dependency of BGN effect.

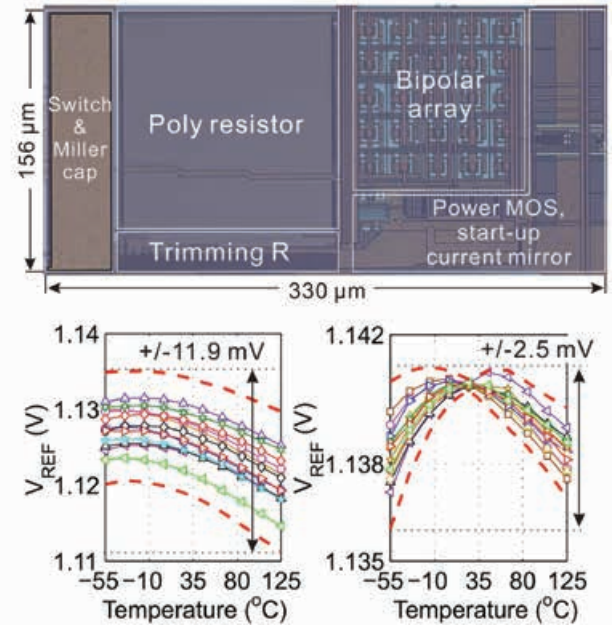

Fig. 2. Chip micrograph (top). Inaccuracy of V_{REF} from 12 samples without trimming (bottom left) and after batch trimming R_{c1} at 25 °C (bottom right).

Publication(s):

[1] B. Wang, M.-K. Law*, and A. Bermak, "A Precision CMOS Voltage Reference Exploiting Silicon Bandgap Narrowing Effect," IEEE Trans. on Electron Device, vol. 62, no. 7, pp. 2128-2135, Jul. 2015.

* Contributors with University of Macau

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BJT Process Spread Compensation Utilizing Base Recombination Current in Standard CMOS

Bo Wang, Man-Kay Law, and Amine Bermak

FEATURES

Minimize BJT inter-/intra-die spread and PTAT drift
Base recombination current for both process and temperature compensation
Standard deviation < 1.8 mV without trimming (30 dies in 2 batches)
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

The designing of a precision Bandgap Reference (BGR) with a temperature coefficient (TC) of 30 ppm/°C over a wide operating temperature is a non-trivial task due to the various error sources introduced during silicon fabrication. BGR error sources such as the amplifier offset, device mismatch and BJT base-emitter voltage (V_{be}) curvature can be mitigated by using circuit techniques like chopping, dynamic element matching and signal linearization. The PTAT drift in V_{be} introduced by BJT spreads (mainly due to the saturation current) ultimately limits the untrimmed BGR precision. This work presents a compensation topology which can minimize the V_{be} spreads of BJTs under different process conditions. This scheme only exploits the electrical properties of a standard BJT and no special process steps are required.

A BJT operating in its deep-saturation region (with tens of mV collector-emitter voltage V_{ce}) is exploited for I_s spread compensation. Under this condition, the electrons are trapped in the base region and strong electron-hole recombination occurs. It can be proved that a strong correlation exists between the recombination current I_r and I_s. As a result, the BJT process spread from I_s can be effectively compensated by injecting an I_r-dependent current into the collector of a BJT. Fig. 1(a) shows the schematic of the proposed BJT spread compensation circuitry, including the start-up block, the bandgap core and the bias/pseudo-supply generator. This design is fabricated in a standard 0.18-µm CMOS process, as shown in Fig. 1(b). The V_{be} STD of 15 standalone BJTs measures 3.24 mV at 25 °C using an external bias current. The compensated V_b (Fig. 1(a) from two batches with on-chip biasing measures only 1.8 mV at 25 °C, as shown in Fig. 1(c). This corresponds to a twofold reduction compared with that without compensation.

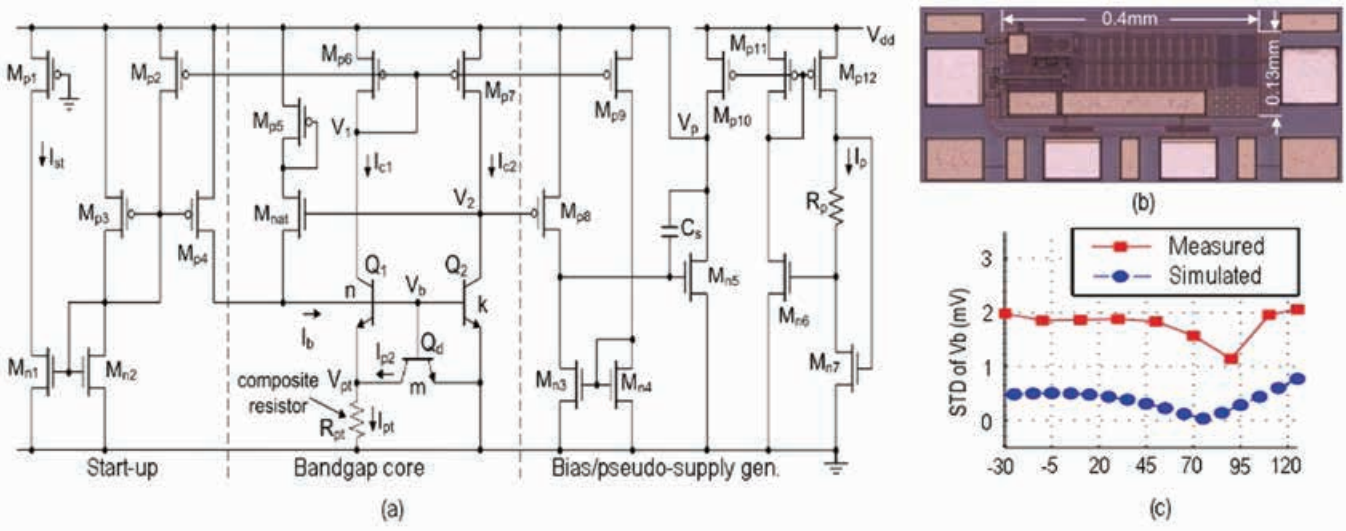

Fig. 1. (a) Schematic of the proposed BJT spread compensation circuitry. (b) Chip micrograph. (c) Measured/Simulated STD of the compensated V_b at different temepratures.

Publication(s):

[1] B. Wang, M.-K. Law*, and A. Bermak, "BJT Process Spread Compensation Utilizing Base Recombination Current in Standard CMOS," IEEE Electron Device Lett., vol. 36, no. 11, Nov. 2015.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong Innovation and Technology Fund

A 2 μW 45 nV/√Hz Readout Frontend With Multiple Chopping Active-High-Pass Ripple Reduction Loop and Pseudo-Feedback DC Servo Loop

Jiangchao Wu, Man-Kay Law, Pui-In Mak, and Rui P. Martins

FEATURES

Active-high-pass filter for filtering capacitor size reduction
Multiple-chopping for residue noise suppression
Pseudo-feedback DSL amplifier with 14nA current bias
Noise-efficiency-factor of 2.9
Silicon verified in standard 180nm bulk CMOS

DESCRIPTION

This work presents a fully integrated low noise chopper-stabilized CCIA with optimized power and area for neural recording applications. Fig. 1(a) presents the proposed neural recording frontend. A single-stage folded-cascode amplifier (G_{m1}) with internal chopping is utilized to achieve low power consumption without loading the amplifier output. The ripple reduction loop (RRL) employs an active high-pass filter composed of a gain stage G_{m2} and a buffer B_2 to further reduce the residual noise from the output and relax the value of C_3. The RRL output is fed back to the main amplifier internally instead of to the main amplifier output to increase the RRL loop gain. Reusing the current of G_{m1} can reduce the overall power consumption while avoiding additional poles that can degrade the system stability.

Multiple chopping is proposed to modulate the RRL offsets to high frequency and to suppress the output ripple. V_{OS2} and V_{OS3} are modulated by using a high chopping frequency f_{high}. As a result, V_{OS2} is modulated to f_{chop} at the input of G_{m3}, with additional high frequency images suppressed by C_3.

The remaining offsets (V_{OS3} at DC and V_{OS2} at f_{chop}) are then up-modulated by f_{high}, with the high order harmonics further filtered by C_3 and C_L. An ultra-low bandwidth pseudo-feedback buffer B_3 is inserted before G_{m4} to achieve a sub-Hz high-pass corner with reduced loading capacitance while dissipating only 14 nA using only a 15 pF on-chip capacitor. Instead of using a large loading capacitor to reduce the DSL induced IRN, the DSL output is fed back to the internal node of the main amplifier that can simultaneously reduce the IRN and the loading capacitor requirement.

The complete neural acquisition frontend was implemented in a standard 0.18 μm CMOS technology. The gain is designed to be approximately 34 dB with a chopping frequency of 20 kHz. This work achieves the smallest RRL + main amplifier (C_{RRL}+ C_L) and DSL (C_{DSL}) filtering/loading capacitance while preserving low IRN. The reduced power consumption by the RRL current reuse and the DSL pseudo-feedback amplifier with internal feedback leads to a NEF of 2.9.

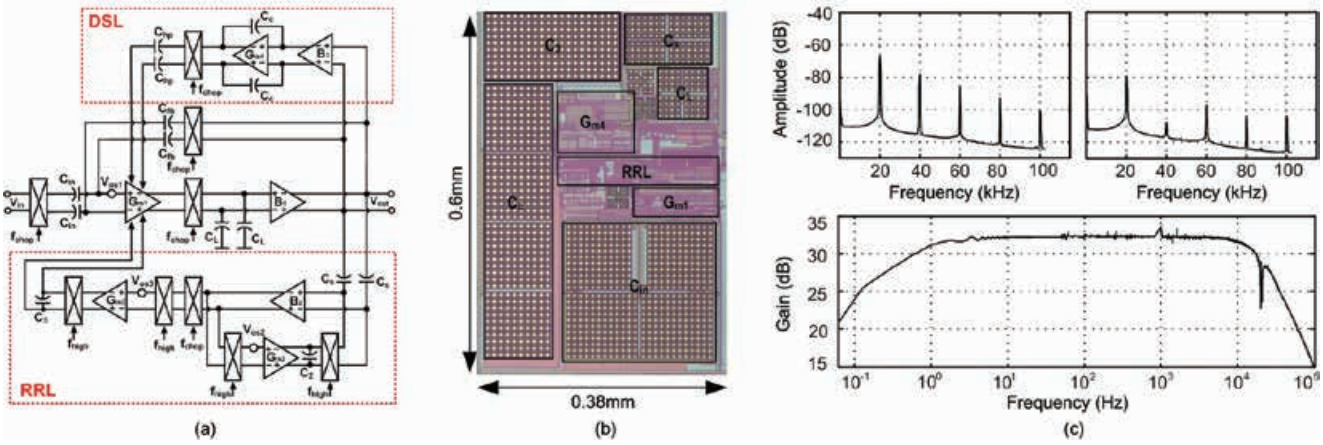

Fig. 1. (a) The proposed chopper-stabilized CCIA topology. (b) Chip photograph. (c) Measured output spectrum and transient waveform of the CCIA with f_{chop}=20 kHz and f_{high}=20 kHz (top left), f_{chop}=20 kHz and f_{high}=80 kHz (top right), and measured frequency response of the complete CCIA (bottom).

Publication(s):

[1] J. Wu, M.-K. Law, P.-I. Mak and R. P. Martins, "A 2 μW 45 nV/√Hz Readout Frontend With Multiple Chopping Active-High-Pass Ripple Reduction Loop and Pseudo-Feedback DC Servo Loop," IEEE Trans. on Circuits Syst. II, Exp. Briefs, vo. 63, no. 4, pp. 351-355, Apr. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Hong Kong Innovation and Technology Fund