RESEARCH ABSTRACTS
SUB-GHz to GHz ADCs

A 4.8-bit ENOB 5-bit 500MS/s Binary-Search ADC with Minimized Number of Comparators

Si-Seng Wong, U-Fat Chio, He-Gong Wei, Chi-Hang Chan, Hou-Lon Choi, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

High Speed Binary Search ADC
Reduced Comparators from 2N-1 to N
Low Power consumption 1.63mW
Very High Sampling Rate 500MS/s
5b Resolution, SNDR=30.7dB
Good Power efficiency, FoM_W=117fJ/step
Very Small Active Area, 0.015mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a topology to improve the system linearity and reduce the complexity of high-speed binary-search ADCs. The proposed topology, when compared with previous binary-search ADC architectures, further reduces the number of comparators from 2N-1 to N for N-bit precision, the comparator structure is simplified, and it can avoid both the signal dependent offsets and the kickback noise. The kickback noise injected to the current stage does not affect the output because the comparator has already quantized the output of the current stage during the kickback. The proposed binary-search ADC has been implemented in 65nm CMOS process and it consumes 1.63mW at an operation frequency of 500MS/s. The measurement results demonstrate that the binary-search ADC achieves 30.7dB SNDR (4.8-bit ENOB).

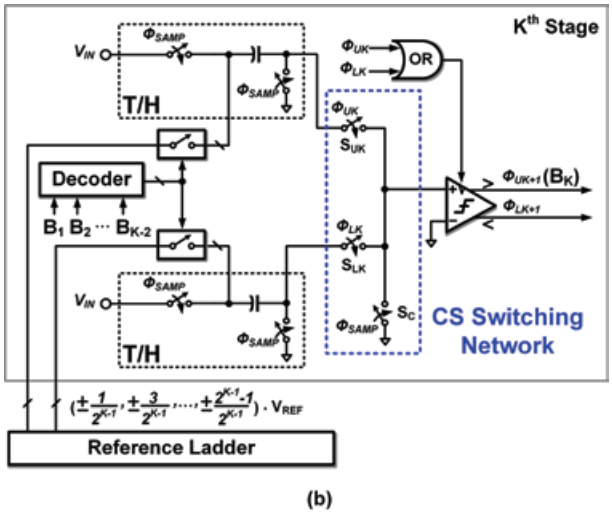

Fig. 1. Scheme of Kth stage of the proposed binary-search ADC.

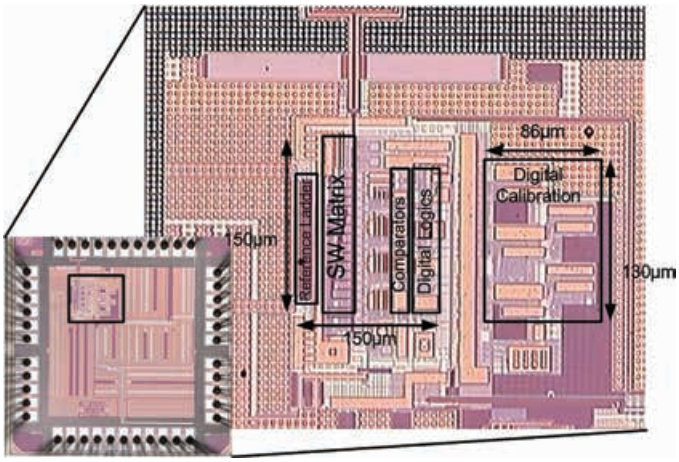

Fig. 2. Chip Photograph.

Publication(s):

[1] S.-S. Wong, U-F. Chio, C.-H. Chan, H.-L. Choi, S.-W. Sin, S.-P. U, R. P. Martins, "A 4.8-bit ENOB 5-bit 500MS/s Binary-Search ADC with Minimized Number of Comparators," in IEEE Asian Solid-State Circuit Conference – A-SSCC, pp. 73-76, Nov 2011.

* Contributors with University of Macau

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Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

2b/cycle SAR ADC
VCM-based multi-bit switching
~34fJ/conversion-step walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

An 8b 1GS/s ADC is presented that interleaves two 2b/cycle SARs. To enhance speed and save power, the prototype utilizes segmentation switching and custom-designed DAC array with high density in a low parasitic layout structure. It operates at 1GS/s from 1V supply w/o interleaving calibration and consumes 3.8mW of power, exhibiting a FoM of 24fJ/conv. step. The ADC occupies an active area of 0.013mm2 in 65nm CMOS including on-chip offset calibration.

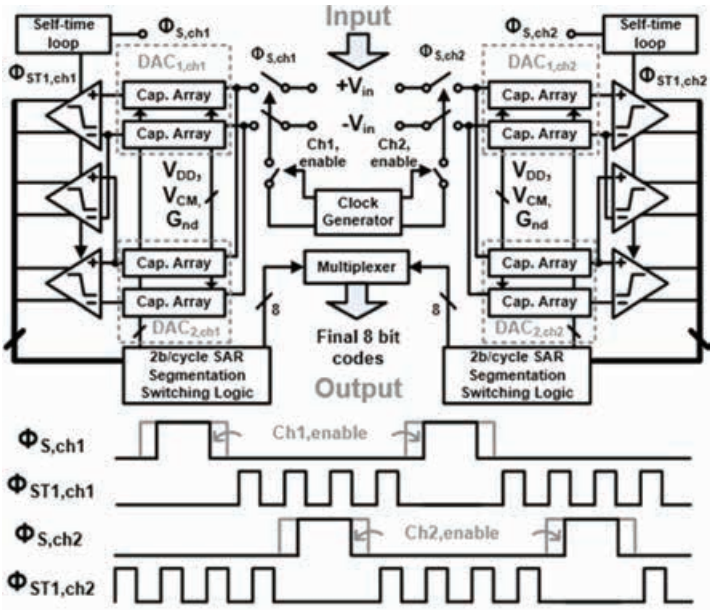

Fig. 1. Overall ADC architecture and its timing diagram.

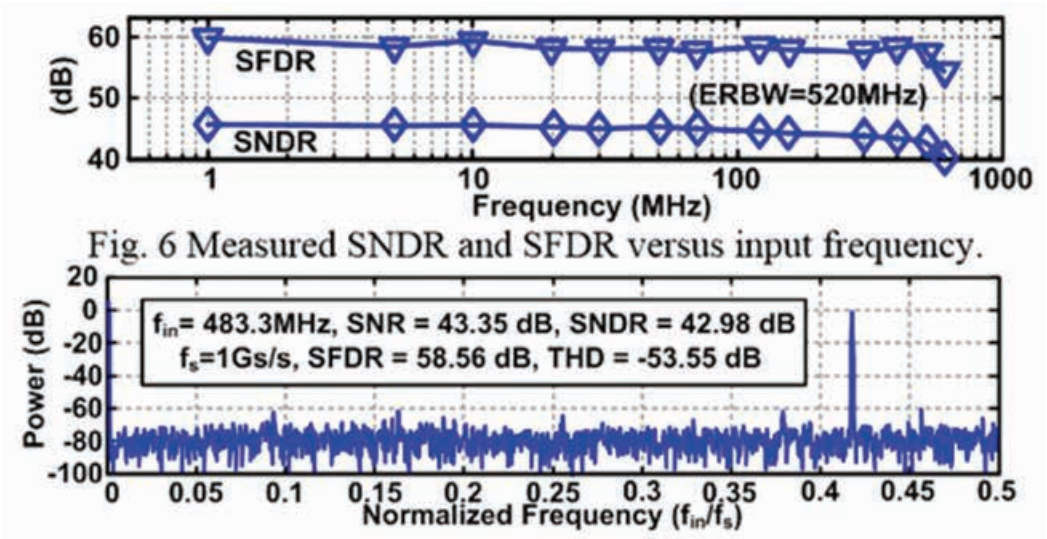

Fig. 2. Spectrum at 1GS/s and Nyquist input (decimated 125x).

Publication(s):

[1] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure," in IEEE Symposia on VLSI Technology and Circuit (VLSIC), pp. 86-87, Jun. 2012.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.024mm² 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65 nm CMOS

He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

2b/cycle SAR
On-Chip Digital Calibration
Low power consumption, 4mW
High Sampling Rate, 400MHz
Excellent Power efficiency, 73fJ/step
Very Small Active Area, 0.028mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This design is a power efficient ADC solution with up to 400MS/s conversion rate based on a (2b/Cycle) SAR topology that uses a resistive-based 2-bit DAC and several power/area reduction techniques, like interpolation in the sampling network, which reduces 33% of the hardware of the sampling circuit, DAC switches and digital decoder. Moreover, cascaded inverters in the decoder instead of the conventional AND/NAND gates saves by 2/3 the number of transistors leading to low-power performance and faster operation. Furthermore, a cross-coupled bootstrapping network alleviates the signal-dependent clock feed-through. The proposed SAR ADC achieves rapid conversion rate, low-power and compact area leading to SNDR of 44.5dB and SFDR of 54.0dB, at 400MS/s with 1.9MHz input. The measured FOM is 73fJ/conversion-step at 400MS/s from 1.2V supply and 42fJ/conversion-step at 250MS/s from 1V supply. The active area with the digital calibration is 0.028mm².

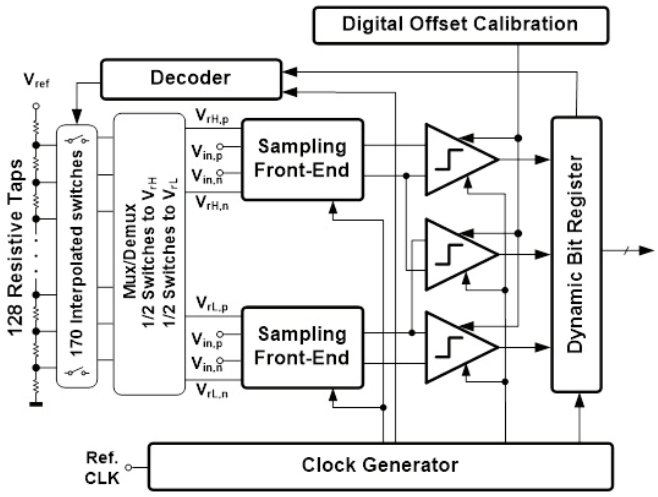

Fig. 1. ADC architecture.

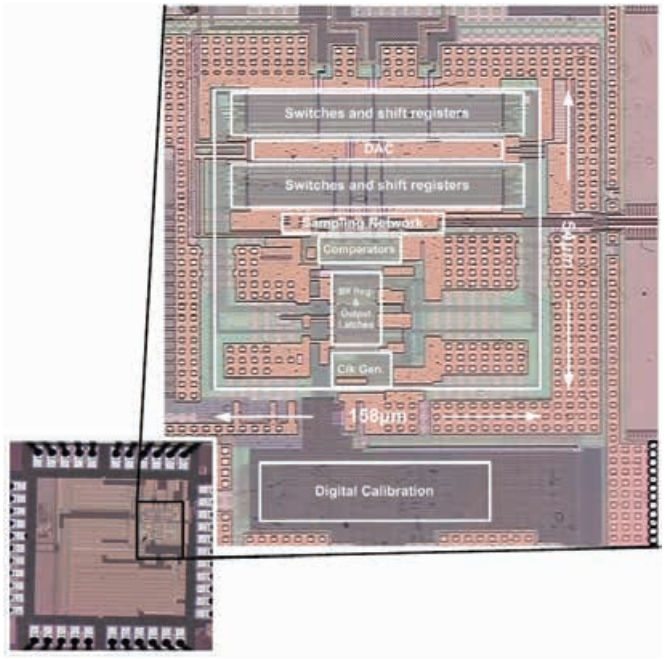

Fig. 2. Chip Photograph.

Publication(s):

[1] H.-G. Wei, C.-H. Chan, U-F. Chio, S.-W. Sin, S.-P. U, R. P. Martins, F. Maloberti, "A 8-bit 400MS/s 2-bit per cycle SAR ADC with Resistive DAC", IEEE Journal of Solid-State Circuits, vol. 47, Issue 11, pp. 2763-2772, Nov 2012.

[2] H.-G. Wei, C.-H. Chan, U-F. Chio, S.-W. Sin, S.-P. U, R. P. Martins, F. Maloberti,"A 0.024mm2 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65 nm CMOS," in IEEE International Solid-State Circuit Conference (ISSCC), vol. 54, pp.188-189, Feb 2011. (ISSCC Silk Road Award)

* Contributors with University of Macau

Sponsorship:

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A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC

Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Partial-Interleaving Architecture
Shared opamp in TI pipeline SAR
Offset calibration onchip
~30 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

A 10b 500MS/s ADC is presented that shares a full-speed SAR at front-end and interleaves the pipelined residue amplification with shared opamp and 2nd-stage SAR ADCs, which achieves high speed, low power and compact area.

The prototype ADC in 65nm CMOS achieves a mean SNDR of 55.4dB with 8.2mW power dissipation at 1.2V. The active die area including the offset calibrations is 0.046mm^2.

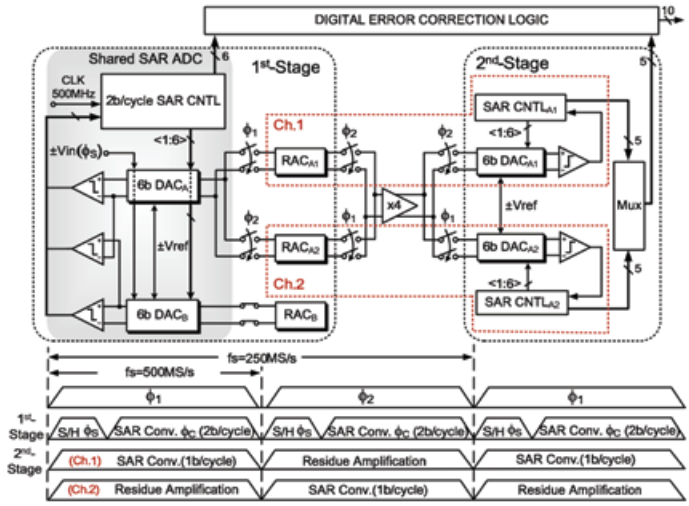

Fig. 1. Overall ADC architecture and its timing diagram.

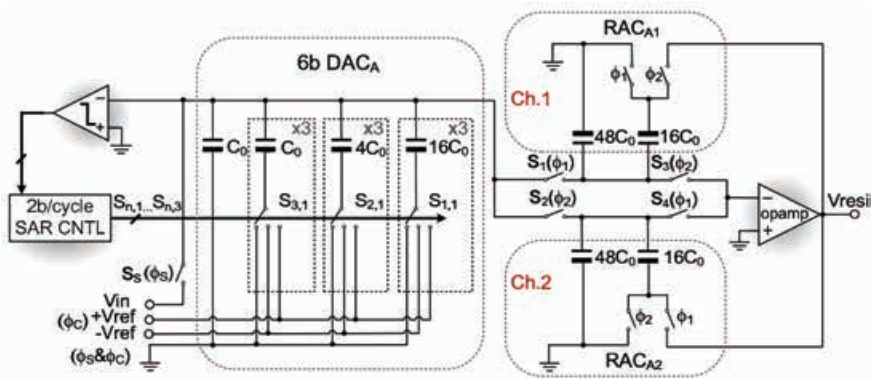

Fig. 2. 1st-stage 6b SAR ADC w/ Opamp-shared TI-Residue Amplification.

Publication(s):

[1] Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC", IEEE Symposium on VLSI Circuits, pp 90-91, Jun-2012.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Passive Folding
Embedded Reference
On-chip offset calibration
Gain calibration
~23 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a 5-bit 1.25-GS/s folding flash ADC. The prototype achieves a folding factor of four with a capacitive folding technique that only consumes dynamic power. Incorporated with various calibration schemes, folding errors and the comparator's threshold inaccuracies are corrected, thus allowing a low input capacitance of 80 fF. The design is fabricated using 65-nm digital CMOS technology and occupies 0.007 mm.

The maximum DNL and INL post calibration are 0.67 and 0.47 LSB, respectively. Measurement results show that the ADC can achieve 1.25 GS/s at 1-V supply with a total power consumption of 595 W. In addition, it exhibits a mean ENOB of 4.8b at dc among ten chips, which yields an FoM of 17 fJ/conversion-step.

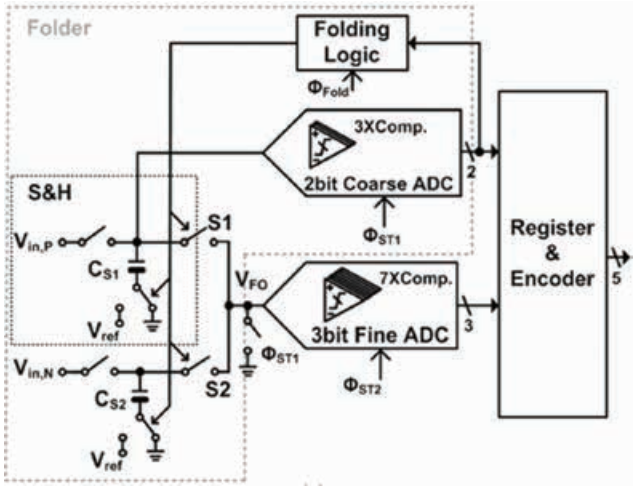

Fig. 1. ADC Architecture (actual implementation is in differential).

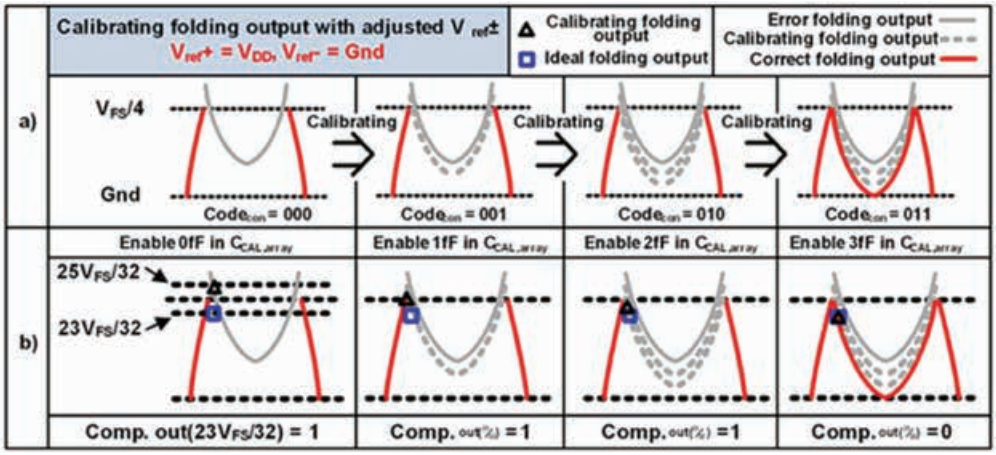

Fig. 2. Folding-reference calibration scheme and its signals behavior.

Publication(s):

[1] C.-H. Chan*, Y. Zhu*, S.-W. Sin*, S.-P. U*, R. P. Martins*, and F. Maloberti, "A 5b 1.25GS/s 4X Capacitive Folding Flash ADC in 65nm CMOS," IEEE Journal of Solid-State Circuits, vol. 48, no. 9, pp. 2154 -2169, Sep. 2013.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

An 11b 900 MS/s Time-Interleaved Sub-ranging Pipelined-SAR ADC

Yan Zhu, Chi Hang Chan, Seng-Pan U, and Rui P. Martins

FEATURES

Hybrid ADC architecture
Channel Selection Embedded boostrap to reduce clock skew effect
Calibration onchip
~56 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a sub-ranging 6-way time-interleaved pipelined-SAR ADC that achieves 900MS/s and 9.3 ENOB in 65nm CMOS. The architecture optimization is based on a pipelined-SAR structure that obtains high-speed with an optimized number of channels, thus leading to relaxed calibration with higher efficiency in power and area consumption.

The proposed channel-selection-embedded bootstrap performs sampling instants synchronization without additional components, thus effectively suppressing the spurs from time skews below -65 dBFS. The mismatch errors due to offset and gain are all solved on-chip, whose spurs are suppressed below -67 dBFS. The prototype achieves 66 dB SFDR and 51.5 dB SNDR with a Nyquist input exhibiting a FoM of 56 fJ/conv.step.

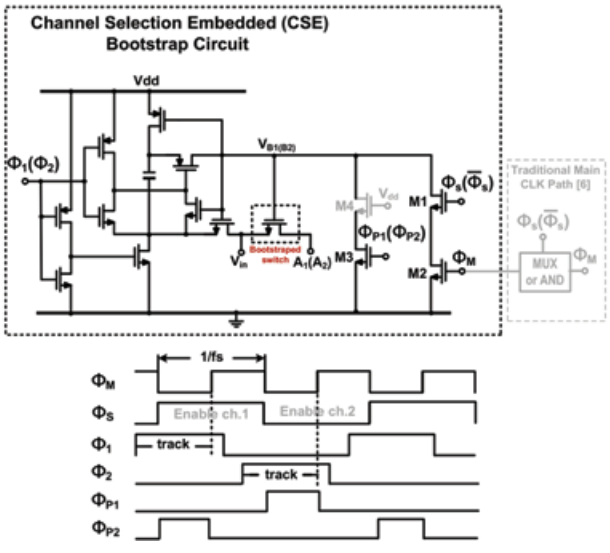

Fig. 1. Proposed Channel-Selection-Embedded bootstrap circuit and its control timing diagram.

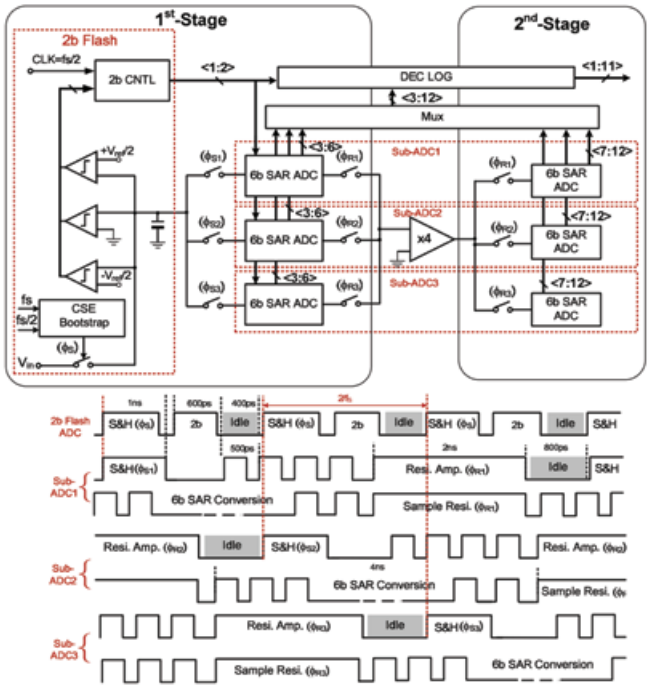

Fig. 2. Main channel ADC architecture and its timing diagram.

Publication(s):

[1] Y. Zhu, C. H. Chan, S.-P. U, and R. P. Martins, "An 11b 900 MS/s Time-Interleaved Sub-ranging Pipelined-SAR ADC", IEEE European Solid-State Circuit Conference – (ESSCIRC), pp.211-214, Sep-2014.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of the University of Macau

A 89fJ-FOM 6-bit 3.4GS/s Flash ADC with 4x Time-Domain Interpolation

Jianwei Liu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Time-based Flash-Subranging ADC
On-Chip Calibration
4x Time-Domain Interpolation Technique
Low power consumption, 12.6mW
Very High Sampling Rate, 3.4GS/s
Excellent Power efficiency, 89fJ/step
Very Small Active Area, 0.034mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 6-bit 3.4 GS/s flash ADC in 65 nm CMOS. The proposed 4x time-domain interpolation technique allow reducing reduction of the number of comparator from conventional 63 to 16 in a 6-bit flash ADC.

Without extra clocking and calibration in the interpolated stage, the proposed scheme effectively achieves 4x interpolation factor with simply SR-latches.

Offset calibration only applies in the comparators and is implemented on-chip. (how about the time-offsets?) Measurement results show that the prototype can achieve 3.4 GS/s with a total power consumption of 12.6 mW at 1 V supply. Besides, it exhibits a 34.219 dB SNDR at Nyquist, which yields a Walden FoM of 89 fJ/conversion-step.

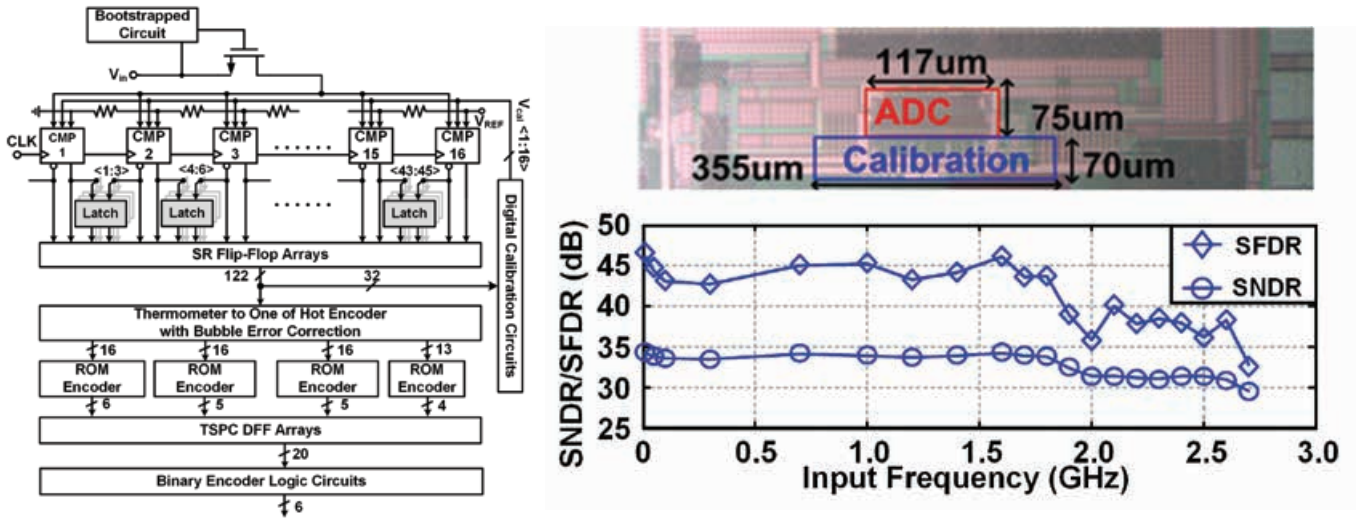

Fig. 1. The ADC architecture, the Chip Photograph and Dynamic Performance.

Publication(s):

[1] J. Liu, C.-H. Chan, S.-W. Sin, S.-P., U, R. P. Martins, " A 89fJ-FOM 6-bit 3.4GS/s flash ADC with 4x time-domain interpolation", in IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 1-4, Nov 2015.

[2] J. Liu, C.-H. Chan, S.-W. Sin, S.-P., U, R. P. Martins, " A 4x Time-Domain Interpolation 6-bit 3.4GS/s 12.6mW Flash ADC in 65nm CMOS", in Journal of Semiconductor Technology and Science, Vol. 16, No. 4, pp. 395-404, Aug 2016.

* Contributors with University of Macau

Sponsorship:

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An 8-bit 0.7-GS/s Single Channel Flash-SAR ADC in 65-nm CMOS Technology

Dante Gabriel Muratore, Alper Akdikmen, U-Fat Chio, Edoardo Bonizzoni, Sai-Weng Sin, Rui Paulo Martins, Franco Maloberti,

FEATURES

Single Channel Flash-SAR Subranging Scheme
Preamplifier with intepolated thresholds generation
Low power consumption, 6mW
High Sampling Rate, 700MS/s
Excellent Power efficiency, 87fJ/step
Very Small Active Area, 0.033mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents the prototype of a single channel 8-bit 0.7-GS/s A/D converter implemented in a 65-nm CMOS process. The result, comparable with the one obtained with smaller line-widths, benefits from an architecture made by the cascade of a 4-bit flash and a two-step SAR converter. Both steps determine 3-bit. The 4+3+3 bits give rise to the 8-bit output; the applied redundancy avoids calibration in the first two stages. The required thresholds are generated from the resistive interpolation embedded within the pre-amplifiers preceding the latches. The active area of the chip is 150 x 220 μm^2 and the total power consumption is 5.96 mW. At Nyquist, the ADC achieves 6.62 ENOB, resulting in a figure of merit equal to 86.7 fJ/conversion-step.

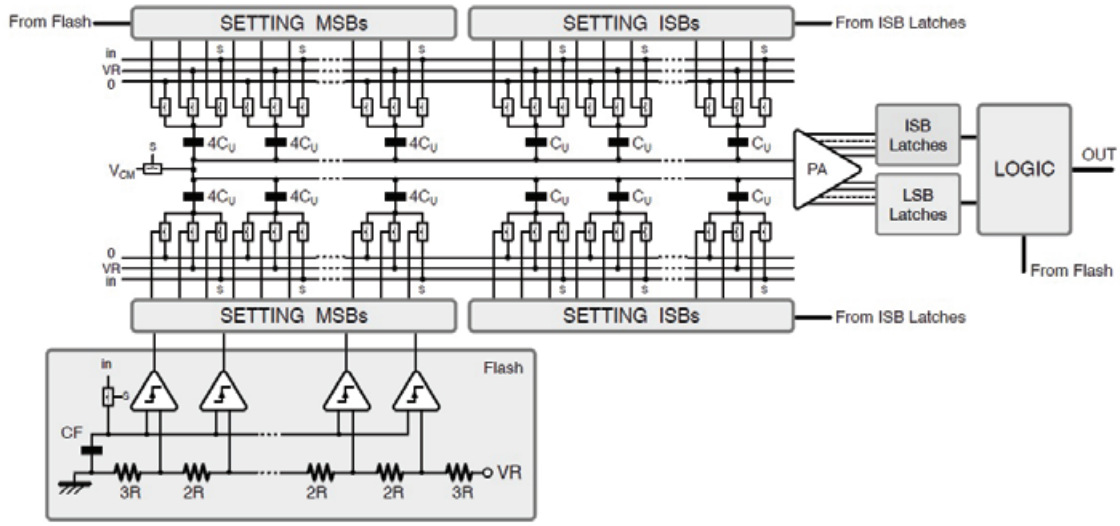

Fig. 1. ADC architecture

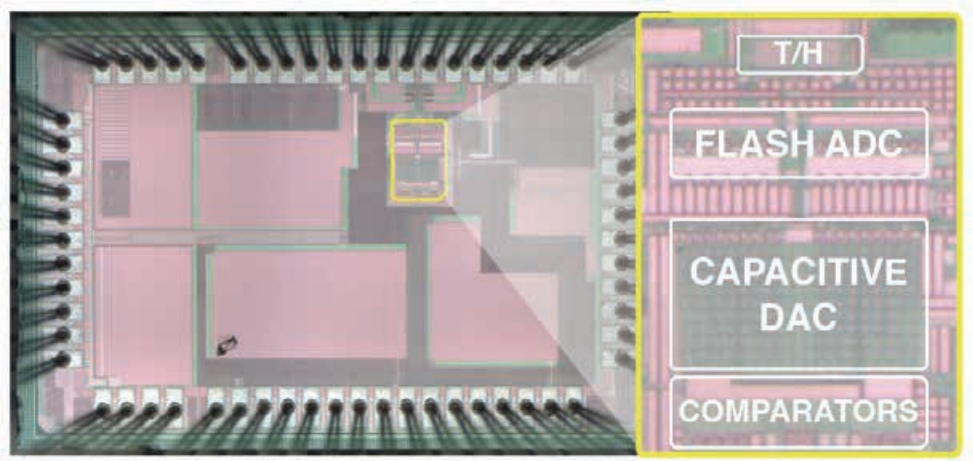

Fig. 2. Chip Photograph

Publication(s):

[1] 1. Dante Gabriel Muratore, Alper Akdikmen, U-Fat Chio*, Edoardo Bonizzoni, Sai-Weng Sin*, Rui Paulo Martins*, Franco Maloberti,"An 8-bit 0.7-GS/s Single Channel Flash-SAR ADC in 65-nm CMOS Technology ", in Proc. IEEE European Solid-State Circuits Conference – ESSCIRC 2016, pp. 421-424, Sept 2016.

* Contributors with University of Macau

Sponsorship:

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A 6-b 5GS/s 4-Interleaved 3b/cycle SAR ADC

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

3b/cycle SAR Architecture
VCM-less Switching
On-chip offset calibration
Boundary Detection Code Overriding
~39 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a 4x time-interleaved 6-bit 5 GS/s 3b/cycle SAR ADC. Hardware overhead induced by a 3b/cycle architecture is eased by an interpolation technique where around 1/3 of the hardware is saved. In addition, complicated switching controls are simplified with a proposed fractional DAC array switching scheme, thus reducing the design complexity and the hardware burden. A boundary detection code overriding is introduced to reduce error probability at the large error magnitude, by utilizing the extended time when the comparator is at reset and the DAC at settling.

The floorplan of the front-end is optimized for important interleaving clock distributions, and a master-clock-control bootstrapped-switch technique is adopted to suppress the timing skew effect among the channels. The unit capacitor has been designed to suit for the DAC structure which allows top-plate sharing in both directions, plus, the offset is calibrated on-chip with a clocking variable biasing transistor pair at the latch. Measurement results show that the prototype can achieve 5 GS/s with a total power consumption of 5.5 mW at 1 V supply in 65 nm CMOS technology. Besides, it exhibits a 30.76 dB SNDR and 43.12 dB SFDR at Nyquist, which yields a Walden FoM of 39 fJ/conversion-step.

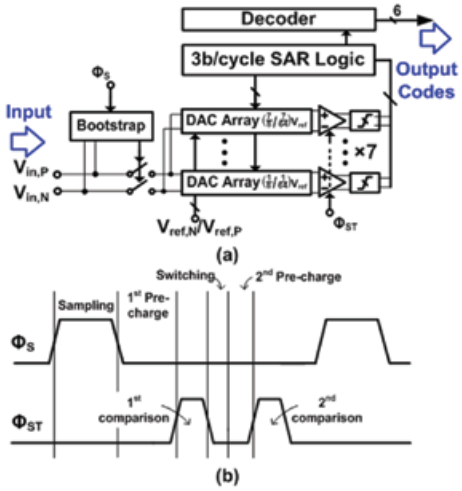

Fig. 1. The ADC (a) architecture and (b) timing diagram with time allocation.

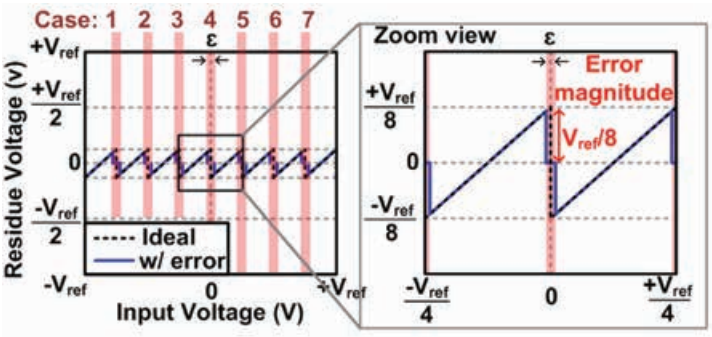

Fig. 2. Ideal and error (dot line) residue transfer curves of 6 bits 3b/cycle SAR with non-differential controls of the DACs in the red regions.

Publication(s):

[1] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 5.5mW 6-b 5GS/s 4-Interleaved 3b/cycle SAR ADC in 65nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 51, no. 2, pp. 365-377, Feb. 2016.

[2] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 5.5mW 6b 5GS/S 4×-interleaved 3b/cycle SAR ADC in 65nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), pp.1-3, Feb. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS

Yan Zhu, Chi Hang Chan, Seng-Pan U, and Rui P. Martins

FEATURES

Hybrid ADC Architecture
Flash + Pipeline SAR + Interleaving
Offset and gain calibration
~32 fJ/conversion-step Walden FoM
Silicon verified in GF 65nm CMOS

DESCRIPTION

This paper presents an 11 bit 450 MS/s three-way time-interleaved (TI) subranging pipelined-successive approximation register (SAR) analog-to-digital converter (ADC).

The proposed hybrid architecture combines the design benefits of different ADC structures to achieve a high conversion rate and accuracy with good power efficiency. The design employs multiple offset calibration schemes to compensate the offset mismatches at each stage.

The solutions require less calibration efforts, thus allowing the ADC to achieve a compact area. Furthermore, a dynamic SAR controller embedded with error-decision-correction (EDC) logic is proposed to reduce large transition error. Measurement results on a 65 nm CMOS prototype operated at 450 MS/s and 1.2 V supply show 7.4 mW total power consumption with a peak signal-to-noise distortion ratio (SNDR) of 60.8 dB and an FOM of 32 fJ/conv.step at Nyquist.

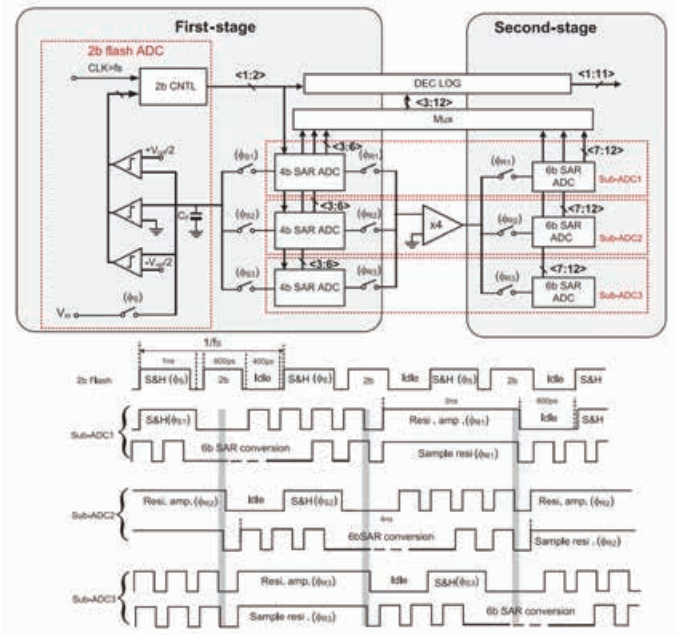

Fig. 1. Overall ADC architecture and its timing diagram.

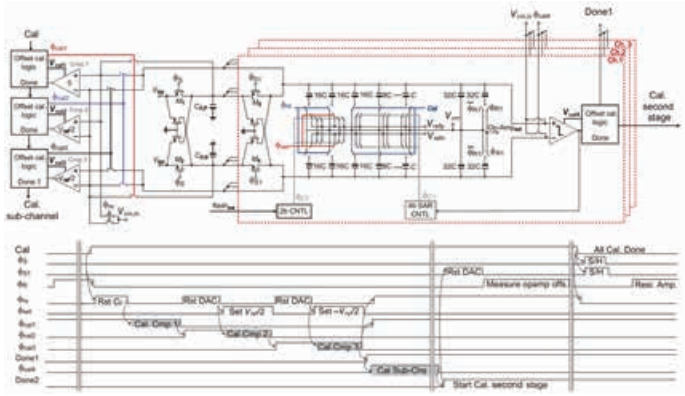

Fig. 2. Detailed circuit implementation of the first stage and offset calibrations for two stages together with its control timing diagram.

Publication(s):

[1] Y. Zhu, C. H. Chan, S.-P. U, R. P. Martins, "An 11b 450 MS/s three-way Time-Interleaved Sub-ranging Pipelined-SAR ADC in 65nm CMOS", IEEE Journal of Solid-State Circuits, Feb-2016.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial V_{cm}-Based Switching

Dezhi Xing, Yan Zhu, Chi Hang Chan, Sai Weng Sin, Fan Ye, Junyan Ren, Seng-Pan U, and Rui P. Martins

FEATURES

Partial Vcm-based switching
Low power and small common-mode variation
Offset calibration offchip
~48 fJ/conversion-step Walden FoM
Silicon verified in TSMC 65nm CMOS

DESCRIPTION

This brief presents a 7-bit 700-MS/s four-way time-interleaved successive approximation register (SAR) analog-to-digital converter (ADC). A partial V_{cm}-based switching method is proposed that requires less digital overhead from the SAR controller and achieves better conversion accuracy. Compared with switchback switching, the proposed method can further reduce the common mode variation by 50%. In addition, the impacts of such a reduction on the comparator offset, noise, and input parasitic are theoretically analyzed and verified by simulation.

The prototype fabricated in a 65-nm CMOS technology occupies an active area of 0.025 mm^2. The measurement results at the 700 MS/s sampling rate show that the ADC achieves signal-to-noise-and-distortion ratio of 40 dB at Nyquist input and consumes 2.72 mW from a 1.2 V supply, which results in a Walden FoM of 48 fJ/conversion step.

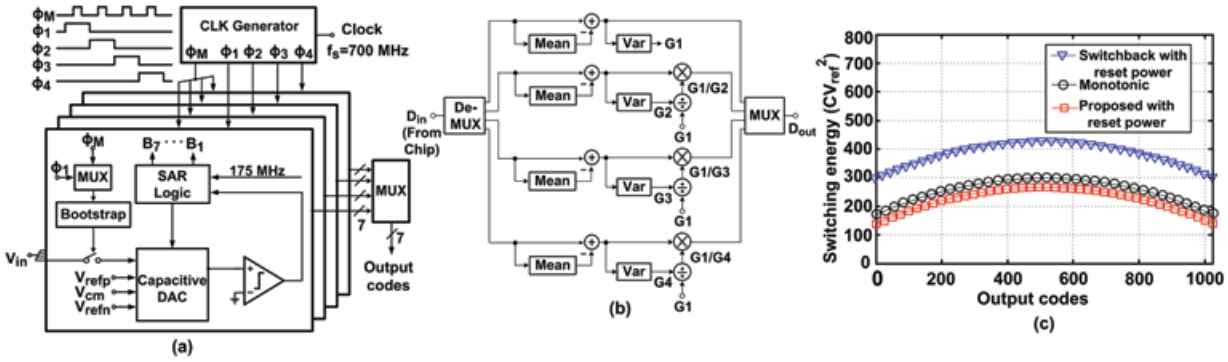

Fig. 1. (a) Overall ADC architecture. (b) Offset/gain mismatches calibration. (c) Switching energy versus output code of a 10-b SAR, including the reset power during sampling.

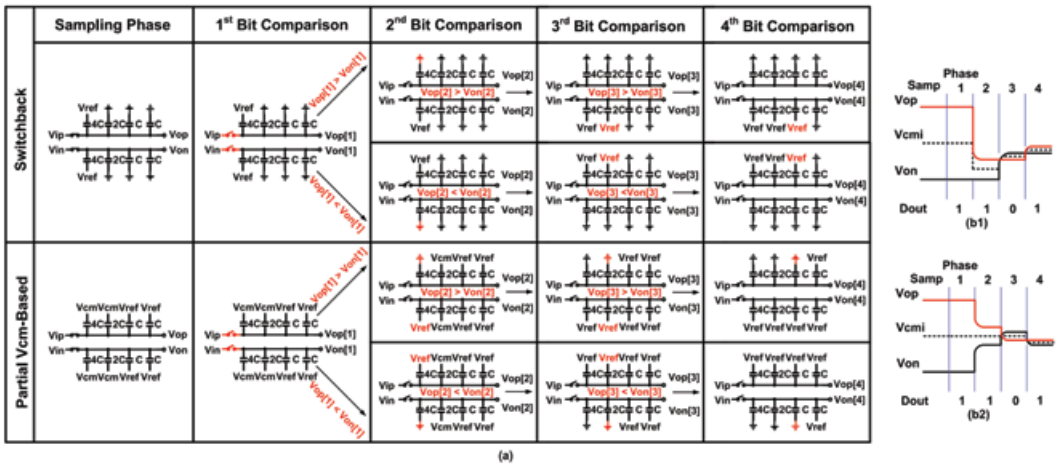

Fig. 2. (a) 4-b example of switchback and partial Vcm-based switching procedures. (b1) Comparator input common mode variation for switchback switching. (b2) Comparator input common mode variation for the proposed switching.

Publication(s):

[1] D. Xing*, Y. Zhu*, C. H. Chan*, S. W. Sin*, F. Ye, J. Ren, S.-P. U*, R. P. Martins*, "Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial Vcm-Based Switching", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Oct-2016.

* Contributors with University of Macau

Sponsorship:

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A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration

Chi-Hang Chan, Yan Zhu, Iok-Meng Ho, Wai-Hong Zhang, Seng-Pan U, and Rui P. Martins

FEATURES

1-then-2b operation
Merge Pre-charge Switching
Background offset calibration
Robust on PVT variation
~25 fJ/conversion-step Walden FoM
Silicon verified in GF 28nm CMOS

DESCRIPTION

This work features a 2x time-interleaved 7b 2.4GS/s 1-then-2b/cycle SAR ADC in 28nm. By quantizing 1b first followed by a 2b/cycle SAR and a dedicated arrangement of the SA control, the conventional pre-charging operation can be saved.

Offset among the comparators is calibrated in the background without requiring extra cycle or reference voltage. The design consumes 5mW with 40.05dB SNDR@Nyq., resulting in a Nyq.-FoM of 25.3fJ/conv.-step. SNDR@low stays >38dB with a wide range of V&T variation.

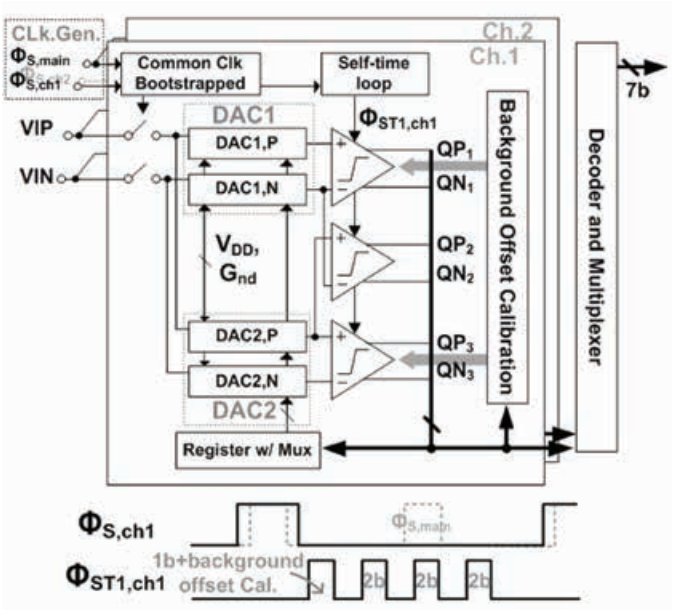
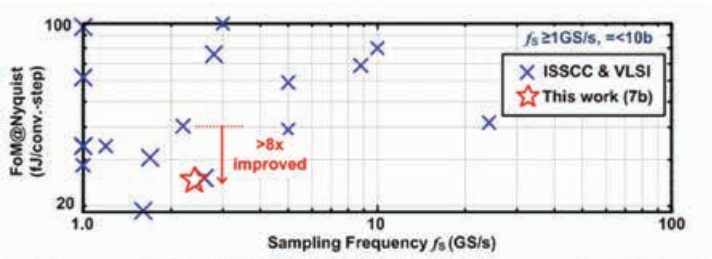


Fig. 1. Overall 2x interleaved 1-then-2bit/cycle SAR ADC architecture.



Publication	ISSCC'14 [5]	JSSC'15 [3]	ISSCC'13 [4]	This work	VLSI'16 [2]
Architecture	Folding Flash	2b/cycle SAR	SAR	2xTI 1-2b SAR	4xTI SAR*
Technology	40nm	45nm	32nmSOI	28nm	16nm
Supply (V)	1.1	1.25	1.0	0.9	0.95
Resolution	7b	7b	8b	7b	10b
f_S (GS/s)	2.2	1.0	1.2	2.4	1.6
SNDR@Nyq(dB)	37.4	40.8	39.3	40.05	50.3
Input Cap. (F)	300f	600f	128f	64f	N/A
Power (mW)	27.4	7.2	3.06	5.0	8.2
FoM@Nyq. (fJ/conv.-step)	205.7	80	34	25.3	19.23
DNL/INL	0.6/0.6	0.4/0.5	0.79/0.91	0.49/0.57	0.62/0.81
Area (mm^2)	0.052	0.016	0.0015	0.0043	0.023
Offset Cal.	No need	Foreground	Background	Background	Background

*Need Timing-skew calibration (offchip)

Fig. 2. Benchmark and table of comparison with the state-of-the-art ADCs.

Publication(s):

[1] C.-H. Chan, Y. Zhu, I. M. Ho, W.H. Zhang, S. P. U, and R. P. Martins, "A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration" IEEE International Solid-State Circuits Conference (ISSCC), pp. 282-283, Feb 2017.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 7.8mW 5b 5GS/s Dual-Edges-Triggered Time-Based Flash ADC

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Partial Vcm-based switching
Low power and small common-mode variation
Offset calibration offchip
~48 fJ/conversion-step Walden FoM
Silicon verified in TSMC 65nm CMOS

DESCRIPTION

This paper proposes a 5b 5 GS/s time-based flash ADC in 65 nm digital CMOS technology which utilizes both rising and falling edges of the clock for sampling and quantization. A dual-edge-triggered scheme reduces the dynamic power consumption of a voltage-to-time converter and the clock buffers by half.

We doubled both the reset and the available regeneration times by interleaving the time comparators. The ADC has a low input capacitance and the calibration circuit is included on-chip for suppressing various mismatches. The prototype running at 5 GS/s consumes 7.8 mW from a 1 V supply and achieves a SNDR of 26.19 dB at Nyquist. The resulting FoM is 94.6 fJ/conversion-step and the core area is only 0.004 mm2.

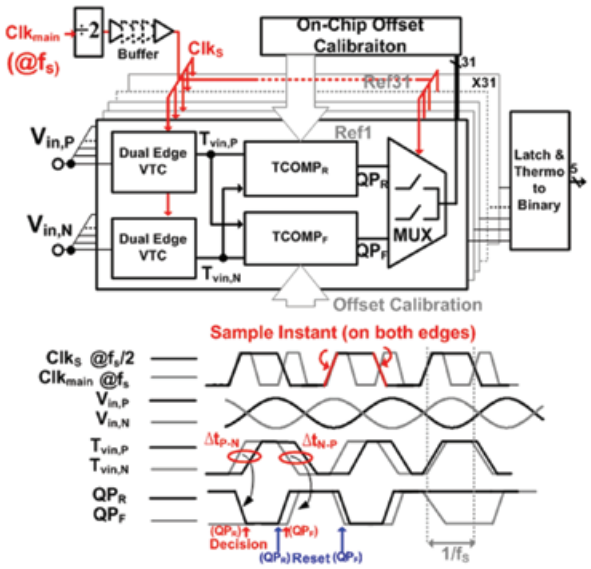


Fig. 1. Proposed ADC architecture and timing diagrams.

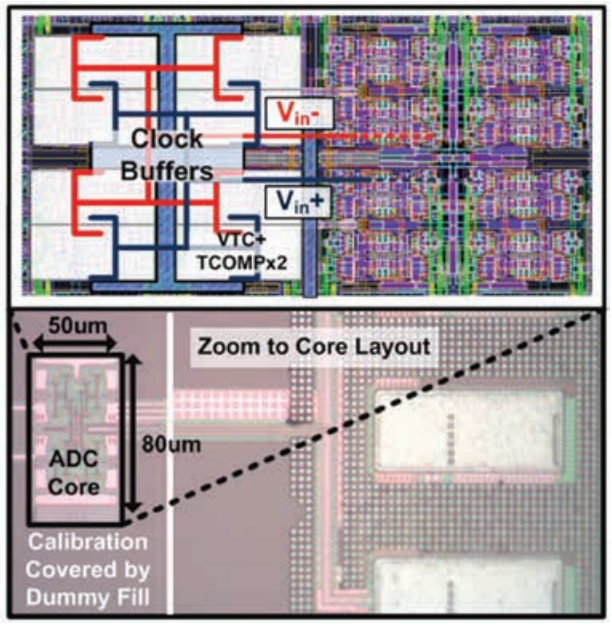


Fig. 2. Chip microphotograph and layout view.

Publication(s):

[1] C.-H. Chan*, Y. Zhu*, S.-W. Sin*, S. P. U*; R. P. Martins*, and F. Maloberti "A 7.8mW 5b 5GS/s Dual-Edges-Triggered Time-Based Flash ADC," IEEE Transactions on Circuits and Systems I: Regular paper, accepted, 2017.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Metastablility in SAR ADCs

Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Boris Murmann, Seng-Pan U, and Rui P. Martins

FEATURES

Analysis metastability in SAR
Quantified the metastability error
Measurement result verification
Silicon verified in ST 65nm CMOS

DESCRIPTION

The fundamental limitation of Nyquist ADC architectures towards high speed is metastability. It refers to the inability of a latched comparator to produce a valid decision in a certain available time. This issue is usually severe in high-speed Successive-Approximation-Register (SAR) ADCs due to their serial conversion scheme, which includes the regeneration and the reset process of the comparator in a feedback loop, thus significantly reducing the available time for the regeneration. As the metastability phenomenon has already been explored and analyzed in Flash and Pipeline architectures, a SAR ADC is studied here.

Our analysis considers the probability of metastability errors as a function of their magnitude and is customized for a timer-based asynchronous SAR ADC (with loop time-out). The resulting framework can also quantify the metastability in a synchronous architecture and we provide a numerical comparison. To validate the analysis, measurement results of an 8-bit 130 MS/s SAR ADC in 90 nm CMOS are provided.

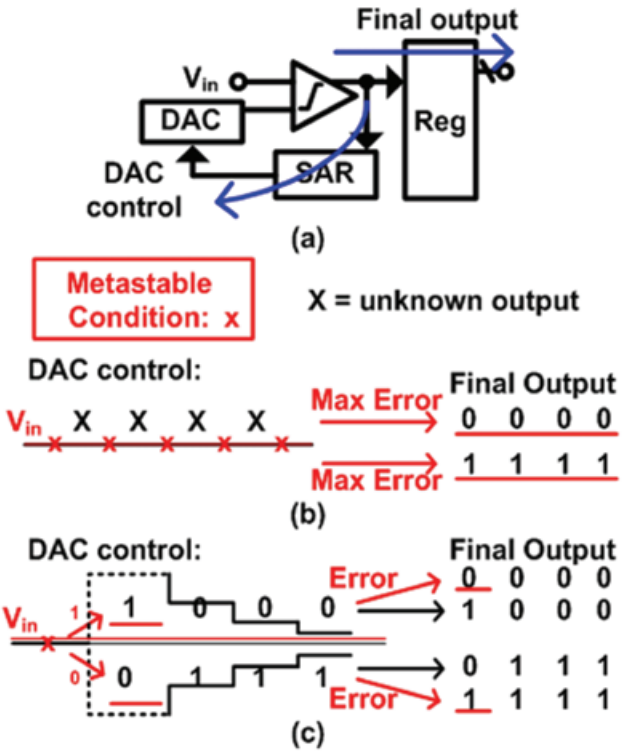


Fig. 1. (a) Conventional SAR block diagram (b,c) metastable error characteristics in the SAR ADC.

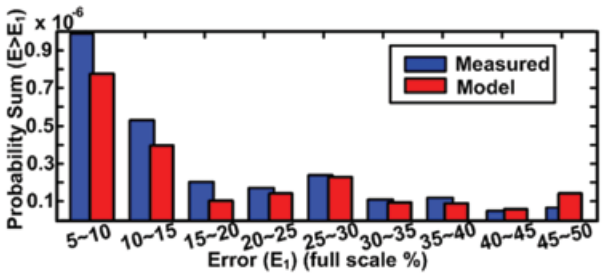


Fig. 2. Error rate versus error magnitude in histogram form with data grouped in 9 intervals.

Publication(s):

[1] C. H. Chan*, Y. Zhu*, S. W. Sin*, B. Murmann, S. P. U*, and R. P. Martins*, "Metastablility in SAR ADCs," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 2, pp. 111-115, Feb. 2017.

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Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau