RESEARCH ABSTRACTS
HIGH SPEED ADCs

A 7-bit 300-MS/s Subranging ADC with Embedded Threshold & Gain-Loss Calibration

U-Fat Chio, Chi-Hang Chan, Hou-Lon Choi, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Low Power Subranging ADC with
Reference Voltages Embedded
Reference Errors and
Subranging Gain Loss Calibrated
Low Power consumption 2.7mW
High Sampling Rate 300MS/s
7b Resolution, SNDR=39dB
Good Power efficiency, FoM_W=88fJ/step
Small Active Area, 0.1 mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work reports a 7-bit 300-MS/s subranging ADC fabricated in standard 65nm CMOS, which utilizes embedded reference and gain loss error calibration techniques. A shared passive capacitive DAC array performs the input sampling in quantization mode and reference generation in calibration mode, providing a linear, accurate and compact calibration implementation. The sign comparator with the threshold at mid-supply quantizes the B1 (MSB) which determines the connection of folding switches between the DAC and the 3-bit flash in the CADC. As a consequence of the developed calibration techniques, uniform-sized dynamic comparators are employed to reduce the process-mismatch variation and nonlinearity error, when compared with the conventional structures. The ADC achieves peak SNDR of 40.5dB at 300MS/s and 39dB at 400MS/s, with ERBW of 300MHz and 350MHz, respectively. The power consumption is 2.3mW only from 1.2-V supply at 300MS/s.

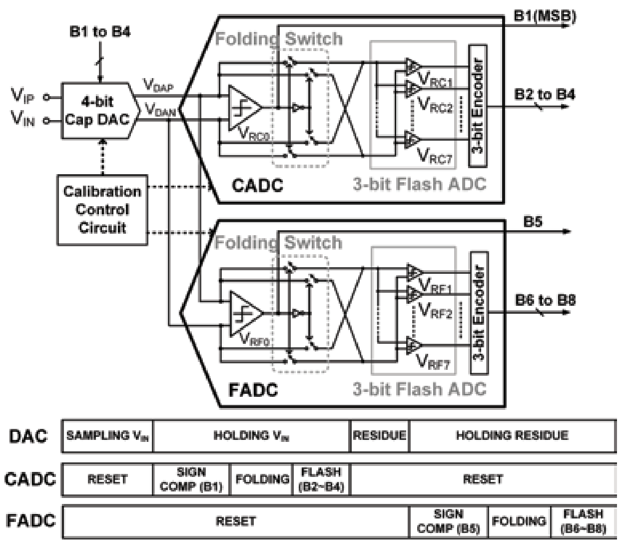

Fig. 1. Proposed ADC circuit diagram.

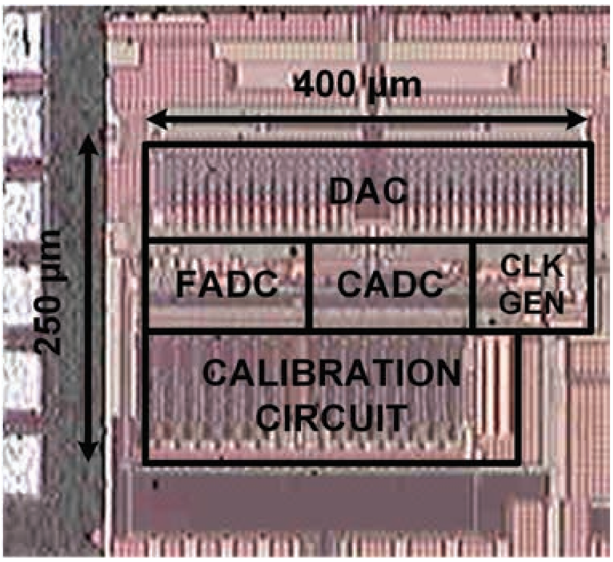

Fig. 2. Chip Photograph.

Publication(s):

[1] U-F. Chio, C.-H. Chan, H.-L. Choi, S.-W. Sin, S.-P. U, R. P. Martins, " A 7-bit 300-MS/s Subranging ADC with Embedded Threshold & Gain-Loss Calibration", in IEEE European Solid-State Circuits Conference – ESSCIRC, pp. 363-366, Sept 2011.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.024 mm² 4.9 fJ 10-bit 2 MS/s SAR ADC in 65 nm CMOS

Guohe Yin, He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Zhihua Wang, and Rui P. Martins

FEATURES

Extreme Low Power SAR ADC for Biomedical / Sensor Applications
Small Capacitor Array is utilized in MSB Conversion to Save Energy
Very Low Power consumption 6.6μW
Sampling Rate 2MS/s
Medium Resolution, SNDR=58.4dB
Excellent Power efficiency, FoM_W=4.9fJ/step
Very Small Active Area, $0.024mm^2$
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a Successive Approximation Register Analog-to-Digital (SAR ADC) design for sensor applications. In this proposed ADC architecture, the conversion does not start from the largest capacitor. An energy-saving switching technique, by utilizing small capacitor Array in MSB conversion first, is proposed to achieve ultra low power consumption. This switching technique is simple with two advantages in saving switching energy. First, the first-step conversion completes in the smaller capacitor instead of the larger capacitor; Second, if the first bit code is zero, there is no need to charge the large capacitor. Both of these can save significant power consumption. The measured signal-to-noise-and-distortion ratios (SNDR) of the ADC is 58.4 dB at 2 MS/s sampling rate with an ultra-low power consumption of only 6.6 μW from a 0.8V supply voltage, resulting in a figure of merit (FOM) of 4.9 fJ/conversion-step. The prototype is fabricated in 65 nm CMOS technology with area of 0.024 mm^2.

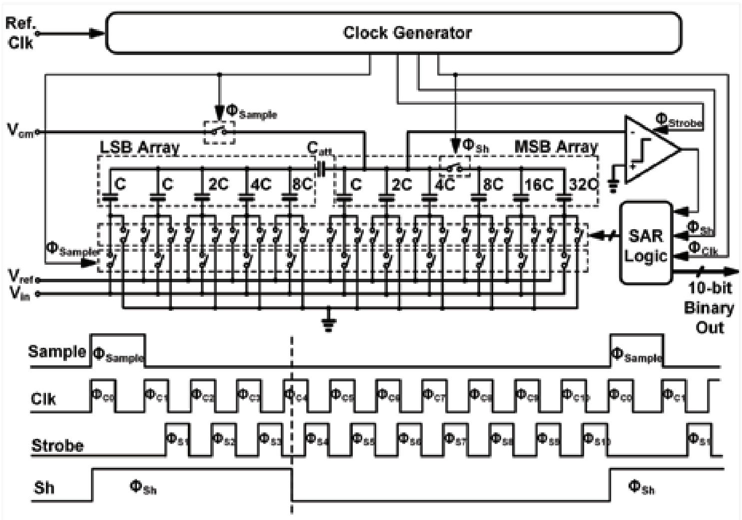

Fig. 1. Proposed ADC circuit diagram.

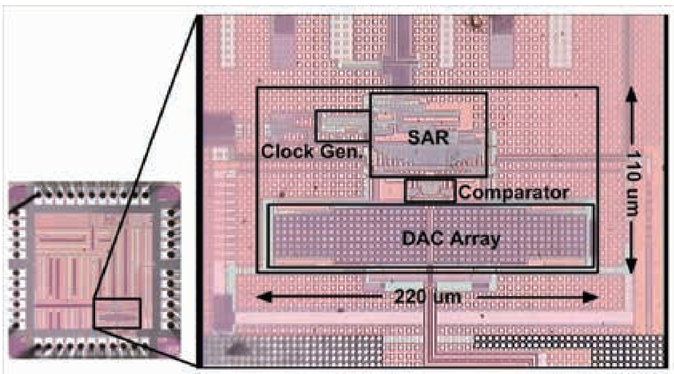

Fig. 2. Chip Photograph.

Publication(s):

[1] G. Yin*, H.-G. Wei*, U-F. Chio*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*,"A 0.024 mm2 4.9 fJ 10-bit 2 MS/s SAR ADC in 65 nm CMOS ", in IEEE European Solid-State Circuits Conference – ESSCIRC 2012, Sept. 2012.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 50-fJ 10-b 160-MS/s Pipelined-SAR ADC Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation

Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Shared Opamp in interleaved pipeline SAR ADC
Reused 1st Stage SAR DAC for flip around MDAC
Offset calibration onchip
~30 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a time-interleaved pipelined-SAR ADC with on-chip offset cancellation technique. The design reuses the SAR ADC to perform offset cancellation, thus saving calibration costs. The inter-stage gain of 8 is implemented in a 6-bit capacitive DAC with a flip-around operation. A capacitive attenuation used in both the first and second DACs significantly reduces the power dissipation and optimizes conversion speed. The detailed circuit implementation of the subthreshold op-amp is discussed, and the possible limits caused by nonidealities are analyzed for a proper correction in the design. These include the inter-stage-gain error and various channel mismatches of offset, gain, and timing. Measurements of a 65-nm CMOS prototype operating at 160 MS/s and 1.1-V supply show an SNDR of 55.4 dB and 2.72 mW total power consumption.

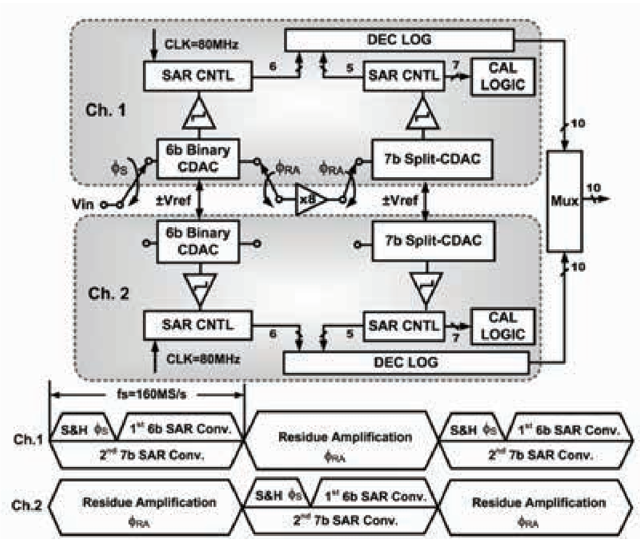

Fig. 1. Overall ADC architecture.

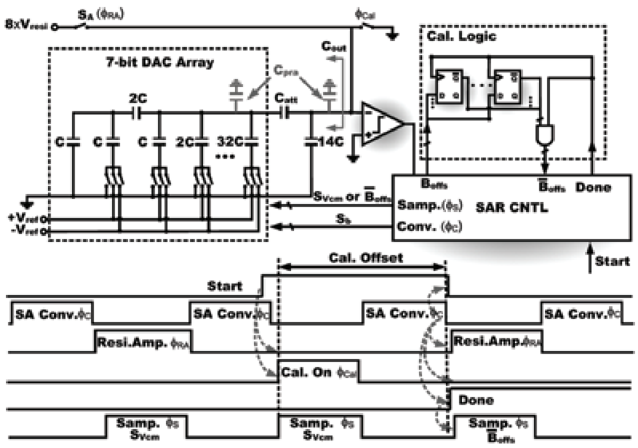

Fig. 2. Second-stage SAR ADC architecture and calibration timing diagram.

Publication(s):

[1] Y. Zhu*, C. H. Chan*, S. W. Sin*, S.-P. U*, R. P. Martins*, F. Maloberti, "A 50fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation", IEEE Journal of Solid-State Circuits, Dec. 2012.
[2] Y. Zhu*, C. H. Chan*, S. W. Sin*, S.-P. U*, R. P. Martins*, F. Maloberti, "A 35 fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation", in IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 61-64, Nov. 2011.
* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470Ms/s Pipelined-SAR ADC

Jianyu Zhong, Yan Zhu, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Inter-stage gain error calibration
Mapping table based calibration
Low completion time for calibration
~31 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper proposes an Inter-Stage Gain Error (ISGE) calibration method devoted to correct the residue gain errors induced by the parasitic effects, non-ideal op-amp gain and capacitor mismatch, and also the mismatched for supply-derived reference voltages between two stages for Pipelined-SAR ADC. The calibration reuses the SAR ADC to estimate the overall inter-stage gain error and compensates it in the 2nd-stage DAC in 2 cycles, and it is implemented in a Pipelined-SAR which achieves 10b 470MS/s in 65nm CMOS with the FoM of 31.5fJ/conv.-step by consuming only 6% of the total ADC area (0.049mm²).

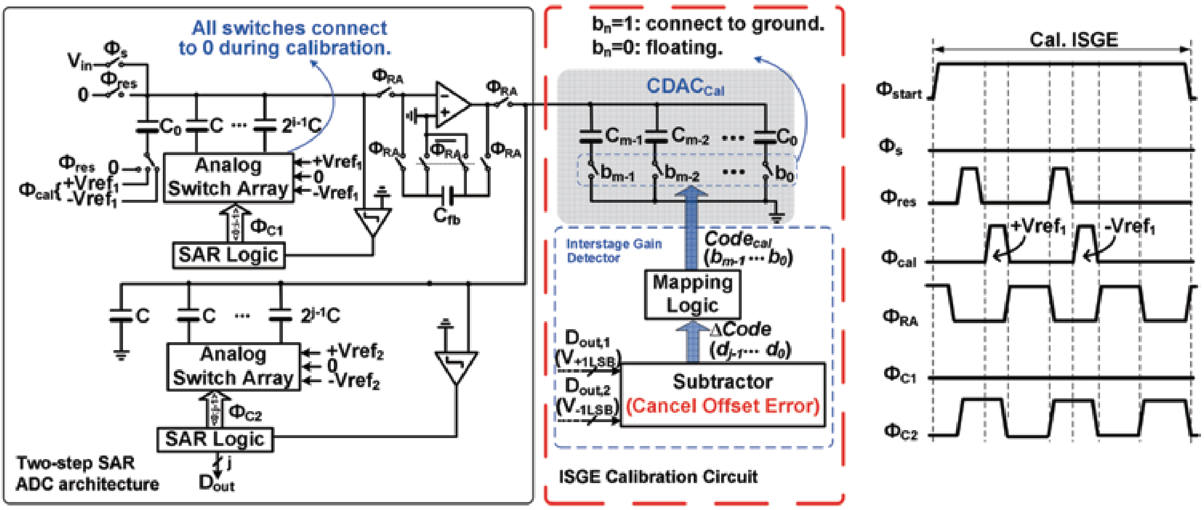

Fig. 1. Two-step SAR ADC with the ISGE calibration and timing diagram.

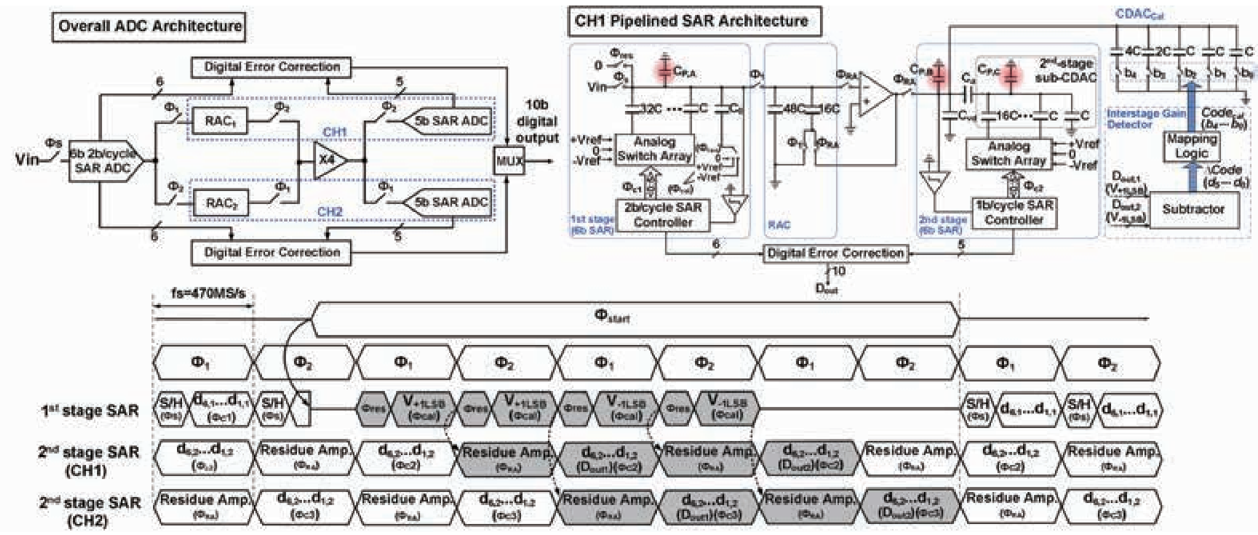

Fig. 2. PI Pipelined SAR ADC with the implementation of the ISGE calibration and timing diagram.

Publication(s):

[1] J. Zhong, Y. Zhu, S. W. Sin, S.-P. U, R. P. Martins, "Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470MS/s Pipelined-SAR ADC", IEEE Asian Solid-State Circuit Conference (A-SSCC), pp 153-156, Nov-2012.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC

Si-Seng Wong, U-Fat Chio, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Two-Step, Binary Search then Interleaved SAR
process insensitive asynchronous logic
Low power consumption, 2.3mW
Moderate Resolution, 10b
Excellent Power efficiency, 36.4fJ/step
Active Area, 0.1mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents the architecture of a 10b 170 MS/s two-step binary-search assisted time-interleaved SAR ADC, which takes the advantages of speed, resolution, and power offered by the two types of ADCs. The front-end stage of this ADC is built with a 5b binary-search ADC, which is shared by two time-interleaved 6b SAR ADCs in the 2nd-stage. The design does not use any static component such as op-amp or pre-amplifier that causes large dissipation of static power. DAC settling speed and power are also relaxed thanks to this architecture. Besides, the process insensitive asynchronous logic further reduces the delay of SA loop rather than using worst case delay cells to compensate the process variation problem. The ADC was fabricated in 65 nm CMOS and achieves 54.6 dB SNDR at 170 MS/s with only 2.3 mW of power consumption, leading to a FoM of 30.8 fJ/conversion-step.

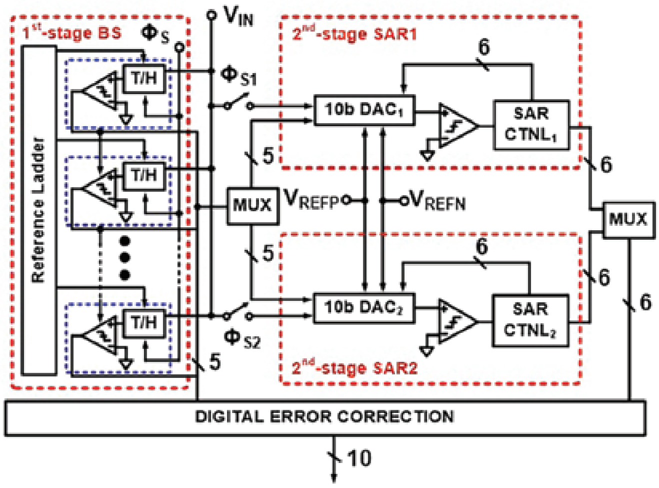

Fig. 1. ADC architecture.

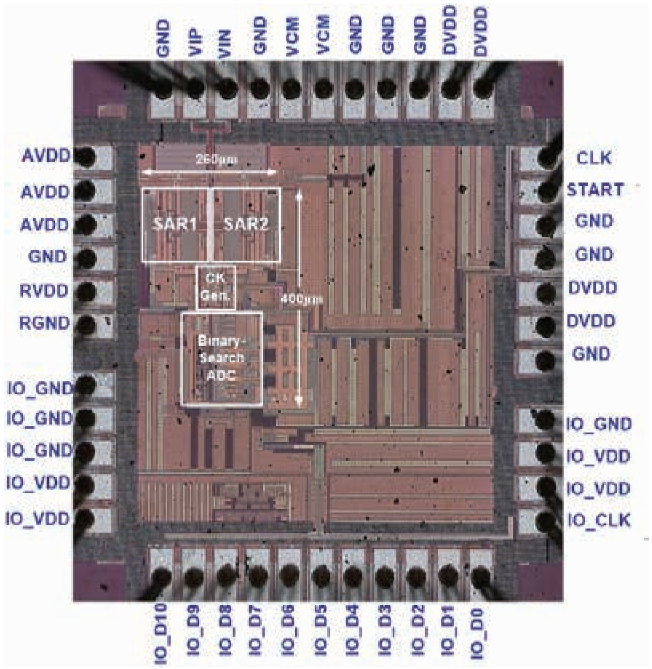

Fig. 2. Chip Photograph.

Publication(s):

[1] S.-S. Wong, U-F. Chio, Y. Zhu, S.-W. Sin, S.-P. U, R. P. Martins, "A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC", in IEEE Journal of Solid-State Circuits, vol. 48, Issue 8, pp. 1783-1794, Aug 2013.

[2] S.-S. Wong, U-F. Chio, Y. Zhu, S.-W. Sin, S.-P. U, R. P. Martins, "A 2.3mW 10-bit 170MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC," in Proc. of IEEE Custom Integrated Circuits Conference – CICC, Sept 2012.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Split-SAR ADCs: Improved Linearity With Power and Speed Optimization

Yan Zhu, Chi Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti

FEATURES

Switching techniques analysis
DNL and INL in SAR ADC
Switching energy in SAR ADC
Verified in UMC 90nm CMOS

DESCRIPTION

This paper presents the linearity analysis of a successive approximation registers (SAR) analog-to-digital converters (ADC) with split DAC structure based on two switching methods: conventional charge-redistribution and V_{cm}-based switching. The static linearity performance, namely the integral nonlinearity and differential nonlinearity, as well as the parasitic effects of the split DAC, are analyzed hereunder. In addition, a code-randomized calibration technique is proposed to correct the conversion nonlinearity in the conventional SAR ADC, which is verified by behavioral simulations, as well as measured results. Performances of both switching methods are demonstrated in 90 nm CMOS. Measurement results of power, speed, and linearity clearly show the benefits of using V_{cm}-based switching.

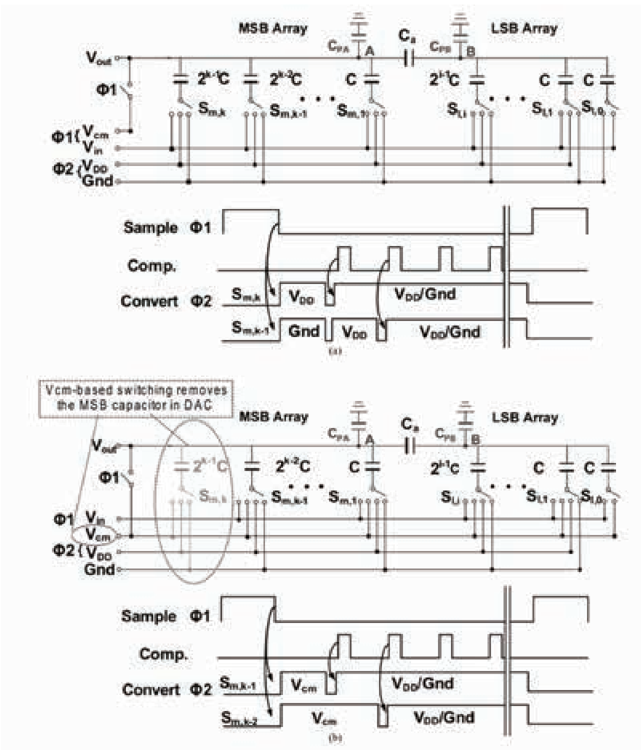

Fig. 1. Single-ended n-bit and (n − 1)-bit split capacitive DAC arrays with their switching timing diagrams (n = k + i). (a) Conventional switching. (b) V_{cm}-based switching.

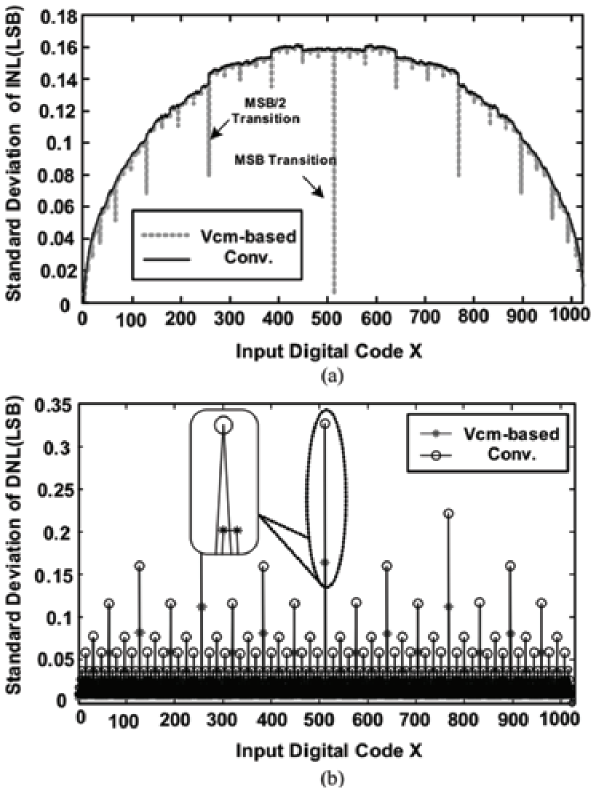

Fig. 2. Behavioral simulation comparing the DNL and INL of conventional and V_{cm}-based 10-b SAR ADCs.

Publication(s):

[1] Y. Zhu*, C. H. Chan*, U-F. Chio*, S. W. Sin*, S.-P. U*, R. P. Martins*, and F. Maloberti, "Split-SAR ADCs: Improved Linearity with Power and Speed Optimization," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Feb-2014.

* Contributors with University of Macau

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs

Jianyu Zhong, Yan Zhu, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Noise analysis in two architectures
Analyzed reference noise in SAR ADC
Provided design guideline for SAR and Pipeline SAR ADC
Simulation verified in ST 65nm CMOS

DESCRIPTION

This paper analyzes the thermal and reference noises of two types of successive-approximation-register (SAR) analog-to-digital converters (ADCs): the time-interleaving (TI) and the partial-interleaving (PI) Pipelined. The thermal noise is investigated with accurate estimation by deriving closed-form expressions according to the noise equivalent models on different phases. Additionally, the design trade-off between power and noise for two ADC architectures is discussed in detail. On the other hand, the reference noise due to the large switching transient, which significantly degrades the conversion accuracy, is analyzed and verified through behavioral and circuit level simulations of two ADC architectures operating at 500 MS/s for 10-bit resolution. The simulated results show the supremacy of the PI Pipelined-SAR (PS) architecture over the TI-SAR because it exhibits less reference noise sensitivity.

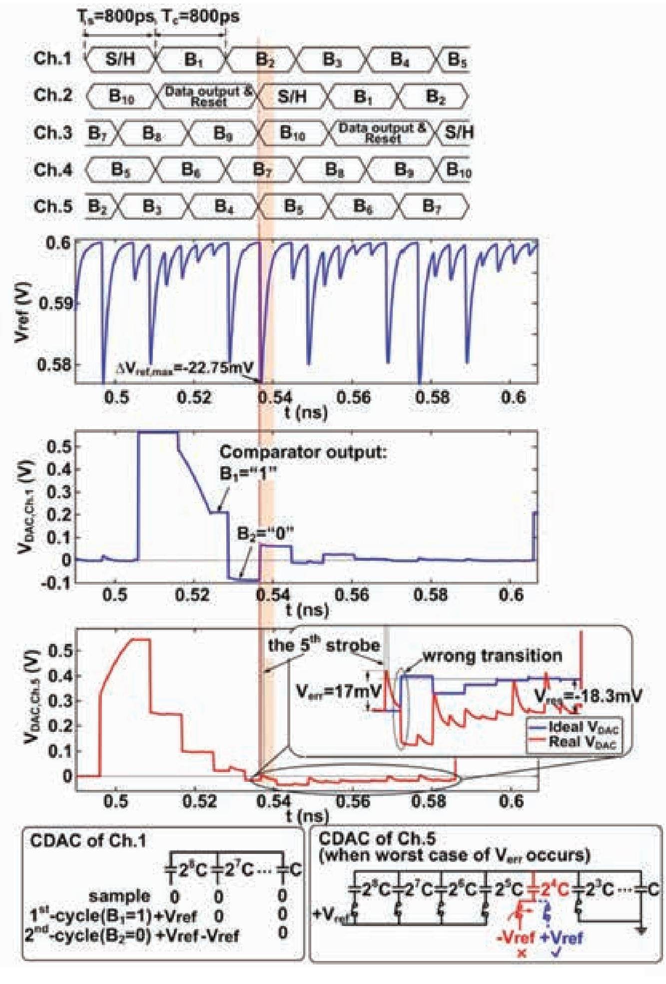

Fig. 1. The worst case of reference ripples in the TI-SAR ADC.

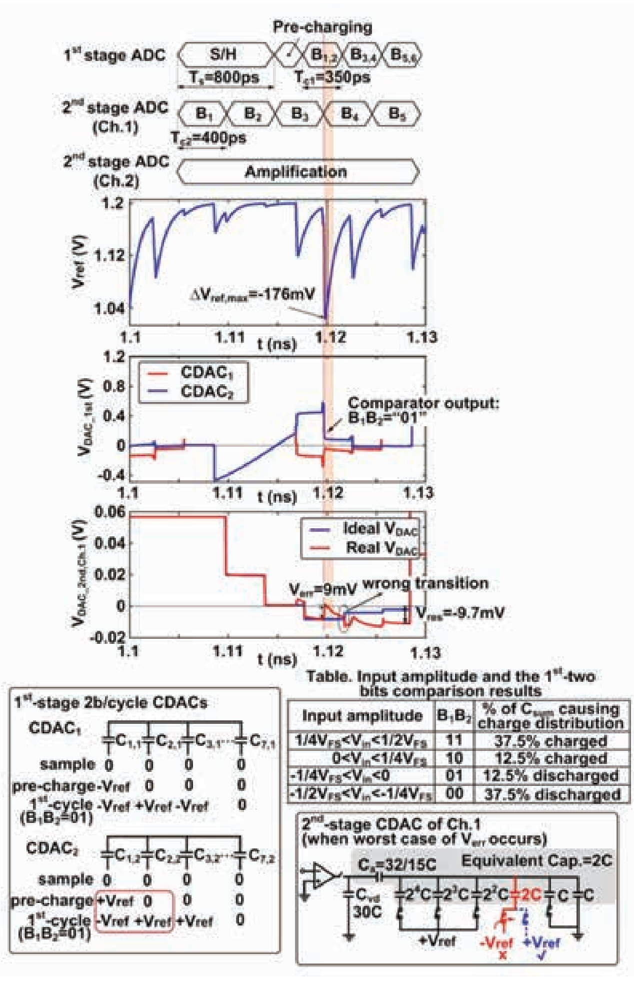

Fig. 2. The worst case of reference ripples in the PI PS ADC.

Publication(s):

[1] J. Zhong, Y. Zhu, S. W. Sin, S.-P. U, R. P. Martins, "Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs", IEEE Transactions on Circuits and Systems I: Regular Papers, Sep-2015.

Sponsorship:

Research Committee of the University of Macau, Macao Science and Technology Development Fund (FDCT)

Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC

Yan Zhu, Chi Hang Chan, S.-S. Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Gain error calibration
Histogram-based enhance accuracy
Verified with a SAR ADC design
~30 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This brief reports a 120 MS/s 12-bit successive approximation register analog-to-digital converter (ADC). The conversion nonlinearity in a bridge digital-to-analog converter is analyzed, and its corresponding histogram-based ratio mismatch (HBRM) calibration is presented in detail. Verified by behavioral simulations as well as measured results, the solution improves both the dynamic performance and the static performance of the ADC.

The measurement results demonstrate that the HBRM calibration effectively improves the signal-to-noise distortion ratio from 56.9 to 63.7 dB at dc input, with a sampling frequency of 120 MS/s.

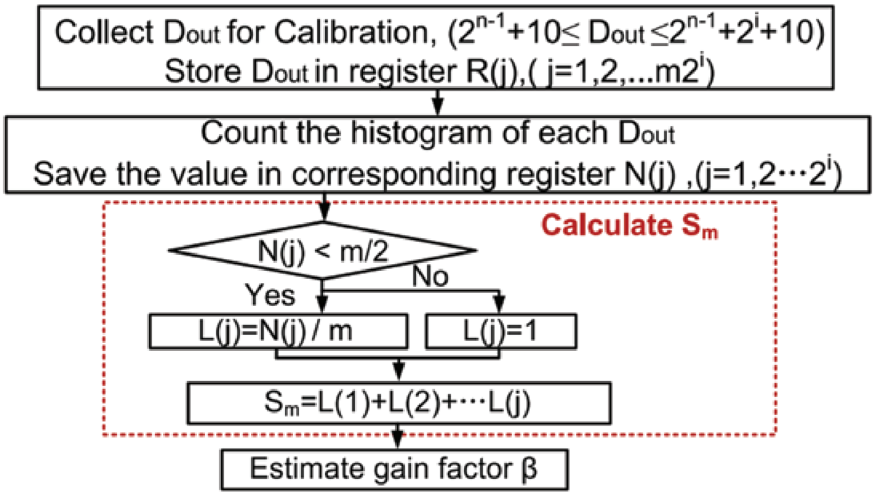

Fig. 1. Flowchart of the HBRM calibration.

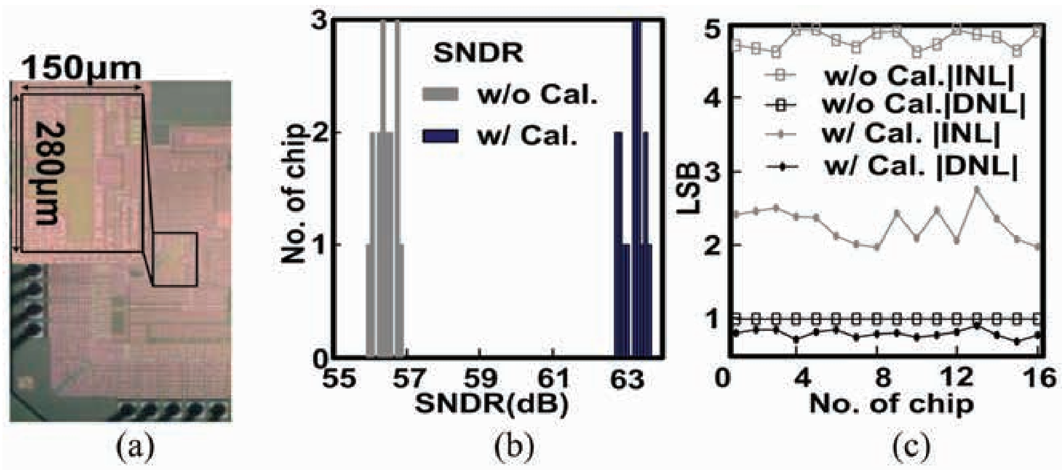

Fig. 2. (a) Chip photograph of SAR ADC. (b) Measured SNDR of total 16 chips. (c) Measured DNL and INL of total 16 chips.

Publication(s):

[1] Y. Zhu, C. H. Chan, S.-S. Wong, S.-P. U, R. P. Martins, "Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Jun-2015.

[2] Y. Zhu, C. H. Chan, S.-P. U, R. P. Martins, "A 10.4-ENOB 120MS/s SAR ADC with DAC Linearity Calibration in 90nm CMOS", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp 69-72, Nov-2013.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of the University of Macau

A 0.011mm² 60dB SNDR 100MS/s Reference Error Calibrated SAR ADC with 3pF Decoupling Capacitance for Reference Voltages

Chi-Hang Chan, Yan Zhu, Iok-Meng Ho, Wai-Hong Zhang, Chon-Lam Lio, Seng-Pan U, and Rui P. Martins

FEATURES

SAR reference error calibration
Low hardware overhead
~22 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a calibration scheme for reference error caused by signal dependent switching transient in a high speed SAR ADC. The scheme has a little hardware overhead, which is not dependent on the type of the input signal and is able to run in the background without interrupting the ADC's normal operation. The calibration along with the SAR ADC are implemented in a 65 nm CMOS and the measurement results show that the proposed scheme effectively improves the SNDR of an 11b SAR ADC by ~9 dB.

The calibration allows the placement of only 3 pF decoupling capacitance in the reference voltages. The prototype achieves 100 MS/s sampling rate with a total power consumption of 1.6 mW at a 1.2 V supply. Plus, it exhibits a 59.03 dB and 60.4 dB SNDR at Nyquist and low input frequency, respectively, yielding a Walden FoM@Nyquist of 21.9 fJ/conv.-step. The total core area is 0.011 mm2 which includes the decoupling capacitor.

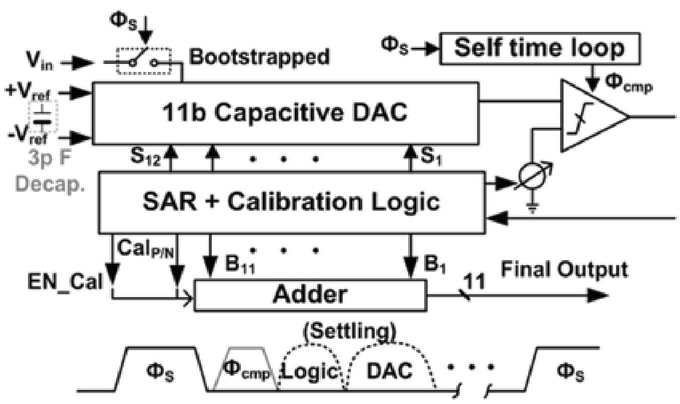

Fig. 1. ADC Architecture (actual implementation is in differential).

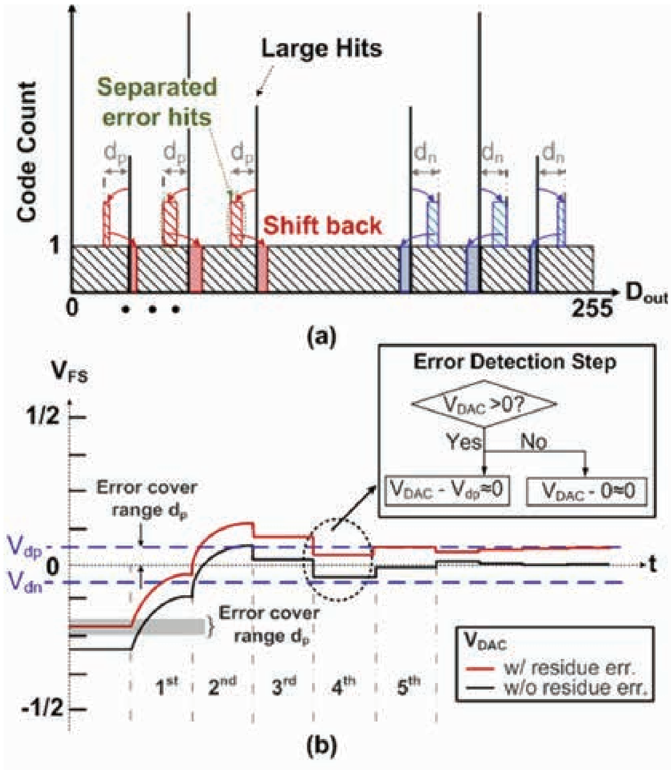

Fig. 2. (a) Code histogram of an 8b example with reference error. (b) Signal behavior of the DAC's output.

Publication(s):

[1] C.-H.g Chan, Y. Zhu, I.-M. Ho, W.i-H. Zhang, C.-L. Lio, S.-P. U, R. P. Martins, "0.011mm2 60dB SNDR 100MS/s Reference Error Calibrated SAR ADC with 3pF Decoupling Capacitance for Reference Voltages," in IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 145-148, Nov. 2016. Highlighted paper and invited to special issue of JSSC

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC

Jianwei Liu, Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Gain error calibration
Uniform Quantization based to simplified hardware
Calibration offchip
~30 fJ/conversion-step Walden FoM
Silicon verified in UMC 90nm CMOS

DESCRIPTION

This brief presents a uniform quantization theory (UQT)-based digital-to-analog converter (DAC) linearity calibration for a successive approximation register (SAR) analog-to-digital converter. According to the uniform quantization noise property, the nonlinearity due to the parasitics in an LSB array of the split-DAC structure is estimated and corrected in the digital domain. The calibration requires that the characteristic of the input signal must fulfill the prerogative of the quantization theory. The advantages lie in its low design complexity with no additional analog circuit modification. The proposed calibration is verified by both behavioral simulations and measured results in an SAR ADC. The measurements are based on a prototype implemented with large nonlinear split-DACs, which demonstrate that the UQT-base linearity calibration can effectively improve the Signal to Noise and Distortion (SNDR) from 56.9 to 63.3 dB at dc input with a sampling frequency of 120 MS/s.

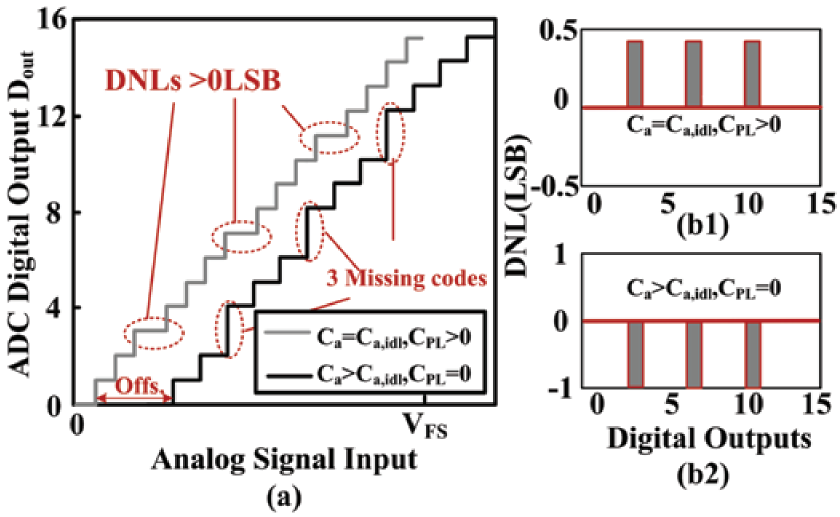

Fig. 1. (a) Output transfer characteristic of a 4-bit split-DAC. (b1) and (b2) Corresponding output code histogram of the 4-bit SAR ADC.

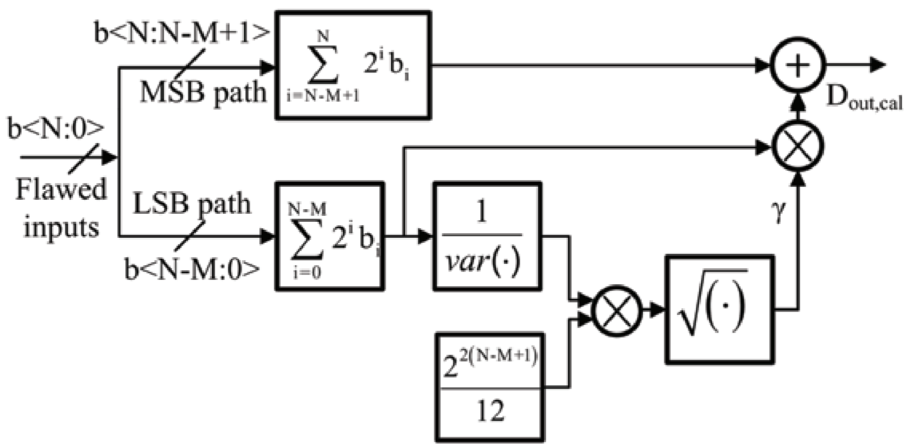

Fig. 2. Block diagram of the calibration based on UQT.

Publication(s):

[1] J. Liu, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Jan-2016.

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 12b 180MS/s 0.068mm² With Full-Calibration-Integrated Pipelined-SAR ADC

Jianyu Zhong, Yan Zhu, Chi Hang Chan, Sai Weng Sin, Seng-Pan U, and Rui P. Martins

FEATURES

Inter-stage gain calibration
Binary search calibration scheme to enhance completion time
Calibration on-cihp
Implement in a Pipeline SAR ADC
~37 fJ/conversion-step Walden FoM
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper presents a 12b 180 MS/s 0.068 mm² 2× time-interleaved pipelined-SAR analog-to-digital converter (ADC) with gain and offset calibrations fully embedded on-chip. The proposed binary-search gain calibration (BSGC) technique corrects the inter-stage gain error caused by the open-loop residue amplifier. The BSGC, fully integrated into the second-stage SAR ADC, contributes to a compact area. We improve the noise performance by implementing a merged-residue-DAC operation in the first-stage ADC.

Also, we propose a dual-phase bootstrap technique to improve the sampling linearity in the partial interleaving architecture. The measurement results of the ADC prototype in 65 nm CMOS demonstrate the effectiveness of the proposed calibration through the enhancement of the signal to noise-and-distortion ratio from 51.5 to 60.9 dB at a Nyquist input, leading to a FoM@Nyq of 36.7 fJ/conversion-step.

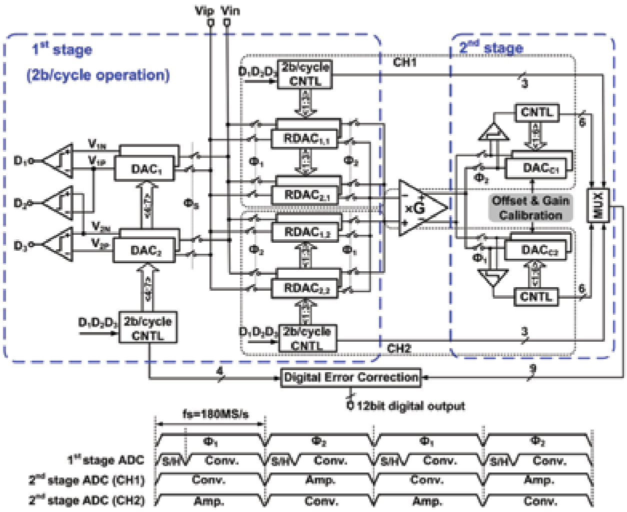

Fig. 1. PI Pipelined-SAR ADC architecture and timing diagram.

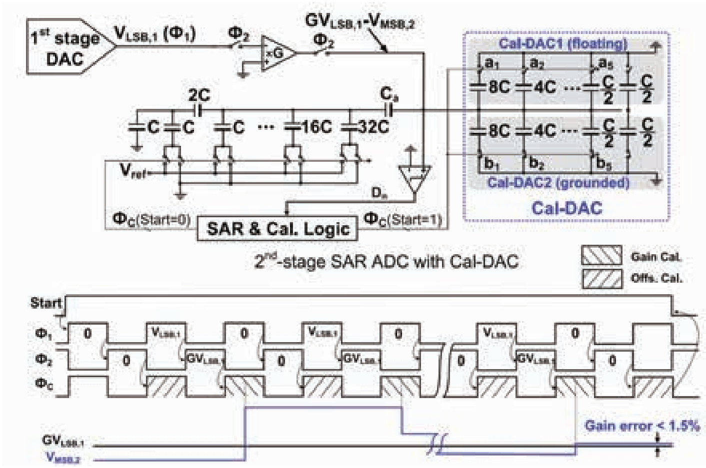

Fig. 2. Circuit implementation of the BSGC technique and its control timing diagram (Only Channel 1 shown).

Publication(s):

[1] J. Zhong, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 12b 180MS/s 0.068mm2 with Full-Calibration-Integrated Pipelined-SAR ADC", IEEE Transactions on Circuits and Systems I: Regular paper, Feb-2017

[2] J. Zhong, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 12b 180MS/s 0.068mm2 Pipelined-SAR ADC with Merged-residue DAC for Noise Reduction", IEEE European Solid-State Circuits Conference – ESSCIRC 2016, pp. 169-172, Sep-2016.

[3] J. Zhong, Y. Zhu, C. H. Chan, S. W. Sin, S.-P. U, R. P. Martins, "A 12b 180MS/s 0.068mm2 Full-Calibration Integrated Pipelined-SAR ADC", International Solid State Circuits Conference (ISSCC), Student Research Previews, Feb-2015

Sponsorship:

Macao Science and Technology Development Fund (FDCT), Research Committee of the University of Macau