RESEARCH ABSTRACTS
WIRELESS TRANSCEIVERS

A 53-to-75-mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS

Ka-Fai Un, Pui-In Mak, and Rui P. Martins

FEATURES

Two-stage 6-/14-path harmonic-rejection mixers
Low power consumption, 53 to 75 mW
Large bandwidth, 54 to 862 MHz
High harmonic rejection ratio, 59.3 dB
Low LO reference frequency, 432 to 864 MHz
Silicon verified in ST 65nm bulk CMOS

DESCRIPTION

A TV-band white-space transmitter covering a 16x-wide spectrum from 54 to 864 MHz is described.

It features a systematic co-design between the architecture and circuits to address the harmonic-mixing problem.

It incorporates two-stage 6-/14-path harmonic-rejection mixers and low-Q passive-RC/-CLC filters to manage the unwanted harmonic emission fully on chip.

It achieves an uncalibrated harmonic rejection ratio (HRR) of minimally 59.3 dB (16 samples) for all in-/out-band harmonics.

The employed 8-/16-phase LO generator is based on injection-locked 4-/8-phase correctors and even-ratio-only frequency dividers to save the LO-path power (2.5 to 14.2 mW) while lowering the required reference LO frequency (432 to 864 MHz).

Without any pre-distortion, the EVM tested under a 64-QAM OFDM digital-TV signal is 2.9% at 96 MHz, 3.3% at 384 MHz, and 4.0% at 600 MHz.

The first (second) adjacent channel leakage ratio is -46 dBc (-43 dBc) at 6 MHz (12 MHz) offset.

The power consumption is 53.1 to 75.2 mW and active area is 0.93 mm in 65-nm CMOS.

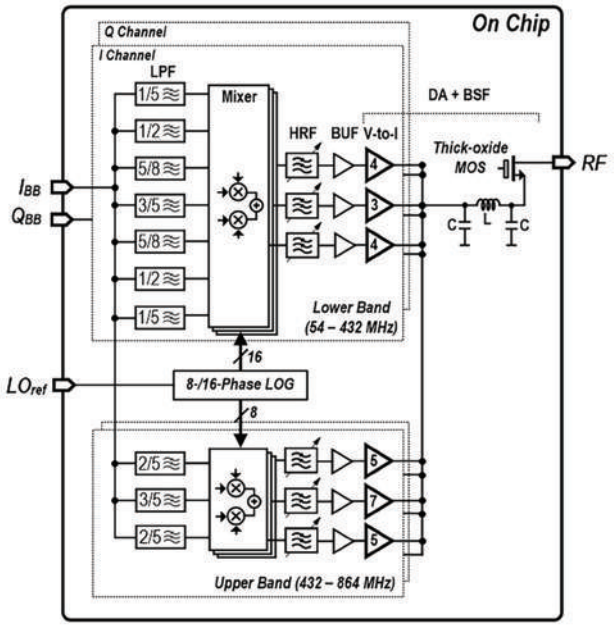

Fig. 1. Proposed TX with two-stage 6-/14-path harmonic rejection mixer.

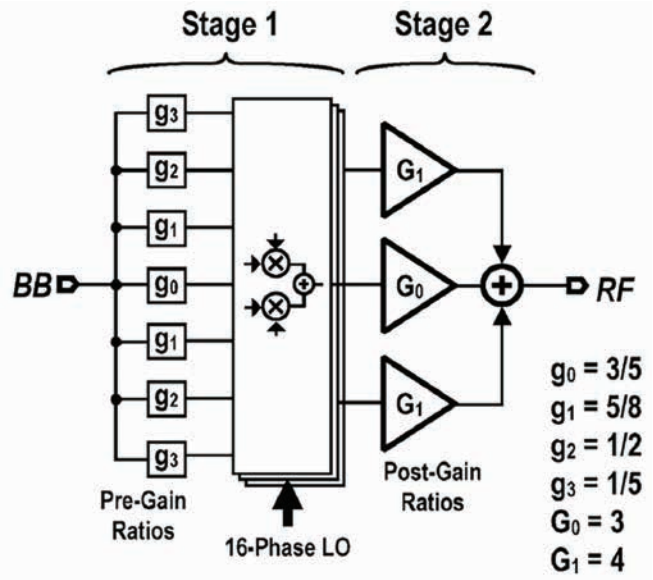

Fig. 2. Single-ended diagram two-stage 14P-HRM.

Publication(s):

[1] K.-F. Un, P.-I. Mak, and R. P. Martins, "A 53-to75-mW, 59.3-dB HRR, TV-Band White-Space Transmitter Using a Low-Frequency Reference LO in 65-nm CMOS," IEEE J. Solid-State Circ., vol. 48, no. 9, pp. 2078-2089, Sep. 2013.

Sponsorship:

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A 0.46-mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS

Pui-In Mak and Rui P. Martins

06

FEATURES

Full-band mobile TV (170 to 1700 MHz)
Low power consumption, 43 to 55 mW
Gain-boosting current-balancing Balun-LNA
Direct-injection-locked 4-/8-phase LO generator
Current-reuse mixer-lowpass filter
Silicon verified in ST 65 nm CMOS

DESCRIPTION

It is a unified receiver front-end (RFE) for full-band mobile TV covering the VHF-III (174 to 248 MHz), UHF (470 to 862 MHz) and L (1.4 to 1.7 GHz) bands, where standards like T-DMB, ISDB-T, DVB-H and DMB-T are resided. The performance, power and area efficiencies are advanced in threefold: 1) a gain-boosting current-balancing balun-LNA exhibits high linearity, wideband output balancing and adequate against gain control; 2) a current-reuse mixer-low-pass-filter merges quadrature-/harmonic-rejection mixing and 3rd-order current-mode post-filtering in one block, enhancing linearity and noise just where both are demanding, while saving power and area for its simplicity; 3) a direct injection-locked 4-/8-phase local oscillator (LO) generator relaxes the master LO frequency by avoiding frequency division.

Fabricated in 65-nm CMOS, the RFE measures 4-dB noise figure, 17-to-35-dB gain range, and 32/3.4-dBm IIP2/IIP3 with no tuning. The power consumption ranges from 43 mW (170 MHz) to 55 mW (1.7 GHz). The active area is 0.46 mm2 excluding the VCO. Dual 1.2/2.5-V supplies allow more functions to be realized in the current domain. Device reliability is ensured via a hybrid use of thin-oxide and thick-oxide MOSFETs and voltage-conscious biasing.

Benchmarking with the prior art, this work succeeds in extending the operating bandwidth and baseband selectivity with comparable power, while reducing the external parts, chip area and frequency of the LO that can ease the design of the PLL and VCO.

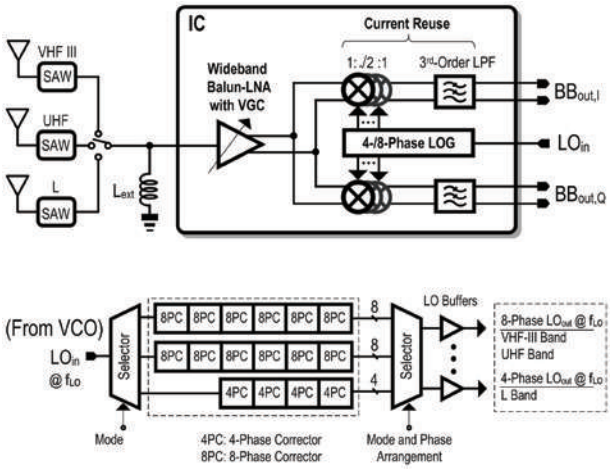

Fig. 1. (a) Receiver front-end (RFE) architecture and (b) detail of the LO generator.

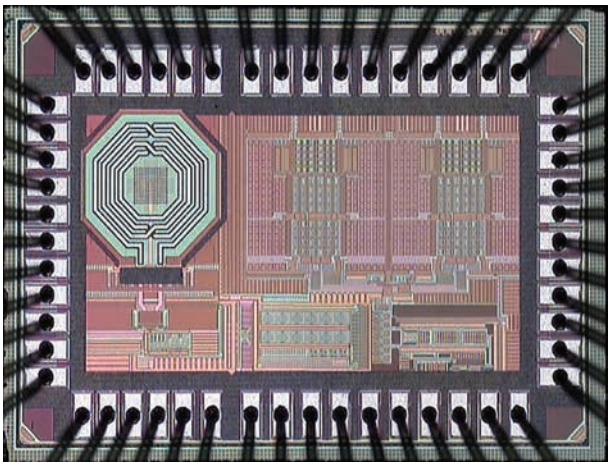

Fig. 2. Chip micrograph.

Publication(s):

[1] P.-I. Mak and R. P. Martins, "A 0.46-mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS," IEEE Journal of Solid-State Circuits, pp. 1970-1984, vol. 46, Sept. 2011.

[2] P.-I. Mak and R. P. Martins, "A 0.46mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), pp. 172-173, Feb. 2011.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Nonrecursive Digital Calibration Technique for Joint Elimination of Transceiver I/Q Imbalances With Minimized Add-On Hardware

Wei-Han Yu, Chak-Fong Cheang, Pui-In Mak, Weng-Fai Cheng, Ka-Fai Un, U-Wai Lok, and Rui P. Martins

08

FEATURES

A non-recursive local oscillator switching technique
Coordinate rotation digital computer algorithm
Improved TX's image rejection, from 27.8 to 37.2 dB
Improved RX's image rejection, from 31.2 to 42.0 dB
Algorithm verified on an FPGA

DESCRIPTION

A non-recursive digital calibration technique, namely, local oscillator (LO) switching, is proposed for jointly eliminating transmitter (TX) and receiver (RX) I/Q imbalances in one combined process.

The add-on analog parts are limited to a set of source followers (0.00228 mm^2) and metal–oxide–semiconductor (MOS) switches (0.00017 mm^2) for reusing the 90° phase shift property of the reference LO, avoiding the sinusoidal test tone, loop-back detector, high-speed analog-to-digital converter, and 2-D iterative search algorithm, mostly required in the prior art.

A 65-nm complementary MOS transceiver, which is co-designed with a field-programmable-gate-array-based coordinate rotation digital computer algorithm, measures a 10-dB improvement in the image rejection ratio of both the TX (27.8 → 37.2 dB) and the RX (31.2 → 42 dB).

The required digital circuitry for the algorithm is also assessed and simulated.

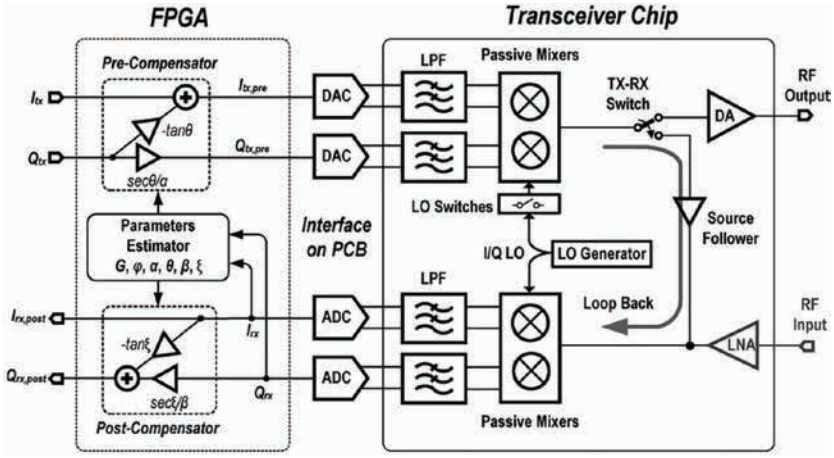

Fig. 1. CMOS TRX chip co-designed with an FPGA implementing the proposed calibration algorithm.

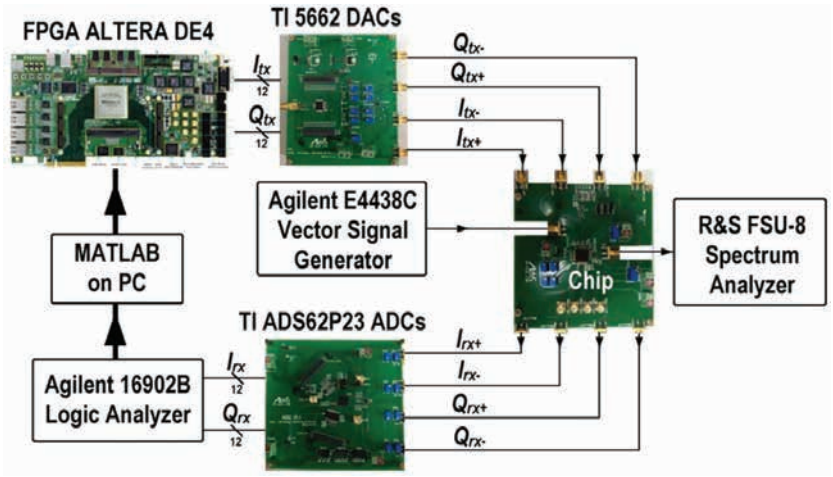

Fig. 2. Measurement setup.

Publication(s):

[1] W.-H. Yu, C.-F. Cheang, P.-I. Mak, W.-F. Cheng, K.-F. Un, U-W. Lok, and R. P. Martins, "A Nonrecursive Digital Calibration Technique for Joint Elimination of Transmitter and Receiver I/Q Imbalances with Minimized Add-On Hardware," IEEE Trans. Circuits Syst. II, Express Briefs, vol. 60, no. 8, pp. 462-466, Aug. 2013.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 2.4-GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65-nm CMOS

Zhicheng Lin, Pui-In Mak, and Rui P. Martins

FEATURES

On-chip input matching network + balun-LNA
Low power consumption, 1.7 mW
Wide S_{11} matching bandwidth, >1 GHz
Compact chip area, 0.24 mm^2
Silicon verified in ST 65 nm CMOS

DESCRIPTION

Ultra-low-power radios have essentially underpinned the development of short-range wireless technologies such as personal/body-area networks and Internet of Things. The main challenges faced by them are the stringent power and area budgets, and the pressure of minimum external components to save cost and system volume.

Ultra-low-voltage ultra-low-power radios are the most widespread design trend for ZigBee, Bluetooth and energy-harvesting applications. Yet, the lack of voltage head-room will limit the signal swing and transistor's f_T, imposing the need of bulky inductors/ transformers to facilitate the biasing and tune out the parasitics. Thus, the die area is easily penalized.

This work is a 2.4-GHz ZigBee receiver, unifying a balun-LNA-I/Q-mixer (Blixer) and a baseband (BB) hybrid filter in one cell, is fabricated in 65-nm CMOS. Without any external components, wideband input matching and passive pre-gain are concurrently achieved via co-optimizing an integrated low-Q network with a balun-LNA. The latter also features active-gain boosting and partial-noise canceling to enhance the gain and noise figure (NF). Above the balun-LNA are I/Q double-balanced mixers driven by a 4-phase 25% LO for downconversion and gain-phase balancing. The generated BB currents are immediately filtered by an IF-noise-shaping current-mode Biquad and a complex-pole load, offering 1st-order image rejection and 3rd-order channel selection directly atop the Blixer. Together with other BB and LO circuitries, the receiver measures 8.5-dB NF, 57-dB gain and –6-dBm $IIP3_{out\text{-}band}$ at 1.7-mW power and 0.24-mm^2 die size. The S_{11}-bandwidth (<–10 dB) covers 2.25 to 3.55 GHz being robust to packaging variations. Most performance metrics compare favorably with the state-of-the-art.

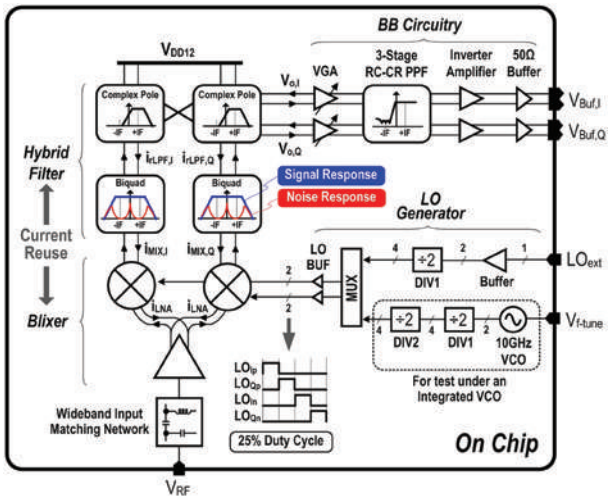

Fig. 1. Proposed 2.4-GHz RF-to-BB-current-reuse ultra-low-power receiver.

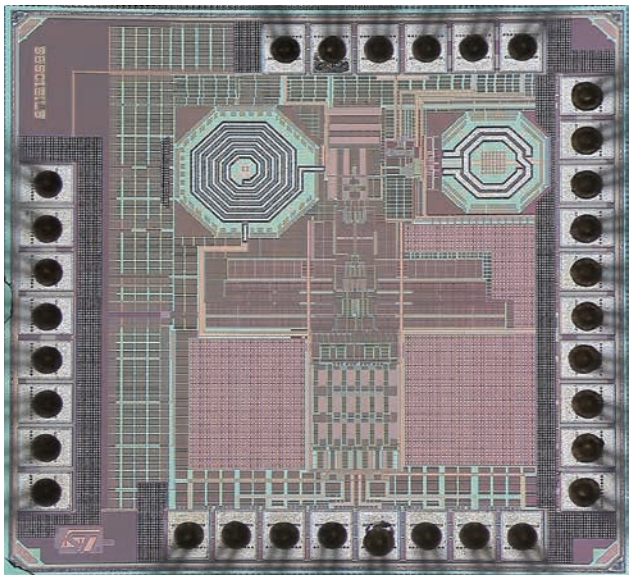

Fig. 2. Chip micrograph.

Publication(s):

[1] Z. Lin, P.-I. Mak and R. P. Martins, "A 2.4-GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65-nm CMOS," IEEE Journal of Solid-State Circuits, vol. 49, pp. 1333-1344, Jun. 2014.

[2] Z. Lin, P.-I. Mak and R. P. Martins, "A 1.7mW 0.22mm^2 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), pp. 448-449, Feb. 2013.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/ Passive Mixers and a Single-MOS Pole-Zero LPF

Fujian Lin, Pui-In Mak, and Rui P. Martins

FEATURES

Clock-rate-defined on-chip N-path bandpass filtering
Low power consumption, 16.2 mW at 0.85 GHz
High out-of-band linearity, IIP2=61 dBm, IIP3=17.4 dBm
Compact chip area, 0.55 mm^2
Silicon verified in ST 65 nm CMOS

DESCRIPTION

Frequency-flexible radios are low-cost platforms for multi-band multi-standard wireless communications. To minimize the number of SAW filters, wideband receivers mostly favor the N-path passive mixer for down-conversion, due to its high linearity and bidirec-tional response-translational property. Depending on the first baseband (BB) node of the receiver that can be a virtual ground or a lowpass-RC, the N-path passive mixer can be classified into current or voltage mode, respectively. For the former, the BB virtual ground is frequency-translated to RF, absorbing both the in-band signal and out-of-band interferers. As such, the signal amplification and channel selection can be delayed to BB. For the latter, the lowpass-RC at BB is shifted to RF, offering a tunable bandpass response to suppress the out-of-band interferers.

This work is an extensively-current-reuse wideband receiver exploiting parallel N-path active/passive mixers. The key features are: 1) a stacked RF-to-BB front-end with an 8-path active mixer realizing RF amplification, harmonic-recombination (HR) down-conversion and BB filtering in the current domain for better linearity and power efficiency; 2) a feedforward 8-path passive mixer enabling LO-defined input S_{11} matching without external components, while offering frequency-translated bandpass filtering and noise cancelling; 3) a single-MOS pole-zero lowpass filter (LPF) permitting both RF and BB filtering at low voltage headroom, while easing the tradeoff between the in-/out-of-band linearity, and 4) a BB-only two-stage HR amplifier boosting the harmonic rejection ratios ($HRR_{3,5}$). Measurements over 0.15 to 0.85 GHz manifest favorable NF (4.6 ± 0.9 dB) and out-of-band IIP2/IIP3 (+61/+17.4 dBm) at small power (10.6 to 16.2 mW) and area (0.55 mm^2). The HRR_{2-6} are >51 dB without any calibration or tuning. The out-of-band P_{-1dB} is >+2.5 dBm. The BB stopband rejection is >86 dB at 150-MHz offset.

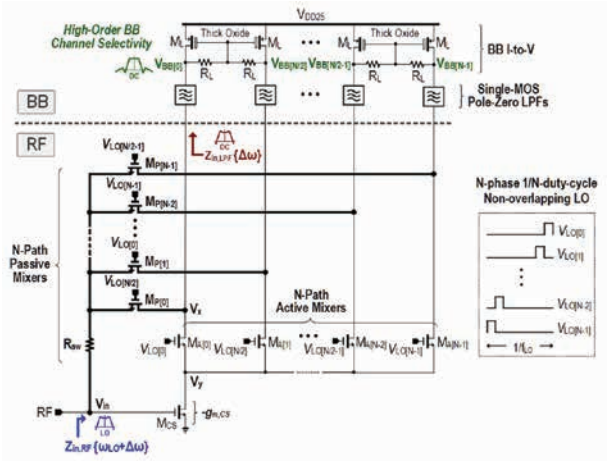

Fig. 1. Proposed RF-to-BB-current-reuse wideband receiver with the N-path filtering technique.

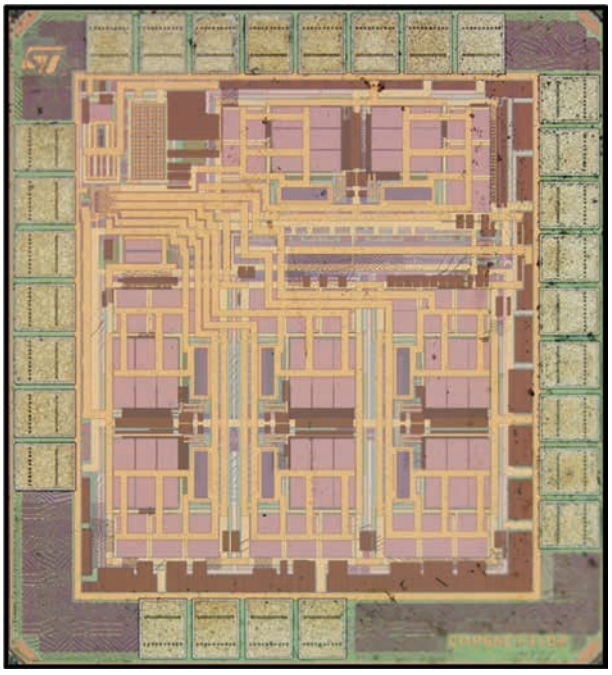

Fig. 2. Chip micrograph.

Publication(s):

[1] F. Lin, P.-I. Mak and R. P. Martins, "An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/ Passive Mixers and a Single-MOS Pole-Zero LPF," IEEE Journal of Solid-State Circuits, vol. 49, pp. 2547-2559, Nov. 2014.

[2] F. Lin, P.-I. Mak and R. P. Martins, "An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF," IEEE International Solid-State Circuits Conference (ISSCC), pp. 74-75, Feb. 2014.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications

Zhicheng Lin, Pui-In Mak, and Rui P. Martins

FEATURES

On-chip area-efficient N-path bandpass filtering
Ultra-Low power consumption, 1.15 mW
Multiple ISM bands (433/860/915/960 MHz)
Compact chip area, 0.2 mm^2
Silicon verified in ST 65 nm CMOS

DESCRIPTION

With the concept of Internet of Things (IoT), sub-GHz ULP wireless nodes compliant with the existing wireless standard such as the IEEE 802.15.4c/d (ZigBee) will be of great demand, especially for those that can cover all regional ISM bands [e.g., China (433 MHz), Europe (860 MHz), North America (915 MHz) and Japan (960 MHz)]. Together with the obvious goals of small chip area, minimum external components and ultra-low-voltage (ULV) supply (for possible energy harvesting), the design of such a receiver is quite challenging.

This work is a sub-GHz multi-ISM-band (433/860/915/960 MHz) ZigBee receiver. It features a gain-boosted N-path switched-capacitor (SC) network embedded into a function-reuse RF front-end, offering concurrent RF (common-mode) and BB (differential-mode) amplification, LO-defined RF filtering, and input impedance matching with zero external components. Interestingly, not only the BB power and area are nullified, but also the loading effect between the RF and BB blocks is averted, resulting in better noise figure (NF). Unlike the existing N-path filtering, the described gain-boosted topology offers: 1) double RF filtering at both input and output of the RF front-end; 2) size reduction of the physical capacitors thanks to the Miller multi-plication effect, and 3) LO-power saving by decoupling the mixer's on-resistance to the ultimate stopband rejection. Together with a low-voltage LC-VCO with extensively-distributed negative-gain cells for current-reuse with the BB filters, the receiver achieves 8.1 ± 0.6 dB NF, 50 ± 2 dB gain and –20.5 ± 1.5 dBm out-of-band IIP3 at 1.15 ± 0.05 mW power at 0.5 V over the four ISM bands.

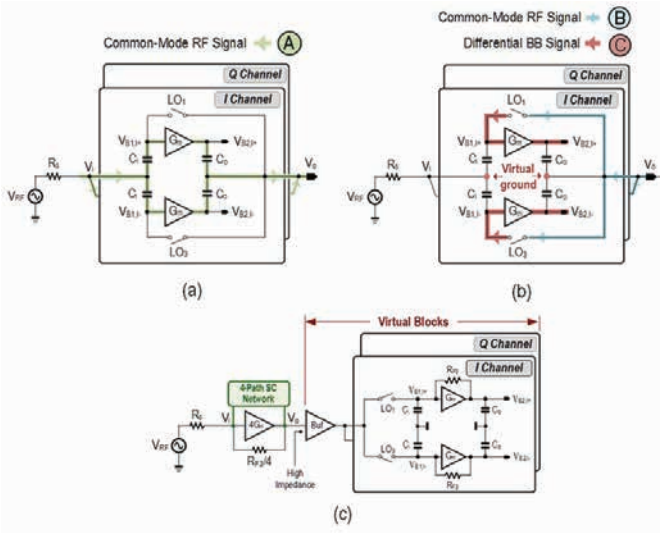

Fig. 1a-c Key idea of the proposed sub-GHz multi-ISM-band ZigBee receiver gain-boosted N-path filtering.

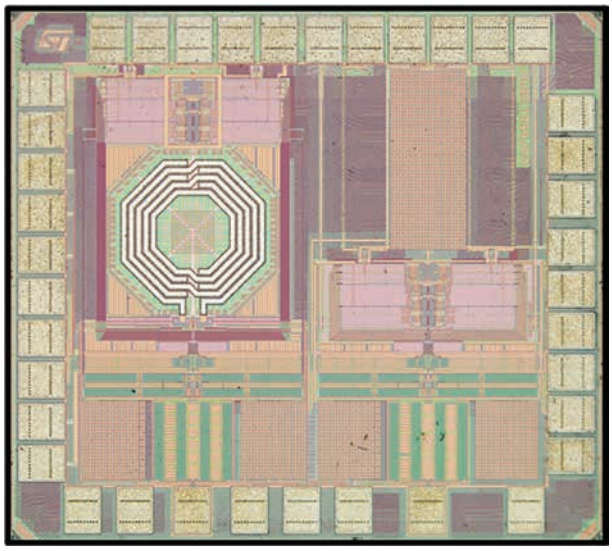

Fig. 2. Chip micrograph.

Publication(s):

[1] Z. Lin, P.-I. Mak and R. P. Martins, "A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications," IEEE Journal of Solid-State Circuits, vol. 49, pp. 2990-3004, Dec. 2014.

[2] Z. Lin, P.-I. Mak and R. P. Martins, "A 0.5V 1.15mW 0.2mm^2 Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components," IEEE International Solid-State Circuits Conference (ISSCC), pp. 164-165, Feb. 2014.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.02-mm² 59.2-dB SFDR 4th-Order SC LPF with 0.5-to-10 MHz Bandwidth Scalability Exploiting a Recycling SC-Buffer Biquad

Yaohua Zhao, Pui-In Mak, Rui P. Martins, and Franco Maloberti

FEATURES

High in-band IIP3, +17.6 dBm
High SFDR, 59.2 dB
Ultra-compact chip area, 0.02 mm²
Silicon verified in ST 65 nm CMOS

DESCRIPTION

In response to the ever-increasing demand for higher data rates, Long-Term Evolution (LTE) and Wireless Local-Area Network (WLAN) radios have introduced the carrier aggregation (CA) and multiple-input multiple-output (MIMO) techniques to enhance their throughput. The numerous channel-selection low-pass filters (LPFs) will occupy a significant chip area. For common LPF topologies like active-RC and gm-C that hinge on passives to define the time constant, the area can be relatively large because of bandwidth (BW) tuning and kT/C requirement. Also, to resist the process variations and allow BW scaling, spare capacitor banks are unavoidable. Although the recent ring-oscillator-based LPF has improved area and power efficiencies, the BW could only be tuned by the supply voltage. This undertaking couples the BW scalability with other performance metrics, while entailing a precision voltage regulator to avoid drifting of BW against PVT.

This work is a switched-capacitor (SC)-buffer Biquad that can be recycled efficiently as an ultra-compact LPF. It incorporates only passive-SC networks and open-loop unity-gain buffers; both are friendlier to technology downscaling than most conventional Biquads that use high-gain amplifiers and closed-loop negative feedback. Complex-pole pairs with independent Q factors are recursively realized in one clock period, while ensuring low crosstalk effect between the formations of each pole. Nonlinearity and parasitic effects are inherently low due to no internal gain.

The fabricated 65-nm CMOS 1x-recycling SC-buffer Biquad is equivalent to a 4th-order Butterworth LPF with 75% buffer utilization. It occupies a die size of only 0.02 mm² and exhibits 20x BW tunability (0.5 to 10 MHz), linear with the clock rate. At 10-MHz bandwidth, the in-band IIP3 is +17.6 dBm and input-referred noise is 19.5 nV/√Hz; they correspond to 59.2-dB SFDR and 0.013-fJ FoM that is favorably comparable with the recent art. The P_{1dB} conforms to the out-of-band blocker profile of the LTE standard at a 20-dB front-end gain.

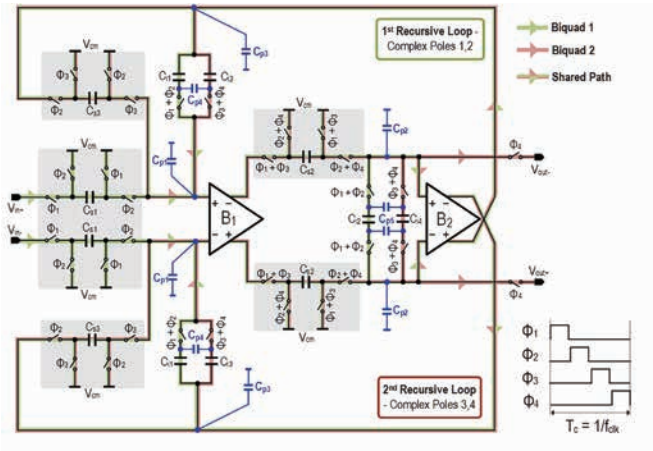

Fig. 1. 1x-recycling SC-buffer Biquad that is equivalent to a 4th-order Butterworth LPF.

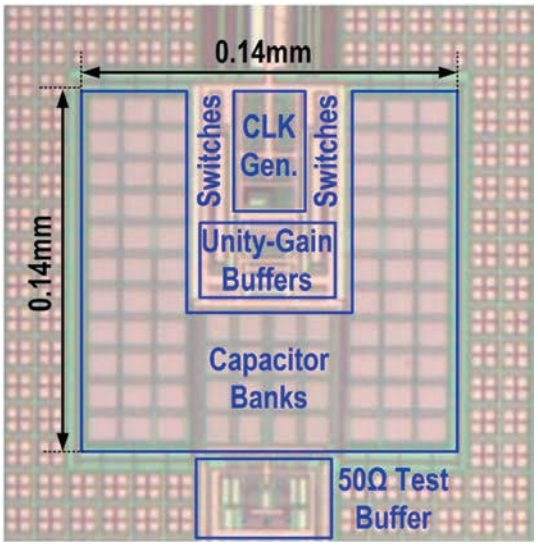

Fig. 2. Chip micrograph.

Publication(s):

[1] Y. Zhao, P.-I. Mak and R. P. Martins, and F. Maloberti, "A 0.02-mm² 59.2-dB SFDR 4th-Order SC LPF with 0.5-to-10 MHz Bandwidth Scalability Exploiting a Recycling SC-Buffer Biquad," IEEE Journal of Solid-State Circuits, vol. 50, pp. 1988-2001, Sep. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S_{11} Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF

Zhicheng Lin, Pui-In Mak, and Rui P. Martins

FEATURES

Low 0 dBm-blocker Noise Figure, 13.5 dB
Low power consumption, 11 mW
Wide RF coverage (0.1 to 1.5 GHz)
Ultra-compact chip area, 0.028 mm²
Silicon verified in ST 65 nm CMOS

DESCRIPTION

An RF-tunable blocker-tolerant receiver (RX) is desired to enhance the flexibility of multi-band multi-standard radios at low cost. The mixer-first RX delays the signal amplification to baseband (BB) by frequency-translating the BB lowpass response to RF as bandpass. This aim raises the out-of-band (OB) IIP3 at the expense of NF and power due to no RF gain. The noise-cancellation RX breaks such a tradeoff via paralleling a voltage-sensing RX with the mixer-first. This undertaking confers a better pair of NF and OB-IIP3, but sacrificing more die size and power to accommodate the doubled RF and BB circuitries. Although there is N-path RF filtering that can be combined with noise cancellation to save the die area and power consumption while offering a high OB-IIP3, a high supply voltage is required to widen the voltage headroom.

This work is a single-mixing blocker-tolerant RX using a gain-boosted-mixer-first topology. Two unexplored features: indirect BB amplification and double-RF N-path filtering improve the NF (1.5 to 2.9 dB) and OB-IIP3 (13 dBm) over a wide range of RF (0.1 to 1.5 GHz), while squeezing the power (11 mW) and area (0.028 mm²) with zero external components. The RX also originates partial-inductive input impedance to self-cancel the frequency shift of S_{11} bandwidth, which is a typical inadequacy of mixer-first RX demanding input-impedance tuning.

Thanks to the double-RF N-path filtering with narrow –3-dB bandwidth, the OB-IIP3 rapidly reaches 10 dBm at 30 MHz offset. The RF-to-IF gain is 38 dB, and drops by 1 dB with a –6 dBm blocker power at 80MHz offset, consistent with the 5.8 dB BB gain measured at that frequency offset. With a 0 dBm blocker, the 10 dB gain compression is due to the saturation of the BB amplifiers. The –3-dB BW at BB is ~2 MHz. With a single-tone blocker injected at 80MHz offset, the 0 dBm-blocker NF is 13.5 dB. Benchmarking with the recent art, this work succeeds in squeezing the power and area without penalizing the NF and OB-IIP3.

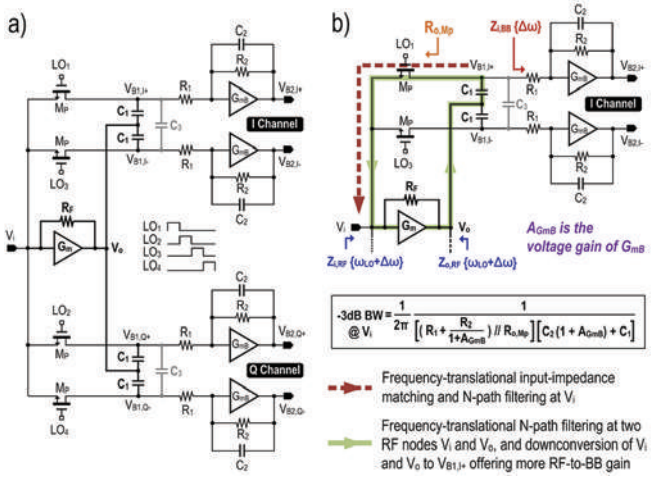

Fig. 1. Key idea of the proposed single-mixing blocker-tolerant receiver.

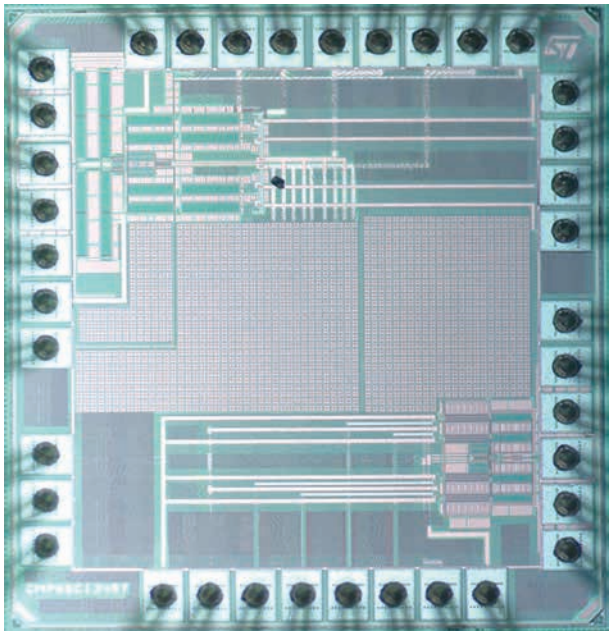

Fig. 2. Chip micrograph.

Publication(s):

[1] Z. Lin, P.-I. Mak and R. P. Martins, "A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S11 Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF," IEEE International Solid-State Circuits Conference (ISSCC), pp. 36-37, Feb. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.07 mm² 2.2 mW 10 GHz Current-Reuse Class-B/C Hybrid VCO Achieving 196-dBc/Hz FoM_A

Md. Tawfiq Amin, Jun Yin, Pui-In Mak, and Rui P. Martins

FEATURES

Low power, 2.2mW
Small area, 0.77 mm²

DESCRIPTION

This work is a current-reuse class-B/C hybrid voltage-controlled oscillator (VCO) with robust startup, enhanced phase noise and differential balancing at small area and power. Specifically, an asymmetrical CMOS class-C core is aided by a symmetrical NMOS-only class-B core that effectively shares the bias current for deeper class-C operation of the former; wider margin of startup against PVT variations, and lower amplitude imbalance against oscillation frequencies. Moreover, this topology adds the freedom of adjustable peak dynamic current and boosts the oscillation swing at low power. The spiral inductors with patterned ground shields shrink the die size. Fabricated in 65 nm CMOS, the 0.07 mm² VCO prototype exhibits 10.15-to-11.17 GHz tunability, and -107.7dBc/Hz phase noise at 1 MHz offset, while dissipating merely 2.2 mW at 1.2 V. The achieved area-included figure-of-merit (FoM_A = 196 dBc/Hz) favorably compares with the state-of-the-art.

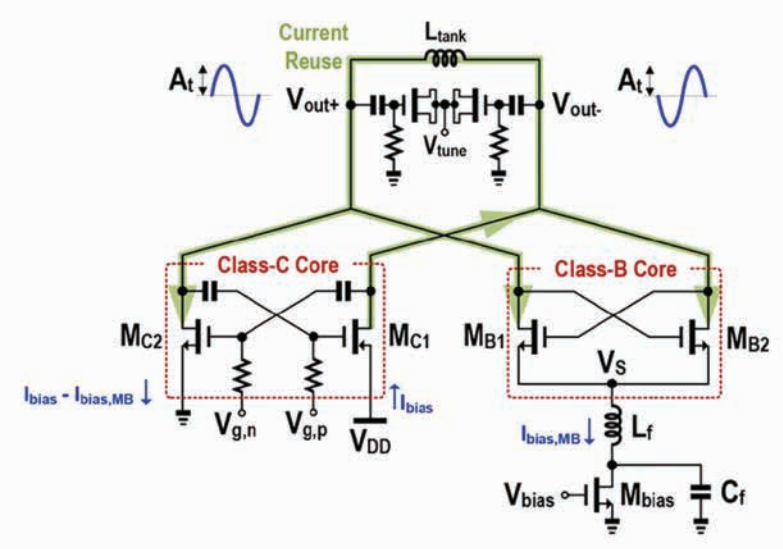

Fig. 1. Schematic of the proposed current-reuse class-B/C hybrid VCO.

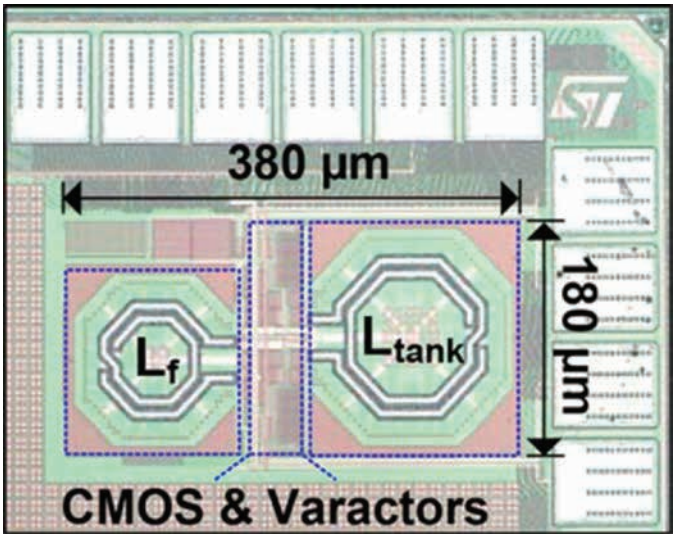

Fig. 2. Chip photo of the proposed VCO fabricated in 65 nm CMOS.

Publication(s):

[1] M. T. Amin, J. Yin, P.-I. Mak, and R. P. Martins, "A 0.07 mm² 2.2 mW 10 GHz Current-Reuse Class-B/C Hybrid VCO Achieving 196-dBc/Hz FoM_A," IEEE Microwave and Wireless Components Letters (MWCL), vol. 25, no. 7, pp. 457-459, Jul. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Sub-GHz Wireless Transmitter Utilizing a Multi-Class-Linearized PA and Wideband-Auto I/Q-LOFT Calibration for IEEE 802.11af WLAN

Ka-Fai Un, Wei-Han Yu, Chak-Fong Cheang, Gengzhen Qi, Pui-In Mak, Rui P. Martins

FEATURES

Multi-class-linearized PA
Time-domain auto I/Q-LOFT calibration
Large bandwidth, 54 to 600 MHz
High harmonic rejection ratio, 59.8 dB
High system efficiency, 7.4 to 18.5%
Low harmonics, -41 dBc
Silicon verified in ST 65nm bulk CMOS

DESCRIPTION

This work describes a sub-GHz wireless transmitter (TX) with an integrated multi-class-linearized power amplifier (PA) compliant with the IEEE 802.11af wireless local-area network.

It features a wideband in-phase/quadrature (I/Q) modulator exploiting two-stage 6-/14-path harmonic-rejection mixers plus G_m-C low-pass filters to manage the spurs emission induced by hard-switched mixing.

The entailed 8/16-phase local oscillator (LO) is generated by injection-locked phase correctors plus frequency dividers to relax the frequency and tuning range of the reference LO.

The linearized PA features overdriven-class-A/B/C cells to balance the power efficiency and linearity.

A dual-gate input pair enlarges the linear gain range.

A wideband low-impedance ground at the second harmonic suppresses the harmonic distortion and ground bounces.

The wideband I/Q imbalance and LO feedthrough are resolved by automatic digital calibration, which incorporates time-domain parameter estimation for better computational efficiency.

Benchmarking with the recent art, this solution fabricated in 65-nm CMOS exhibits higher system power efficiency (from 7.4% to 18.5%) and 1-dB compression point (from 12.5 to 16.3 dBm).

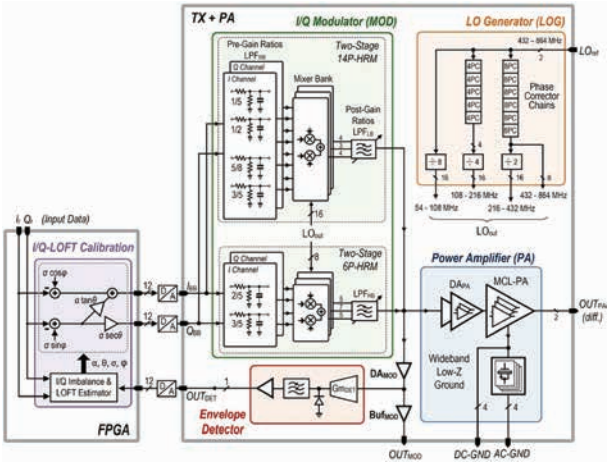

Fig. 1. Proposed wideband TX+PA with automatic I/Q-LOFT calibration in a closed-loop form.

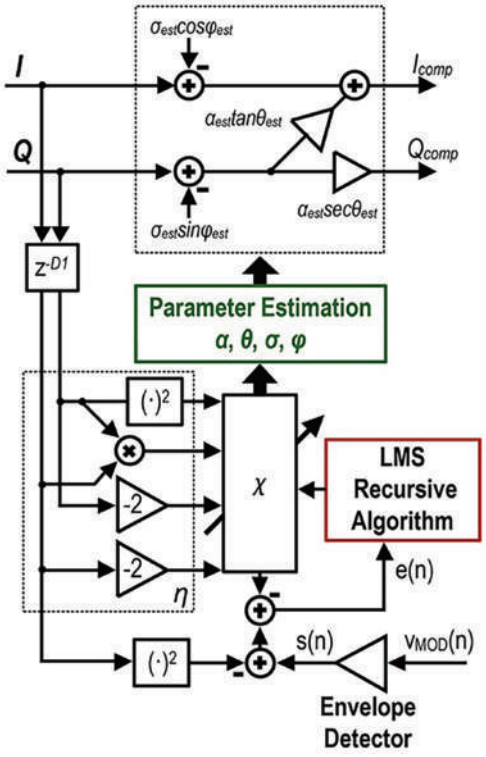

Fig. 2. Block diagram of the digital I/Q-LOFT calibration.

Publication(s):

[1] K.-F. Un, W.-H. Yu, C.-F. Cheang, G. Qi, P.-I. Mak, and R.P. Martins, "A Sub-GHz Wireless Transmitter Utilizing a Multi-Class-Linearized PA and Time-Domain Wideband-Auto I/Q-LOFT Calibration for IEEE 802.11af WLAN," IEEE Trans. Microw. Theory Techn., vol. 63, no. 10, pp. 3228-3241, Oct. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Combinatorial Impairment-Compensation Digital Predistorter for a IEEE 802.11af-WLAN CMOS Transmitter Covering a 10x-Wide Bandwidth

Chak-Fong Cheang, Ka-Fai Un, Wei-Han Yu, Pui-In Mak, and Rui P. Martins

FEATURES

A modified dynamic deviation reduction-based Volterra series digital predistorter
Fulfill the IEEE 802.11af standard
Large bandwidth, 54 to 600 MHz
Improved EVM, from 8.1% to 2.8%
Improved ACLR, 10 dB
Algorithm verified on a ST 65-nm CMOS TX prototype

DESCRIPTION

A new combinatorial impairment-compensation digital predistorter (DPD) for a sub-GHz IEEE 802.11af-WLAN CMOS transmitter (TX) is proposed.

For the TX to cover a 10x-wide bandwidth, the DPD implements a modified dynamic deviation reduction (DDR)-based Volterra series to jointly nullify the frequency-dependent I/Q imbalance, counter-inter-modulation (CIM) of mixers, and nonlinearities of power amplifier (PA) with memory effect.

The interactions of those impairments are firstly analyzed using two Volterra series. After applying the tandem properties of Volterra series, interactions of all impairments can be described in one Volterra series by bonding those impairments in parallel.

Coefficients of the DPD are extracted with the Least-Square (LS) estimator, achieving lower running complexity than the existing DPDs, which were developed to handle the PA nonlinearities only.

Verifications are based on both system-level simulations and silicon measurements of a 65-nm CMOS TX prototype. When the TX delivers a 6-MHz bandwidth, 2048-point, 64-QAM OFDM signal at 10 dBm output power, the measured EVM is <3.7% and adjacent channel leakage ratio (ACLR) is <-40.2 dBc under individual DPD applied at each RF.

A novel one-shot calibration for reuse in the entire TV-band is demonstrated also, showing EVM <4.2% and ACLR <-39.8 dBc.

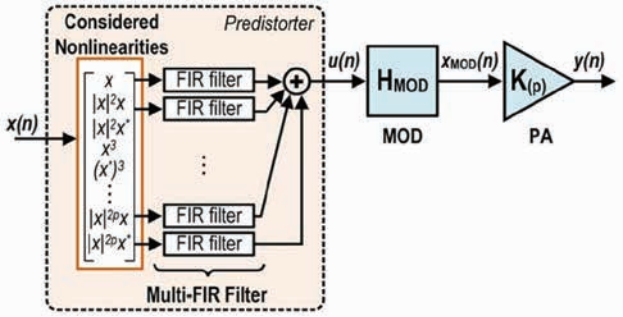

Fig. 1. Block schematic of the DPD addressing both CIM, I/Q imbalance, and RF nonlinearities.

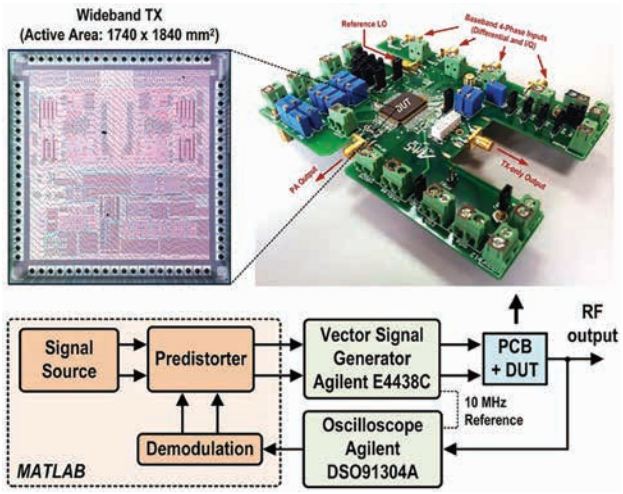

Fig. 2. Measurement setup. The DUT is a wideband TX fabricated in a 65-nm CMOS technology.

Publication(s):

[1] C.-F. Cheang, K.-F. Un, W.-H. Yu, P.-I. Mak, and R. P. Martins, "A Combinatorial Impairment-Compensation Digital Predistorter for a Sub-GHz IEEE 802.11af- WLAN CMOS Transmitter Covering a 10x-Wide RF Bandwidth," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 4, pp. 1025-1032, Apr. 2015.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Time-Interleaved Ring-VCO with Reduced 1/f³ Phase Noise Corner, Extended Tuning Range and Inherent Divided Output

Jun Yin, Pui-In Mak, Franco Maloberti, and Rui P. Martins

FEATURES

Reduced 1/f³ Phase Noise Corner, 90kHz to 150kHz
Extended Frequency Tuning Range
Inherent divided-by-5/7 output
Small area, 0.003mm²
Silicon verified in 65nm bulk CMOS

DESCRIPTION

This work is a time-interleaved (TI) ring-VCO (RVCO) exhibiting an improved phase noise over a wide range of frequency offsets, an extended tuning range and an inherent divided output. Such features are achieved by substantially increasing the number of delay stages in a RVCO, such that the rich multi-phase sub-outputs can be combined through a time-interleaved method, generating a high-frequency output with a significantly lowered 1/f³ phase noise corner (). The critical block is the phase combiner, which features a timing window to minimize the delay offset and mismatch. A reconfigurable TI factor extends the tuning range over the same range of supply voltage (V_{DD}). The prototype is a 35-stage dual-mode TI-RVCO occupying 0.003 mm² in 65-nm CMOS, and has a selectable TI factor of 5 and 7. The measured is 150 kHz at 3.47 GHz, which is 6.2x less than that of a typical 5-stage RVCO. The tuning range covers 1.7 to 3.5 GHz (68.5%) over V_{DD} = 0.7 to 1 V. The multi-phase sub-outputs are the inherent divided output (÷ 5 or ÷ 7) that can be directly utilized in a PLL to save area and power.

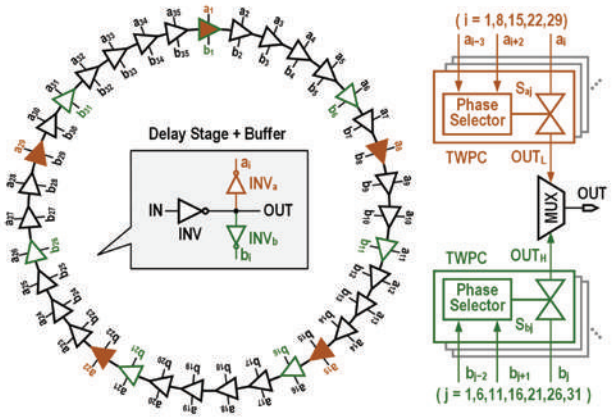

Fig. 1. Schematic of the proposed 35-stage dual-mode TI-RVCO.

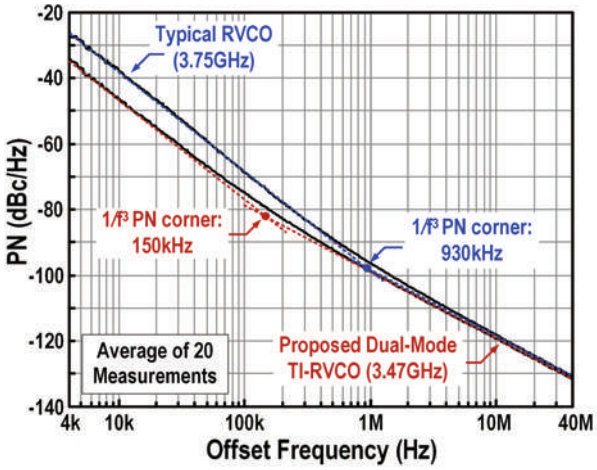

Fig. 2. Measured PN of the 35-stage dual-mode TI-RVCO and typical 5-stage RVCO at V_{DD} = 1V.

Publication(s):

[1] J. Yin*, P.-I. Mak*, F. Maloberti, and R. P. Martins*, "A Time-Interleaved Ring-VCO with Reduced 1/f³ Phase Noise Corner, Extended Tuning Range and Inherent Divided Output," IEEE Journal of Solid-State Circuits (JSSC), vol. 51, no. 12, pp. 2979-2991, Dec. 2016.

[2] J. Yin*, P.-I. Mak*, F. Maloberti, and R. P. Martins*, "A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f³ Phase-Noise Corner," IEEE International Solid- State Circuit Conference (ISSCC), Feb. 2016, pp. 48-49.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 0.038-mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop

Gengzhen Qi, Pui-In Mak, and Rui P. Martins

FEATURES

LO-defined Frequency (e.g., LTE Bands 5, 21, 2)
Low power consumption, 38.4 mW in transmit
20 mW in receive
Ultra-compact chip area, 0.038 mm²
Silicon verified in ST 65 nm CMOS

DESCRIPTION

In order to develop multiband cellular radios at low cost, on-chip N-path switched-capacitor (SC) filters are rekindled as a promising replacement of the off-chip SAW filters. The improved speed and parasitic effects of ultra-scaled CMOS technologies enable the N-path SC filters to provide tunable high-Q filtering over a wide range of frequencies.

This work is an N-path SC gain loop that can operate as an area-efficient SAW-less wireless transceiver (TXR) for multiband TDD communications. Unlike the typical direct-conversion transmitter (TX: BB Filter → I/Q modulation → PA driver) and receiver (RX: LNA → I/Q demodulation → BB Filter) that the functions are arranged in an open-loop style, here the signal amplification, bandpass filtering and I/Q (de)mod-ulation are unified in a closed-loop formation, being reconfigurable as a TX or RX with an LO-defined center frequency. The key advantages are low out-of-band (OB) noise in the TX mode, and high resilience to OB blockers in the RX mode.

Fabricated in 65-nm CMOS, the TXR prototype consumes up to 38.4 mW (20 mW) in the TX (RX) mode at the 1.88-GHz LTE-band2. The LO-defined center frequency covers >80% of the TDD-LTE bands with neither on-chip inductors nor external input-matching components. By properly injecting (extracting) the signals into (from) the N-path SC gain loop, the TX mode achieves an -1-dBm output power, a -40-dBc ACLREUTRA1 and a 2.0% EVM at 1.88 GHz, while showing a -154.5-dBc/Hz OB noise at 80-MHz offset. In the RX mode, a 3.2-dB NF and a +8-dBm OB-IIP3 are measured. The active area (0.038 mm2) of the TXR is 24x smaller than the state-of-the-art LTE solutions.

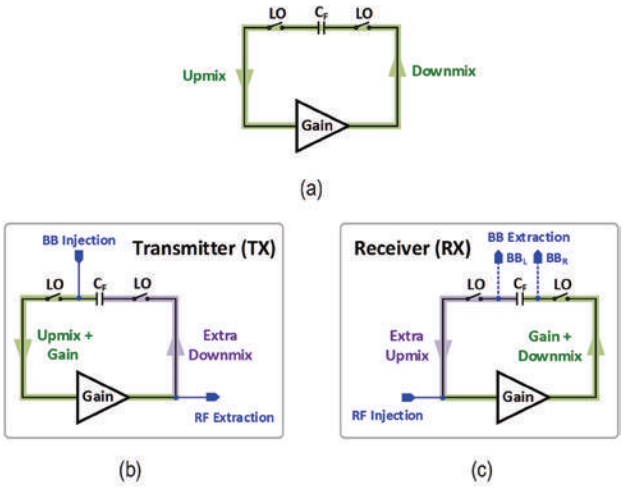

Fig. 1. An N-path SC gain loop operates as an area-efficient SAW-less wireless transceiver.

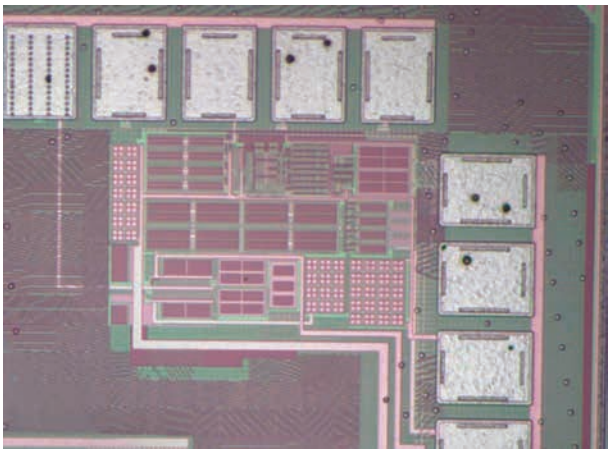

Fig. 2. Chip micrograph.

Publication(s):

[1] G. Qi, P.-I. Mak, R. P. Martins, "A 0.038-mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop," IEEE Journal of Solid-State Circuits, to appear, 2017.

[2] G. Qi, P.-I. Mak, R. P. Martins, "A 0.038mm² SAW-less Multi-Band Transceiver Using an N-Path SC Gain Loop," IEEE International Solid-State Circuits Conference (ISSCC), pp. 452-453, Feb. 2016.

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS
HIGH RESOLUTION ADCs

A 12-Bit 110MS/s 4-Stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique

Rui Wang, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Zhihua Wang, and Rui P. Martins

FEATURES

Background Calibrated Multi-Stage Pipelined-SAR ADC
Ratio-Based Gain Error Calibration Technique
Only one PN Injection to Calibrate Multiple Gain Stages
Low Power consumption 12mW
High Sampling Rate, 120MHz
High Resolution, SNDR=63dB
Excellent Power efficiency, FoM_W=85fJ/step
Active Area, 0.12mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 12-bit 120MS/s multi-stage pipelined SAR ADC integrated through a single low-gain op-amp. A ratio-based GEC (Gain Error Calibration) technique is proposed to reduce the complexity of digital calibration circuit. A timing-derived technique is employed to share a single op-amp for residue amplification between pipelined SAR stages, where three non-overlap phases are allocated to maximize both usable bits and op-amp amplification time in each sampling period. Only one PN (Pseudo-random Number) signal is employed to perform the dither injection but calibrate multiple gain errors, and thus accelerates the convergence speed and minimizes the analog modification due to the background calibration. The effectiveness of the architecture is verified in a 65-nm CMOS chip whose active core area is 0.12 mm^2 only. The ADC obtains a peak SNDR of 63.2 dB and SFDR of 75.2 dB at 120MS/s consuming 12mW from a 1.2-V supply. Only 40 thousand points are needed to achieve desirable SNDR with the proposed calibration technique.

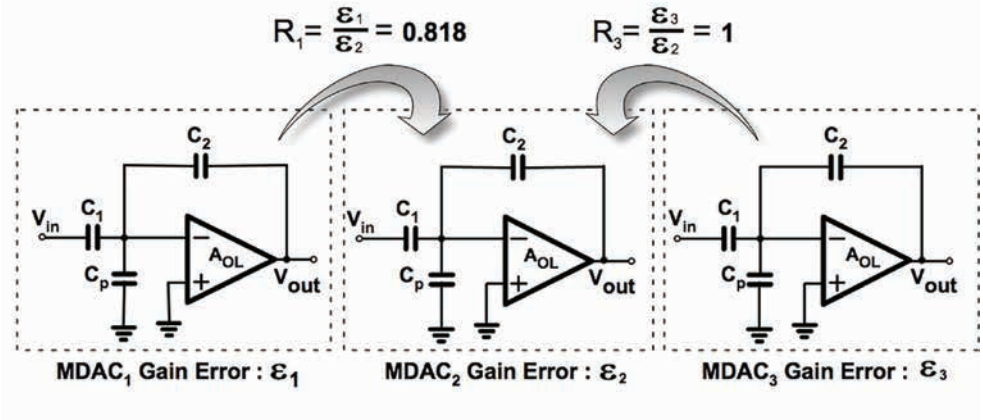

Fig. 1. Gain error ratios tracking between each MDAC.

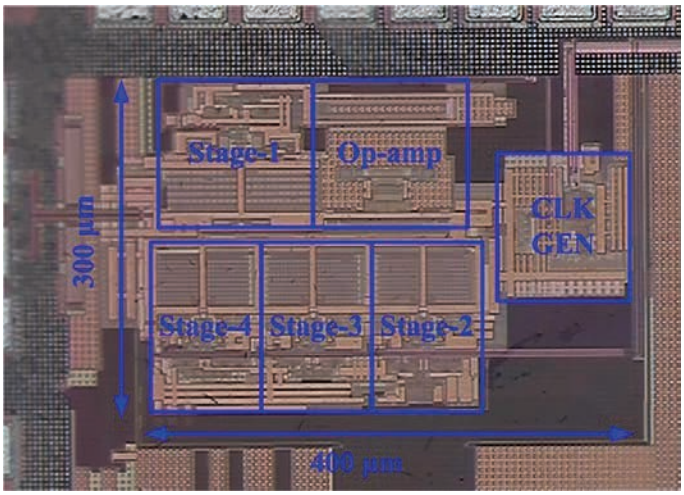

Fig. 2. Chip Photograph.

Publication(s):

[1] R. Wang*, U-Ft Chio*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*, "A 12-Bit 110MS/S 4-Stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique", in Proc. IEEE European Solid-State Circuits Conference – ESSCIRC 2012, Sept 2012.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 22.4μW 80dB SNDR ΣΔ modulator with passive analog adder and SAR Quantizer for EMG Application

Zhijie Chen, Yang Jiang, Chenyan Cai, He-Gong Wei, Sai-Wen Sin, Seng-Peng U, Zhihua Wang, and Rui P. Martins

FEATURES

Multi-bit Sigma-Delta ADC using SAR Quantizer
Passive Analog Summation in SAR DAC Array
Very Low Power consumption 22.4μW
Sampling Rate 1MS/s
High Resolution, SNDR=80dB
Good Power efficiency, FoM_W=130fJ/step
Active Area, 0.13mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

A Feed-Forward (FF) multi-bit ΣΔ modulator with passive analog adder and 4-bit Successive Approximation (SA) quantizer is presented. The scheme is composed by two SC integrators and a 4-bit SAR quantizer with feedback Data-Weighted Averaging (DWA). The modulator covers the 10KHz bandwidth according to electromyography application. The design utilizes the same DAC array of the SAR quantizer to realize analog summation for the FF signal, which significantly reduces the power dissipation and the silicon area. The modulator operates at 1MS/s with 1V supply. The prototype chip implemented in 65nm CMOS achieves 80dB SNDR and 81dB DR with 22.4μW power consumption. The Figure of Merit (FoM) is 0.13 pJ/conv.-step.

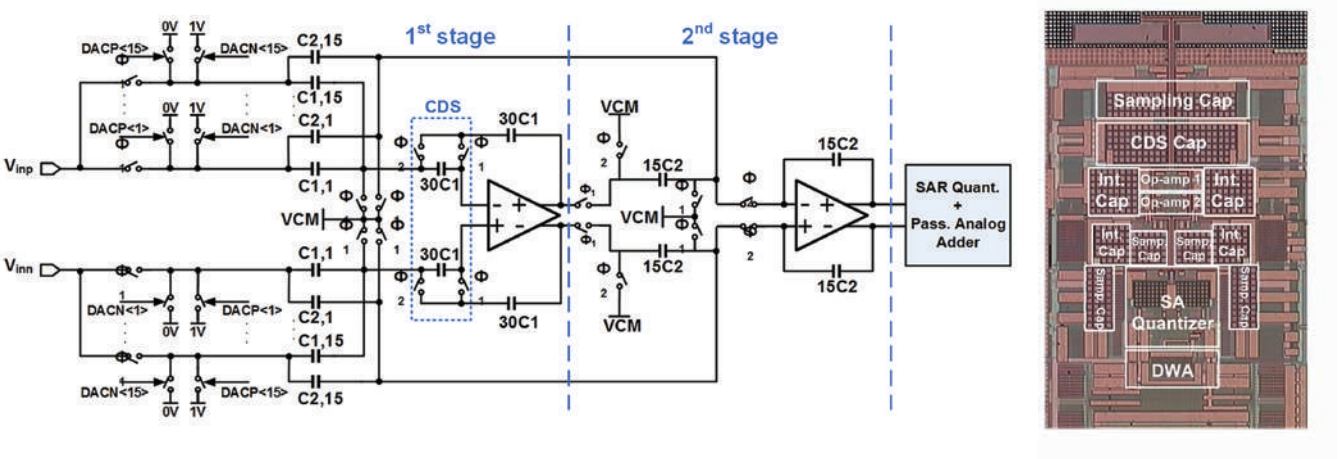

Fig. 1. Circuit Diagram of the Proposed Sigma-Delta ADC and Chip Photograph.

Publication(s):

[1] Z. Chen*, Y. Jiang*, C. Cai*, H.-G. Wei*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*, "A 22.4μW 80dB SNDR ΣΔ Modulator with Passive Analog Adder and SAR Quantizer for EMG Application", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 257-260, Nov 2012.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 13-bit 60MS/s Split Pipelined ADC with Background Gain and Mismatch Error Calibration

Li Ding, Wenlan Wu, Sai-Weng Sin, Seng-Pan, U, and Rui P. Martins

FEATURES

Split Pipelined ADC
Gain and Mismatch Calibration
Background Calibration
Power consumption 63.8mW
High Sampling Rate, 60MHz
High Resolution, SNDR=69dB
Good Power efficiency, FoM_W=452fJ/step
Active Area, 0.93mm^2
Silicon verified in UMC 90nm CMOS

DESCRIPTION

A comprehensive background gain and mismatch error calibration technique is proposed for split ADC, without injecting any test signal. By employing comparator threshold random selection method, the input/output transfer characteristics of each split ADC channel is differed, which allow their residue transfer curves are uncoupled and hence the calibration can be extended to any pipeline stages. Based on Least Mean Square (LMS) adaptation the interstage gain error and capacitor mismatch error are corrected. All the estimations and corrections are performed in digital domain, resulting in little analog circuit modification. The proposed calibration technique is applied on a 13-bit 60MS/s pipelined ADC. Fabricated in a 90nm CMOS process, the ADC achieves 70.8dB SNDR at a power consumption of 63.8mW. The FoM is 377fJ/ step at DC and 452 fJ/ step at Nyquist.

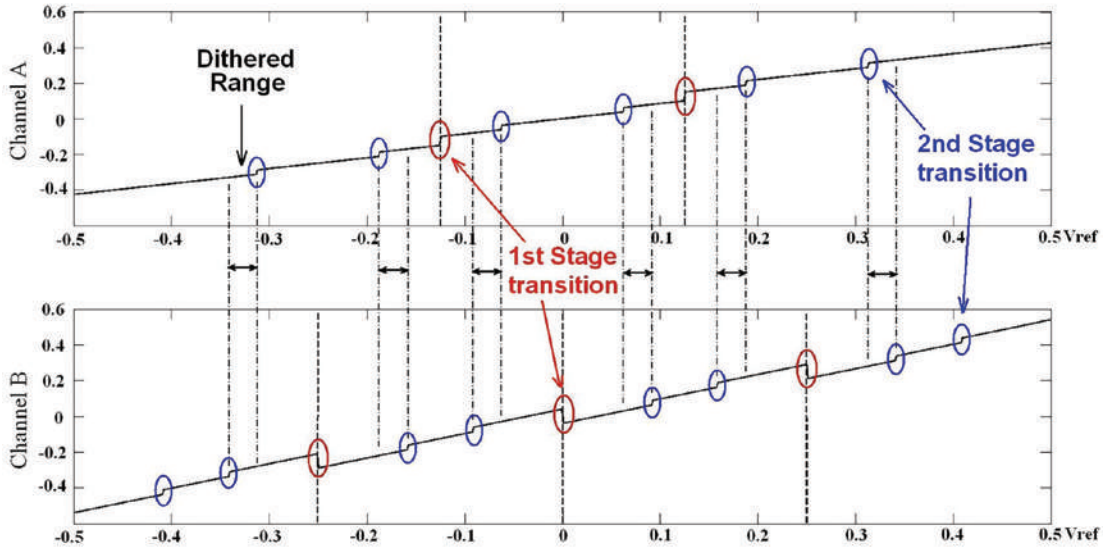

Fig. 1. Proposed Dithered ADC Transfer Characteristics.

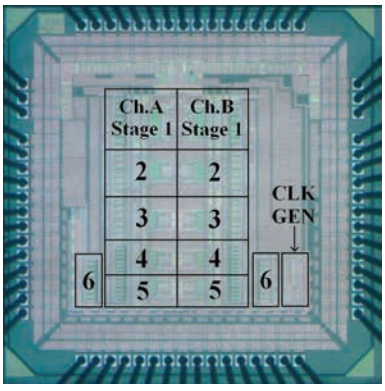

Fig. 2. Chip Photograph.

Publication(s):

[1] L. D., W. Wu, S.-W. Sin, S.-P., U, R .P. Martins, " A 13-bit 60MS/s split pipelined ADC with background gain and mismatch error calibration ", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 77-80, Nov 2013.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters

Da Feng, Franco Maloberti, Sai-Weng Sin, and Rui P. Martins

FEATURES

Theoretical Analysis of the Polyphase Decomposition Technique to the NTF of Band-Pass ΣΔ modulators
Generalized and Tunable Band-Pass Implementation
Mismatch Spurs Out-of-band
Applicable to MASH structures

DESCRIPTION

The use of the polyphase decomposition technique applied to the noise transfer function (NTF) of band-pass sigma-delta (BPΣΔ) modulators is introduced and theoretically analyzed. Schemes for a second order and fourth order bandpass noise shaping are discussed in detail. The class of architectures studied here does not use resonators and avoids spur tones in the signal band. Those architectures are based on the polyphase decomposition applied only to the NTF of band-pass modulators (or to any other NTF responses). The signal transfer function (STF) remains unchanged with respect to the originating single path. The method is usable for any order but the analog inaccuracy limits its application. It is shown that an extension to MASH configurations is possible. The method allows tunability of the center frequency over a wide frequency range. Moreover, MASH schemes allow a rough-fine tuning with the rough tuning in the analog section followed by a fine digital adjustment. Simulation results verify the benefits and outline possible limits.

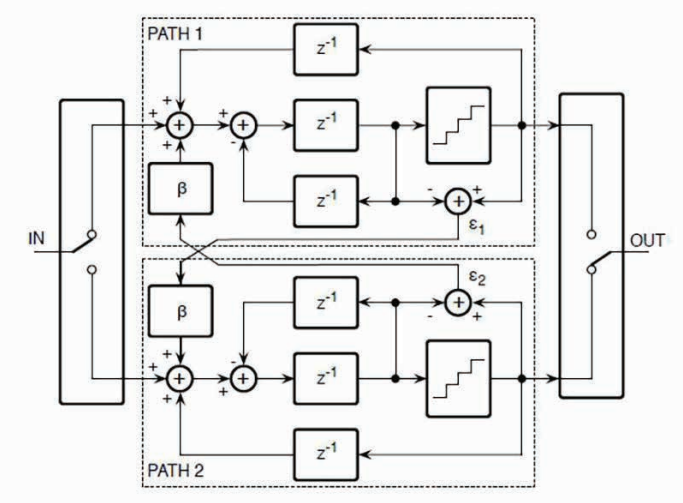

Fig. 1. A 2nd order band-pass polyphase sigma-delta ADC.

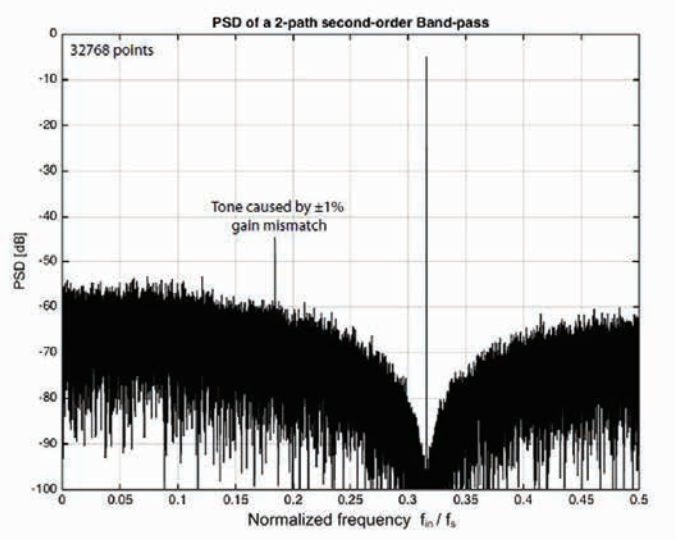

Fig. 2. FFT Spectrum.

Publication(s):

[1] D. Feng, F. Maloberti, S.-W. Sin, R. P. Martins, "Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 5, Issue 4, pp. 537-547, Dec. 2015.

* Contributors with University of Macau

Sponsorship:

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A High DR Multi-Channel Stage-Shared Hybrid Sigma-Delta Analog Interface for Integrated Power Electronics Controller Front-End

Yuan Ren, Sai-Weng Sin, Chi-Seng Lam, Man-Chung Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Hybrid CT-DT ΔΣ Modulator with PGA Front-End
Opamp Shared in Discrete Stage
Low power consumption,68μW/Channel
High Dynamic Range, 98dB
Excellent Power efficiency, FoM_S = 179dB
Very Small Active Area, 0.03mm²/channel
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 4-channel power electronics (PE) controller front-end interface with input signal conditioning and analog-to-digital (A/D) conversion functions for different power electronics system applications. The proposed front-end is composed of a 4-channel continuous-time (CT) and discrete-time (DT) hybrid sigma-delta modulator (H-ΣΔM) embedding an input programmable-gain (PGA) in the first CT stage in order to enhance the dynamic range (DR). The second shared DT stage is designed to utilize multiple-sampling technique with a shared single Op-Amp for low power consumption. This PE controller front-end chip is fabricated with 65 nm CMOS technology. Measurement results show a high dynamic range of 98.3 dB and 84.2 dB SNDR, while achieving a power consumption of 68 μW per channel and a FoMS of 172-179 dB due to the dynamic range boost.

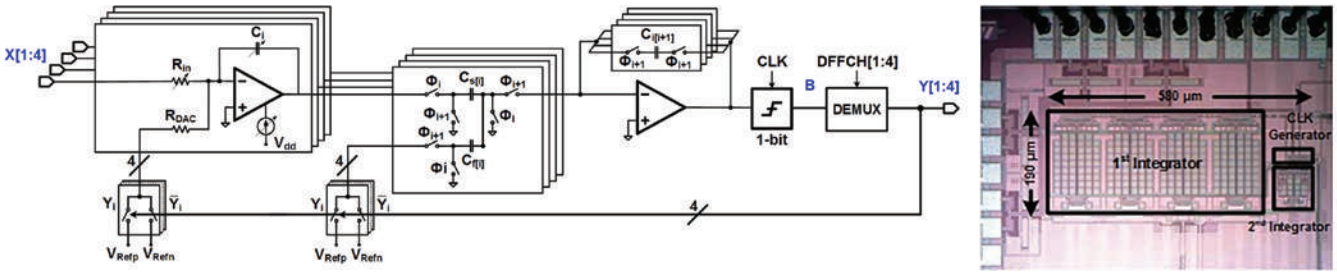

Fig. 1. The Multi-Channel Front-End Architecture and Chip Photograph.

Publication(s):

[1] Y. Ren, S.-W. Sin, C.-S. Lam, M.-C. Wong, S.-P. U, R. P. Martins, " A High DR Multi-Channel Stage-Shared Hybrid Front-End for Integrated Power Electronics Controller", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 1-4, Nov 2016.

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A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing

Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, and Rui P. Martins

FEATURES

Cascaded MASH DT-ΔΣ Modulator
Proposed Multirate Opamp Sharing Scheme
Low power consumption, 4.2mW
Wide bandwidth, 5MHz
High Resolution, SNDR=77.1dB
Excellent Power efficiency, FoM_S=168dB
Very Small Active Area, 0.066mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a discrete time (DT) 2-1 MASH Delta-Sigma (ΔΣ) modulator with multirate opamp sharing for Analog-to-Digital Converters (ADC), targeting the optimization of power efficiency in active blocks, like opamps and quantizers. Through the allocation of different settling times to the opamps and by adopting the multirate technique, the power of the shared opamps is utilized more efficiently, and the 4-bit SAR quantizer and the Data Weighted Averaging (DWA) in the first stage enjoy additional operation time. Moreover, a detailed analysis and related simulations are presented to validate the enhanced opamp power efficiency in the proposed sharing scheme. The 65nm CMOS experimental chip running at multirate 120/240MHz achieves a mean SNDR of 77.1dB for a 5MHz bandwidth, consuming 4.2mW from a 1.2V supply and occupying 0.066mm2 core area. It exhibits a Walden FoM of 69.7fJ/conv-step and a Schreier FoM of 167.9dB based on SNDR.

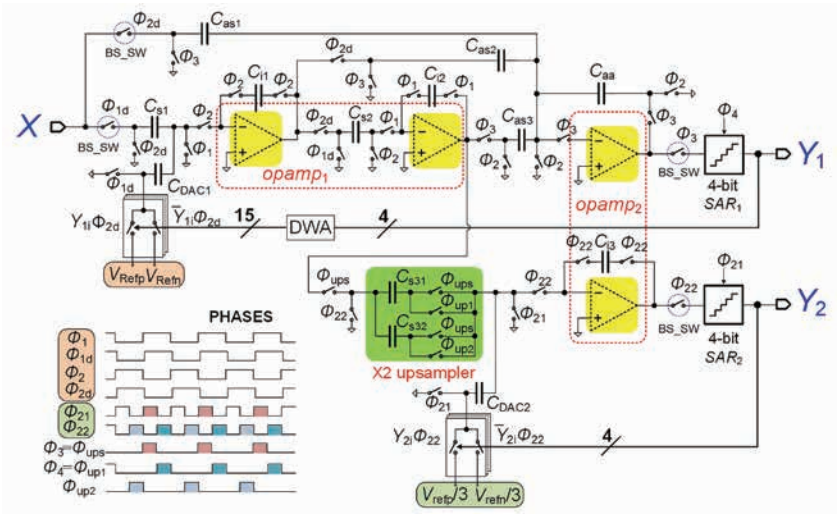

Fig. 1. ADC architecture.

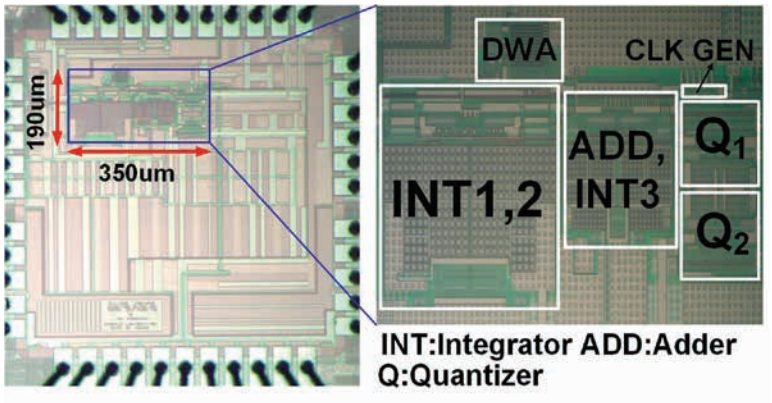

Fig. 2. Chip Photograph.

Publication(s):

[1] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, R. P. Martins, " A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing", IEEE Trans. of Circuits and Systems I – Regular Papers. in press, 2017.

[2] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, R. P. Martins, " A 12.5-ENOB 5MHz BW 4.2mW DT Multirate 2-1 Mash ΔΣ Modulator with Horizontal/Vertical Opamp Sharing in 65nm CMOS' in IEEE International Solid-State Circuits Conference, Student Research Preview, Jan 2016.

* Contributors with University of Macau

Sponsorship:

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Active-Passive ΔΣ Modulator for High Resolution and Low Power Applications

Arshad Hussain, Sai-Weng Sin, Chi-Hang Chan, Seng-Pan U, Franco Maloberti, and Rui P. Martins

FEATURES

Hybrid Active-Passive Integrator DT-ΔΣ Modulator
Proposed Positive Feedback NTF Zero Compensation
Very Low power consumption, 73.6μW
Audio bandwidth, 25kHz
High Resolution, SNDR=88.2dB
Excellent Power efficiency, FoM_S=176dB
Very Small Active Area, 0.1mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper discusses the use of a Low Gain Amplifier and a Passive Switched-capacitor (SC) network to enable the SC integrator function. The method is applied to a Delta-sigma Modulator to achieve high resolution as proven by the 65nm CMOS Technology Test Vehicle. Compared to the conventional operational amplifier (op-amp) based SC integrator, this solution utilizes a low gain open loop amplifier to drive a passive SC integrator with positive feedback. Since the open loop amplifier requires a low DC gain and implements an embedded current adder, the power consumption is very low. Power reduction is obtained by using passive feedforward with built-in adder to assist the first amplifier. The low swing obtained at the output of the active blocks relaxes the slew rate requirement and enhances the linearity. Implemented in 65-nm digital CMOS technology with an active area of 0.1-mm², the test chip achieves a dynamic range (DR) of 91dB, peak signal-to-noise ratio (SNR) of 88.4dB, peak signal-to-noise-plus-distortion ratio (SNDR) of 88.2dB, and a spurious free dynamic range (SFDR) of 106dB while consuming 73.6μW in a 25-kHz signal bandwidth at 1V supply, yielding a Walden FoM of 70fJ/Conversion-Step and Schreier FoM of 176dB.

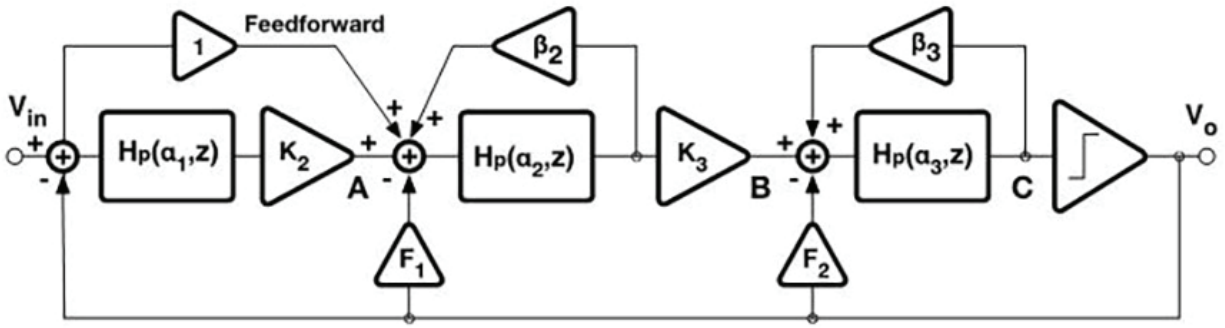

Fig. 1. ADC architecture.

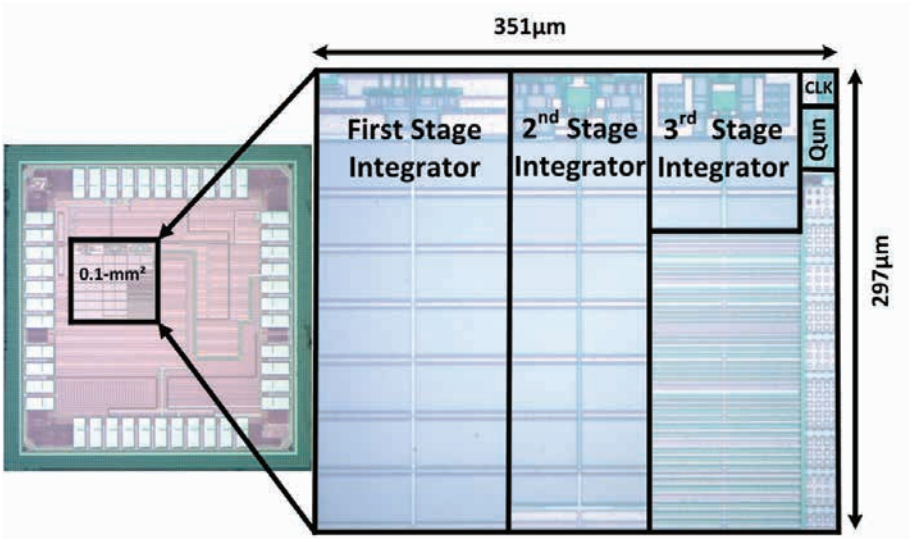

Fig. 2. Chip Photograph.

Publication(s):

[1] A. Hussain, S.-W. Sin, C.-H. Chan, S.-P. U, F. Maloberti, R. P. Martins, "Active-Passive ΔΣ Modulator for High-Resolution and Low-Power Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 1, pp. 364 – 374, Jan 2017.

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