

UNIVERSITY OF MACAU

Major Programme:	Master				oelectr	onics	& Mas	ter of	Philoso	ophy	in Micr	oelecti	ronics	ı			
Course Type:	□ CM - Compulsory Major □ L&S - Languages and Skills □ *GE - General Education □ MI - Minor □ RE - Required Elective □ CPE - Community and Peer Education □ *GE - General Education □ FE - Free Elective												ective				
Course Title: (in Chinese and English)	Digital 數字集			ircuits	uits				Suggested Year of Study:			Year 1					
Duration:	☑ Semester Course				Yearly Course			Credit Units:			3						
Grading System:	☑ Letter Grade				☐ P/NP			Pre-1	requisi y)	te:	None						
Medium of Instruction:				Eı													
Course Description:	This is an introductory course in digital integrated circuits. It covers topics from MOS inverters and different logic family. The student will learn how to model interconnect wires and design optimization with respect to a number of metrics: cost, reliability, speed and power. This course also cover sequential and dynamic logic circuit design, timing considerations, and clocking approaches, as well as design of large system blocks, including memories, such as D-flip-flop and SRAM. This customized course from bottom-up based, which starts from the fundamental techniques for the design and analysis of digital circuits. Then, it provides a detailed understanding of basic logic synthesis and analysis algorithms, and to enable students to apply this knowledge in the design of digital systems and EDA tools. The course aims to give a basic idea of the digital integrated circuit design. The students will have a hands-on experience on combinational circuit optimization (two-level and multi-level synthesis), sequential circuit optimization (state encoding, retiming), timing analysis, testing, and logic verification through the lab work.																
Intended Learning Outcomes (ILO):	• 5	 This course enables students to have: To introduce the essential knowledge in digital circuits design both for custom and auto-genration schemes To introduce common digital circuit building blocks, such as logic gates, adder and SRAM, with practical considerations. To teach students with hands on experience on designing and simulating digital circuits using industrial simulation tools with real world CMOS process. To teach students with hands on experience on the digital standard cell design with real physical layout consideration using industrial layout tools in CMOS process 															
Major Assessment Methods:			Role Playing	Student Presentation	Individual project / paper	Group project / paper	Group discussions	Writing Assignment	Exercises & problems	Service learning	Internship	Field study	Company visits	Reading & Writing Assessments / tests	Listening & Oral Assessments / tests	Others (please specify)	
Class Participation / Discussion10	%								√								
Assignment(s)10	%								√								
Test(s)	%								√								
Examination 20	%								V								
Others: Project 40	_%			√	√												
Course Content: (topic outline)		- Bas Add - Mod - Oth layo	ic comler desideling of the logical	oination gn and of inter c famili O-Flip-	nal logi layout connectes: pass	c overv t wires s gate l d SRA	and op	MOS i timizat ynamic gn and	nverter ion of c logic a	s, Nar lesign	caling. nd gate, : Elmore mino lo	e delay	theory	and log	gical ef	fort.	

Template revised on 20 Oct 2017